Design Considerations of UFS & e.MMC Controllers

Compliance & Compatibility

Yuping Chung

Arasan Chip systems, Inc.
San Jose, CA
Agenda

• Mobile Storage in SoC
• Challenges to Mobile Storage Controller Designs
• Enabling Mobile Storage Design Ecosystem
• Summary
Multiple Mobile Storage Interfaces in Application Processor

- Touch Screen
- Audio Spkr, Mic
- LCD Display
- Camera
- 4G/3G Modem
- WiFi

- I2C / SPI
- Slimbus
- MIPI DSI
- MIPI CSI-3
- HSI, LLI
- HSIC
- SDIO

- LPDDR2 DRAM
- GPMC

- UFS 1.1 / 2.x
- e.MMC 4.51 / 5.x
- SD 3.0/4.0

- SATA-2
- USB2.0/3.0
- USB3.0 OTG

- Keyboard
- GPIO
- UART
- PC
- CLK

- HDMI 1.4a

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- HDMI 1.4a
Mobile Storage Evolution Faster Than Ever

UFS

- e.MMC 4.3 Boot-up
- SD 2.0 High Capacity
- MMC 4.2 High Speed
- e.MMC 4.1 DDR
- e.MMC 4.51 HS200 200MB/s
- e.MMC 5.x

e.MMC

- SD 1.0 High speed
- SD 1.1 High speed
- SD 2.0 High capacity
- SD 3.0 UHS-I 104MB/s 1,4-bit
- SD 4.0 UHS II 1.56 Gbps Serial Differential
- Early Adopter
- Next Gen


UFS 1.0  UFS 1.1  UFS 2.x

2006-2009

2009-2012

2012-2013

Global Standards for the Microelectronics Industry
Challenges of Backward Compatibility

e.MMC

<table>
<thead>
<tr>
<th></th>
<th>e.MMC 4.41</th>
<th>e.MMC 4.51</th>
<th>e.MMC5.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Throughput</td>
<td>High Speed</td>
<td>HS200</td>
<td>HS400</td>
</tr>
<tr>
<td></td>
<td>832 Mbps</td>
<td>1.6 Gbps</td>
<td>3.2 Gbps</td>
</tr>
<tr>
<td>Data Lines</td>
<td>4 or 8-bit</td>
<td></td>
<td>8-bit</td>
</tr>
<tr>
<td>Signal Count</td>
<td>10 Pins</td>
<td></td>
<td>11 Pins</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Data Strobe)</td>
</tr>
<tr>
<td>IO Voltages</td>
<td>1.2 V / 1.8 V</td>
<td>3 V</td>
<td>1.2 V / 1.8 V</td>
</tr>
<tr>
<td>Interface</td>
<td>DDR-52</td>
<td>SDR-200</td>
<td>DDR-200</td>
</tr>
<tr>
<td>Data Strobe</td>
<td>No</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Tuning (Read)</td>
<td>No</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>0 – 52 MHz</td>
<td>0 – 200 MHz</td>
<td></td>
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</tbody>
</table>
e.MMC Compliance

- e.MMC Device spec published by JEDEC
- Compliance can be done through 3rd party Compliance Testers
  - No formal compliance guidelines
Challenges of Backward Compatibility

UFS

<table>
<thead>
<tr>
<th>Transaction Layer</th>
<th>Host Interface</th>
<th>UFS 1.0</th>
<th>UFS 1.1</th>
<th>UFS 2.0</th>
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<tbody>
<tr>
<td>Link Layer</td>
<td>UniPro™</td>
<td>v1.40</td>
<td>v1.41</td>
<td>v1.60</td>
</tr>
<tr>
<td># of Lanes</td>
<td>Single Lane</td>
<td>Single Lane</td>
<td>2-Lane</td>
<td></td>
</tr>
<tr>
<td>Physical Layer</td>
<td>M-PHY</td>
<td>v1.0</td>
<td>v2.0</td>
<td>v3.0</td>
</tr>
<tr>
<td>Data Rate</td>
<td>1.5 Gbps</td>
<td>2.9 Gbps</td>
<td>5.8 Gbps</td>
<td></td>
</tr>
<tr>
<td># of Lanes</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>Tx +/-, Rx +/-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diff V peak-peak</td>
<td>500 mV Max (non-terminated)</td>
<td>250 mV Max (terminated)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: JEDEC
UFS 1.1 Compliance

<table>
<thead>
<tr>
<th>Protocol</th>
<th>Rev.</th>
<th>Test Spec</th>
<th>Certification</th>
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<tbody>
<tr>
<td>Transaction</td>
<td>UFS</td>
<td>1.1</td>
<td>UFSA</td>
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<tr>
<td>Link Layer</td>
<td>UniPro</td>
<td>1.41</td>
<td>MIPI / UNH-OL</td>
</tr>
<tr>
<td>PHY Layer</td>
<td>M-PHY</td>
<td>2.0</td>
<td>M-PHY CTS_v0.99</td>
</tr>
</tbody>
</table>

Source: JEDEC
Design Challenges

Can I have all these validated before starting my SoC design?

1. Compliance to Industry Standard(s)
   - JEDEC
   - mipi
   - e.MMC
   - UFS
   - UniPro™
   - M-PHY™
   - Physical Layer
   - Link Layer
   - Application Layer
   - SD
   - SDIO
   - SDA
   - UFSA
   - UFS
   - UHS-II
   - e.MMC
   - UniPro 1.40
   - M-PHY 1.0
   - SD 2.0
   - UHS-? 1.0
   - UHS-II
   - 2.0
   - UHS-?
   - 3.0
   - 4.0
   - 4.x

2. Backward Compatibility
   - e.MMC 4.3 → 4.4 → 4.5 → 4.51 → 5.x
   - UFS 1.0 → 1.1 → 2.x
   - UniPro 1.40 → 1.41 → 1.6x
   - M-PHY 1.0 → 2.0 → 3.x
   - SD 2.0 → 3.0 → 4.0 → 4.x
   - UHS-II → UHS-?

3. Inter-Operability
   - Data/File Transfer
   - Read/Write Commands
   - Link Initialization
M-PHY Verification Before Silicon
M-PHY Verification Before Silicon

- Reset & Initialization
- Coverage Collection
- Constrained random stimulus
- Functional Check

DUT M-PHY

VIP

UVC RMMI Master

Sequencer

Scoreboarding

VIP

UVC RMMI Monitor

DATA

CTRL

DPDN

VIP

UVC DPDN Monitor

VIP

M-PHY Agent

VIP

M-PHY Agent

VIP

UVC DPDN

Global Standards for the Microelectronics Industry
Verifying Complete UFS Before Silicon
UFS-HCI + UniPro
Migrate to FPGA based System

- A black-box approach enables quick access to a validation platform
- FPGA with Verified UFS IP
FPGA based System for Device Validation & Software Development

Tested M-PHY™ Signals

Certified UniPro™

Verified and Tested UFS-HCI or System Bus Interface

Verified and Tested Driver and Stacks
Enabling UFS/e.MMC Design Ecosystem

• FPGA based Development Platform productized into Validation Platform
  – IP, software stacks and PHY come together

• Used by IP vendor (eg. Arasan) for Interoperability testing with other pioneers

• Used by Test & Measurement vendors as target platforms
  – For validation of protocol generators and analyzers

• Ultimately used by SoC/Device vendors as target or reference platforms for silicon validation
  – Assured of IP interoperability, compliance, and backward compatibility
Summary

- **New JEDEC storage standards** continue to evolve for new markets
  - Early IP/SoC validation enables compliance and compatibility for fast time-to-market

- **Different SoC vendors at different stages of spec adoption**
  - Different spec revisions from different OEM’s
  - Backward compatibility and Interoperability a must among vendors

- **IP vendors** continue to
  - Leading the pack to invest in transforming specs to RTL and GDSII
  - Keeping Backward Compatibility with older standards in new designs
  - Enabling ecosystem-wide Inter-op and Compliance through
    - Software stacks
    - Hardware Validation Platforms

*All these are made available before starting your SoC/Device designs!!*
Design for Compliance and Compatibility

THANK YOU