Design Considerations of UFS & *e*.MMC Controllers

Compliance & Compatibility

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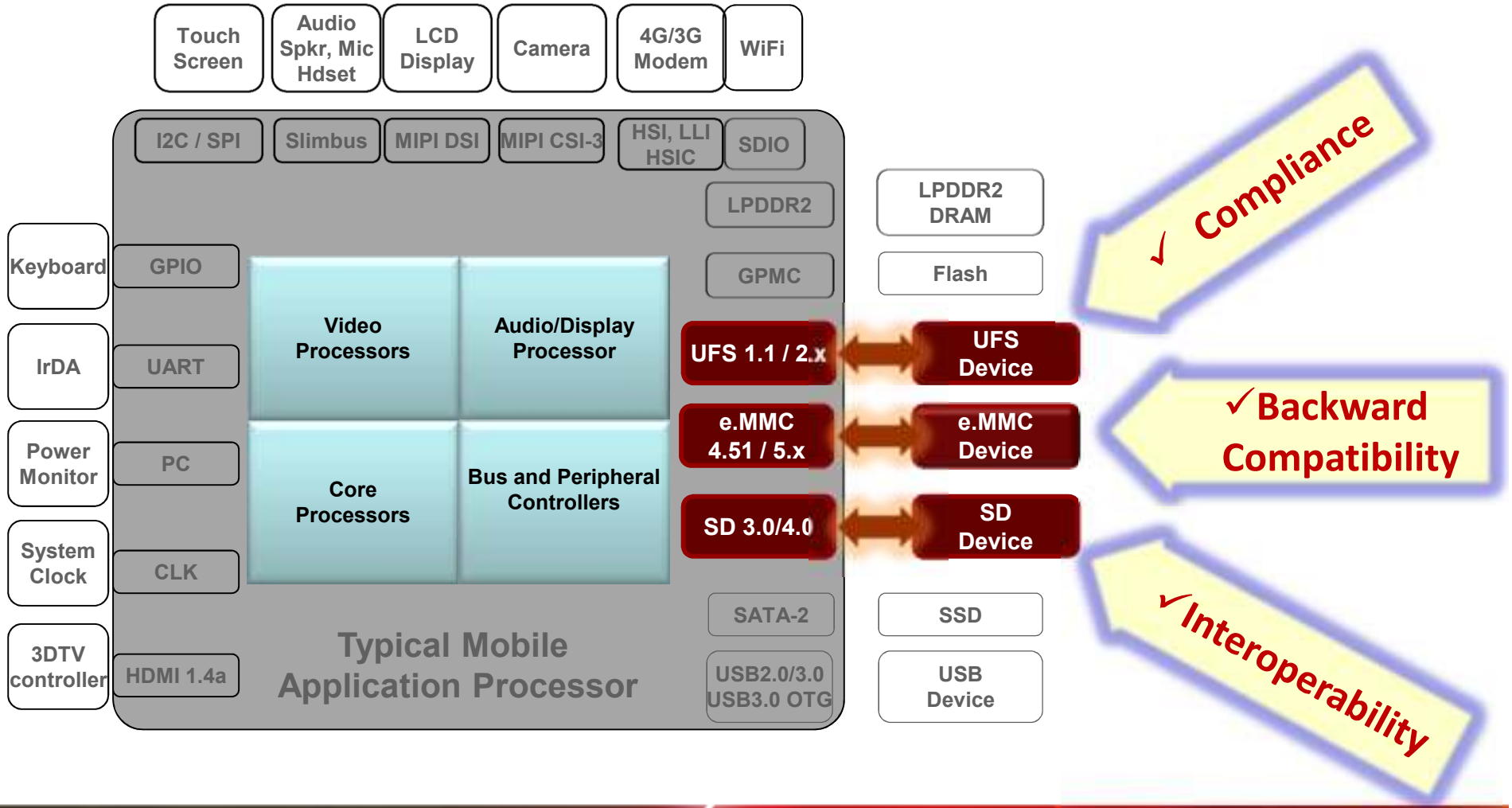
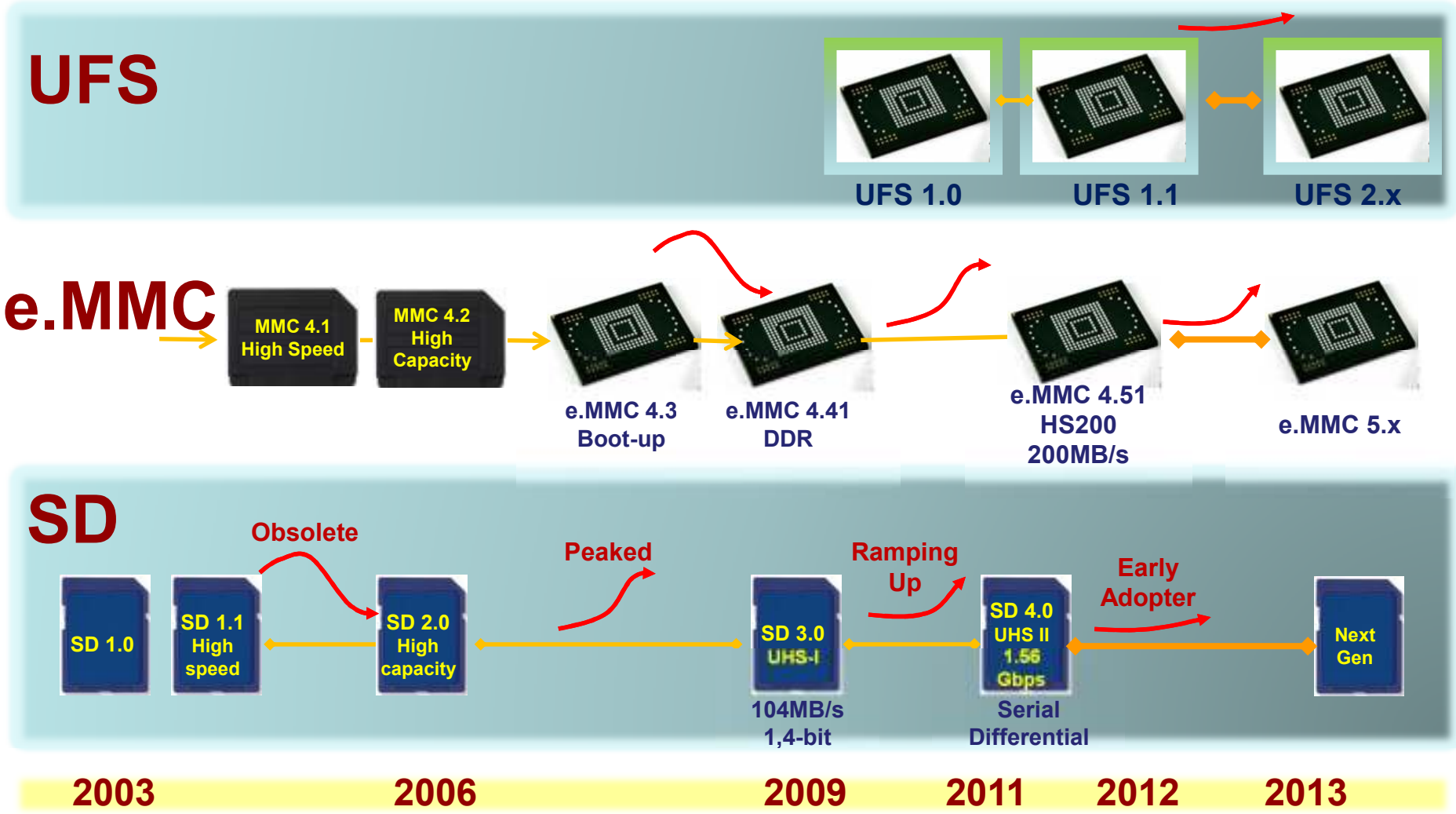
Agenda

- Mobile Storage in SoC
- Challenges to Mobile Storage Controller Designs
- Enabling Mobile Storage Design Ecosystem
- Summary

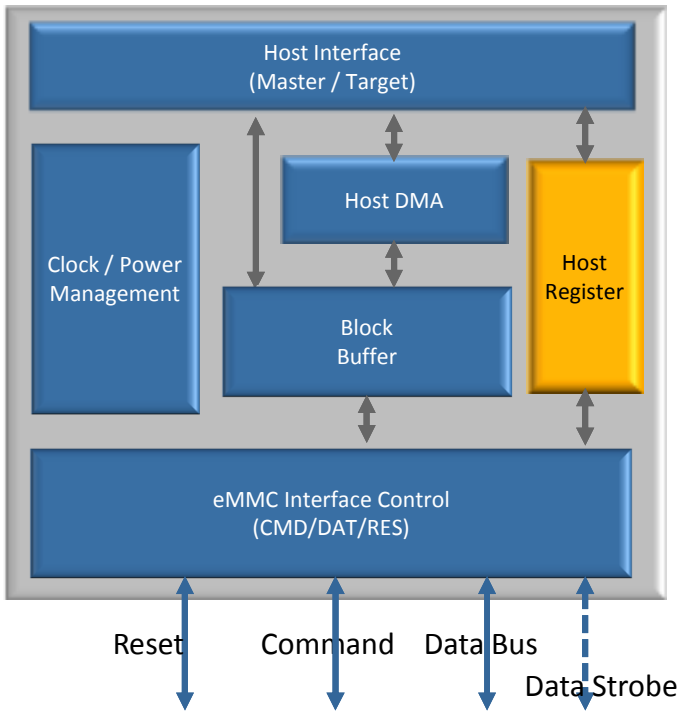
Multiple Mobile Storage Interfaces in Application Processor



Mobile Storage Evolution Faster Than Ever



Challenges of Backward Compatibility e.MMC

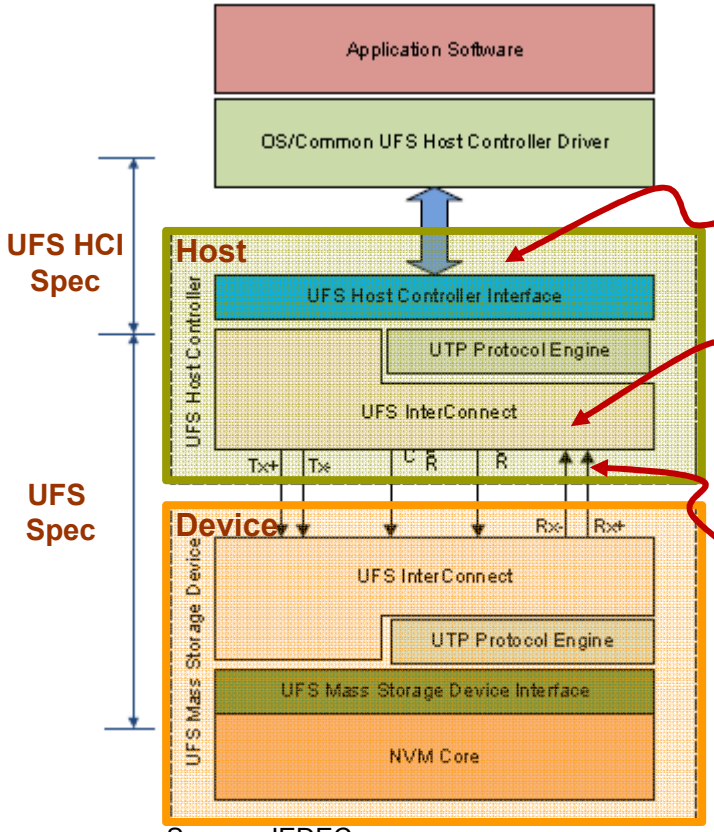


	e.MMC 4.41	e.MMC 4.51	e.MMC5.0
Max Throughput	High Speed 832 Mbps	HS200 1.6 Gbps	HS400 3.2 Gbps
Data Lines	4 or 8-bit		8-bit
Signal Count	10 Pins		11 Pins (Data Strobe)
IO Voltages	1.2 V / 1.8 V 3 V		1.2 V / 1.8 V
Interface	DDR-52	SDR-200	DDR-200
Data Strobe	No		Yes
Tuning (Read)	No	Yes	
Clock (MHz)	0 – 52 MHz	0 – 200 MHz	

e.MMC Compliance

- e.MMC Device spec published by JEDEC
- Compliance can be done through 3rd party Compliance Testers
  - No formal compliance guidelines

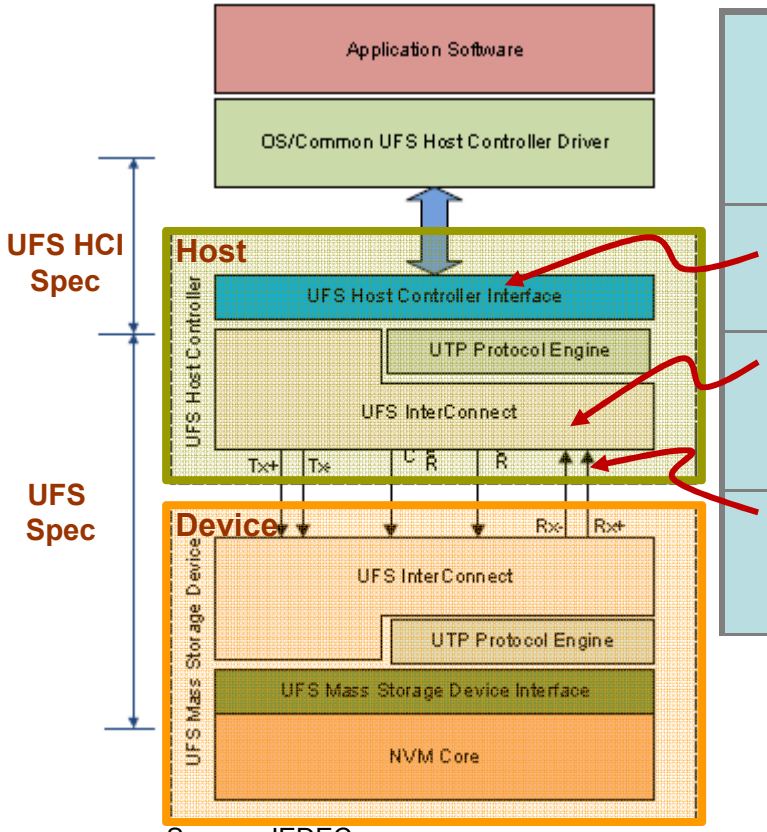
Challenges of Backward Compatibility UFS



Source: JEDEC

		UFS 1.0	UFS 1.1	UFS 2.0
Transaction Layer	Host Interface	HCI 1.0	HCI 1.1	HCI 2.0
Link Layer	UniPro™	v1.40	v1.41	v1.60
	# of Lanes	Single Lane	Single Lane	2-Lane
Physical Layer	M-PHY	v1.0	v2.0	v3.0
	Data Rate	1.5 Gbps	2.9 Gbps	5.8 Gbps
	# of Lanes	1		2
	Interface	Tx +/-, Rx +/-		
	Diff $V_{peak-peak}$	500 mV Max (non-terminated) 250 mV Max (terminated)		

UFS 1.1 Compliance

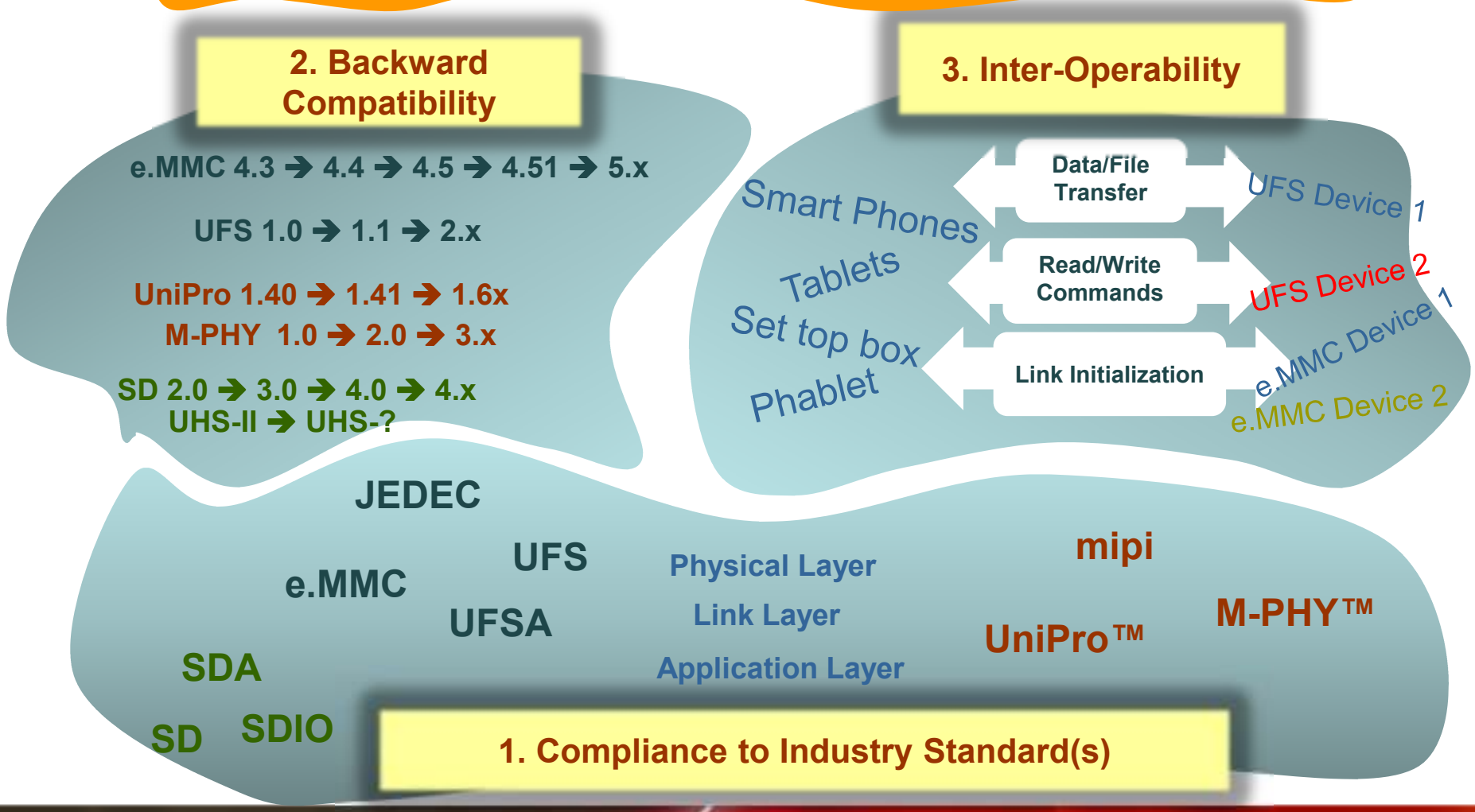


Source: JEDEC

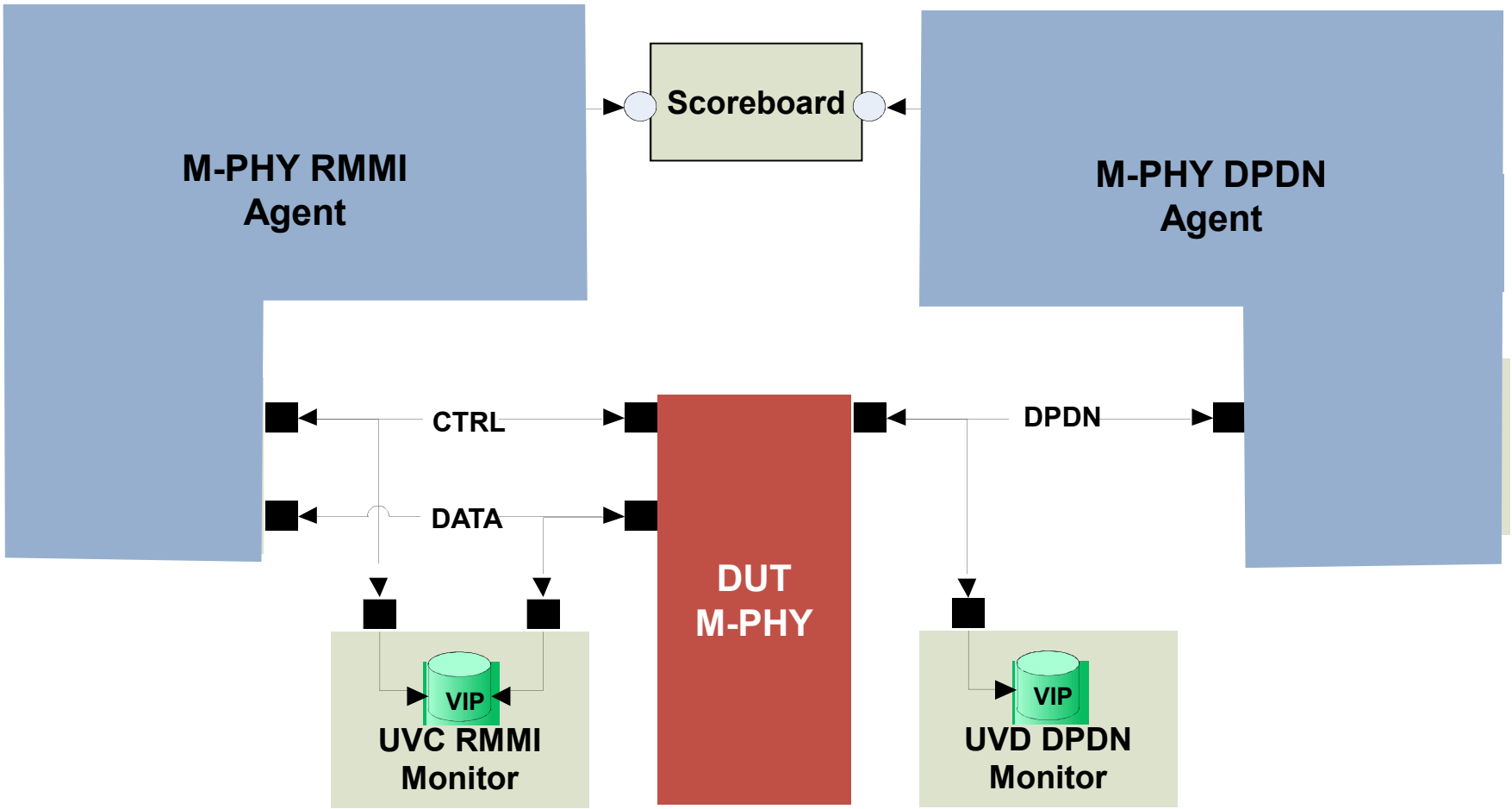
	Protocol	Rev.	Test Spec	Certification
Transaction Layer	UFS	1.1	UFS Test Spec v1.0	UFSA
Link Layer	UniPro	1.41	UniPro CTS_v1.0_r01	MIPI / UNH-OL
PHY Layer	M-PHY	2.0	M-PHY CTS_v0.99	

Design Challenges

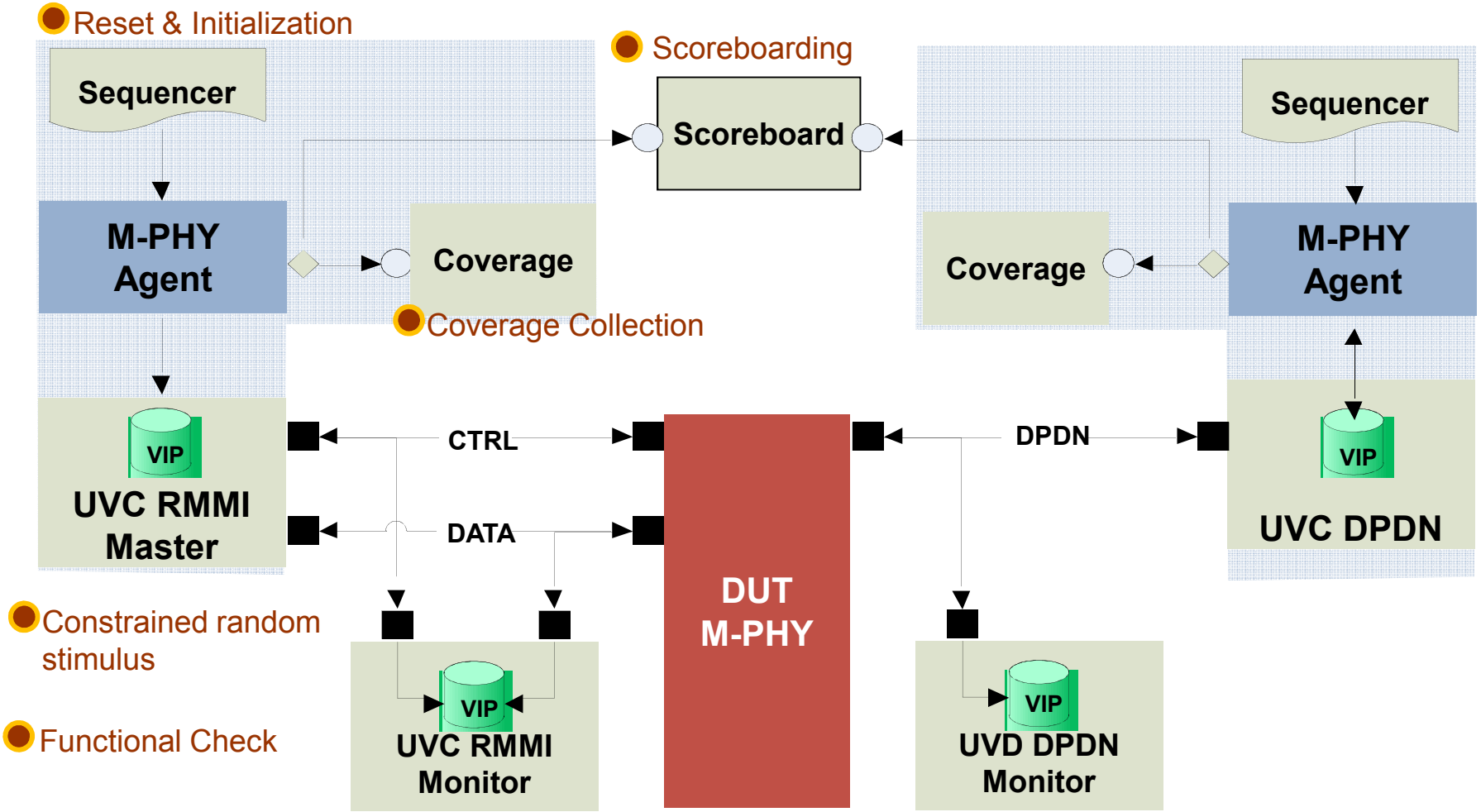
Can I have all these validated before starting my SoC design?



M-PHY Verification Before Silicon

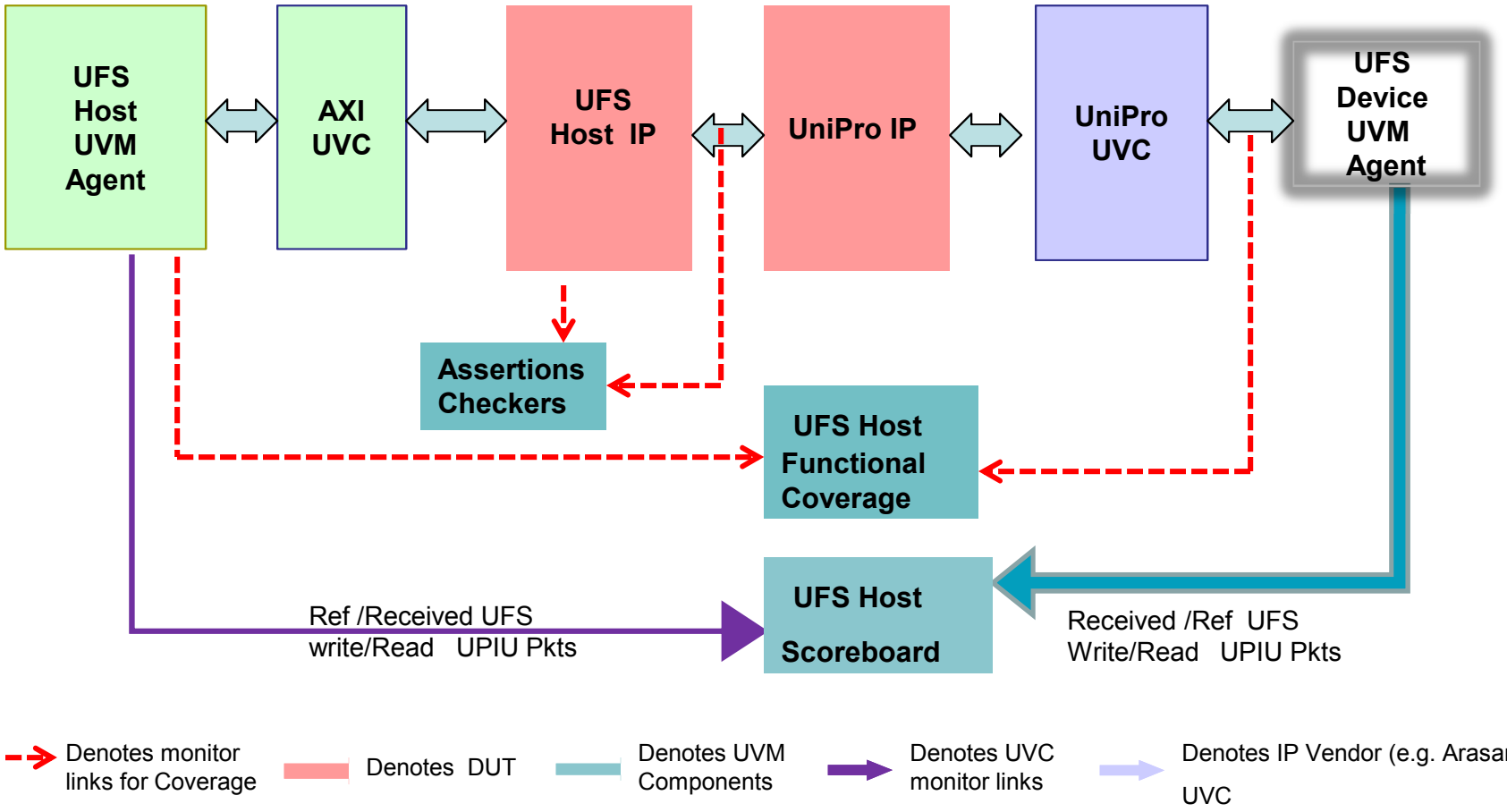


M-PHY Verification Before Silicon



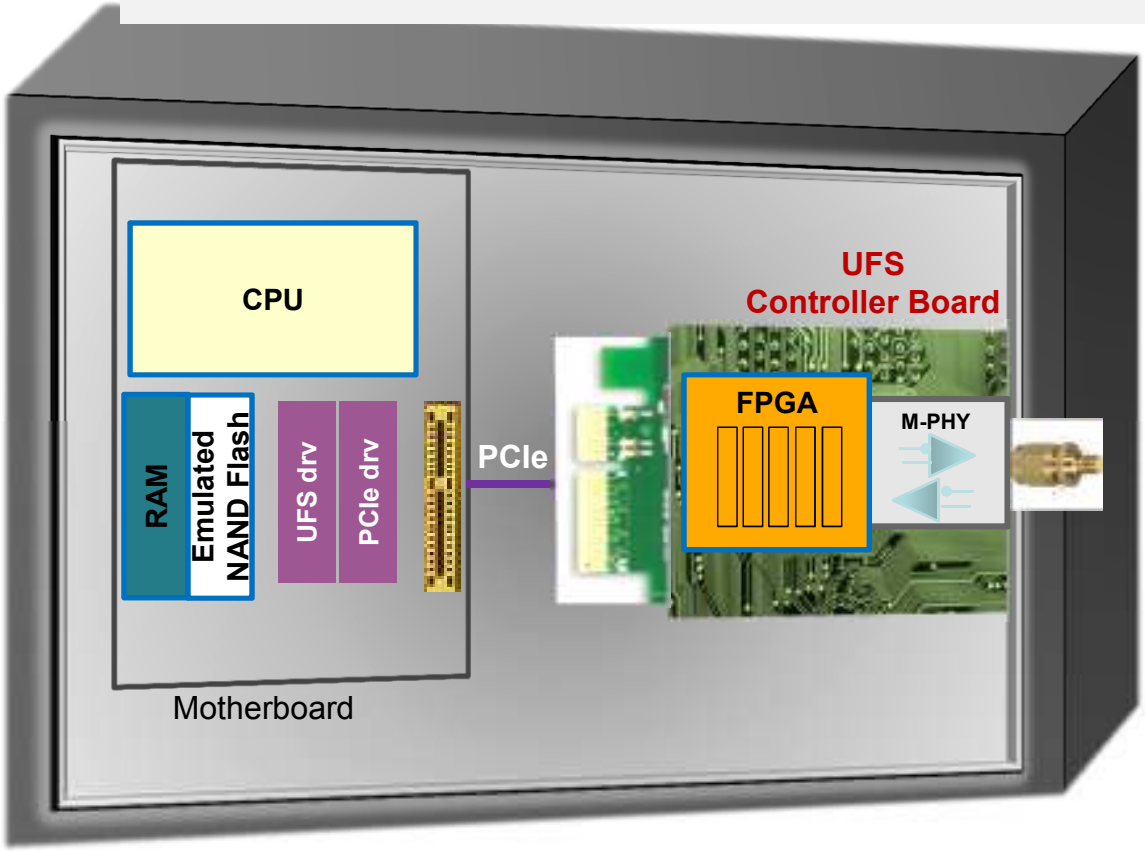
Verifying Complete UFS Before Silicon

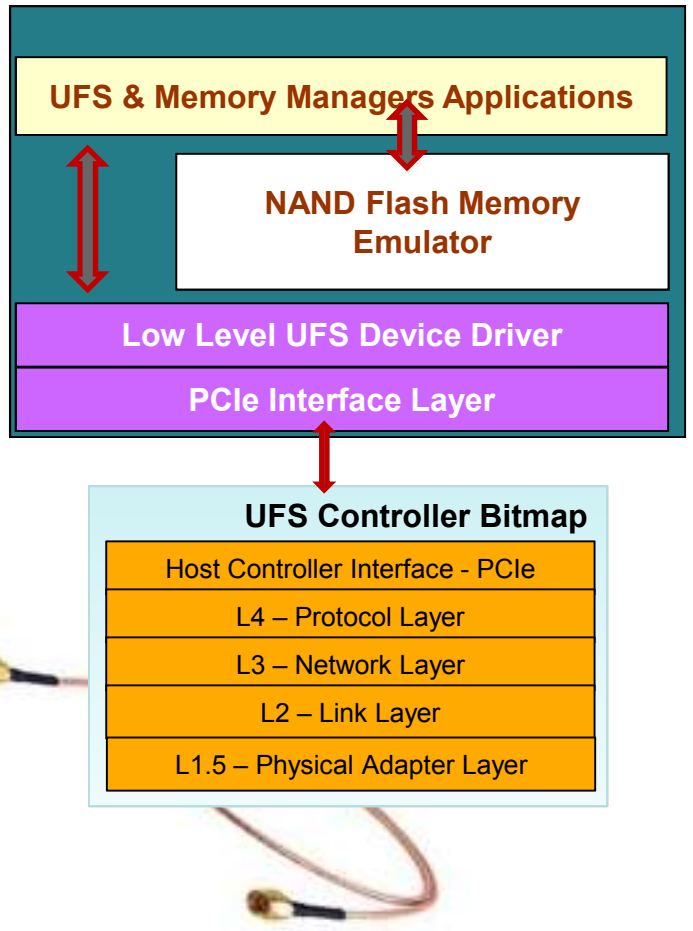
UFS-HCI + UniPro



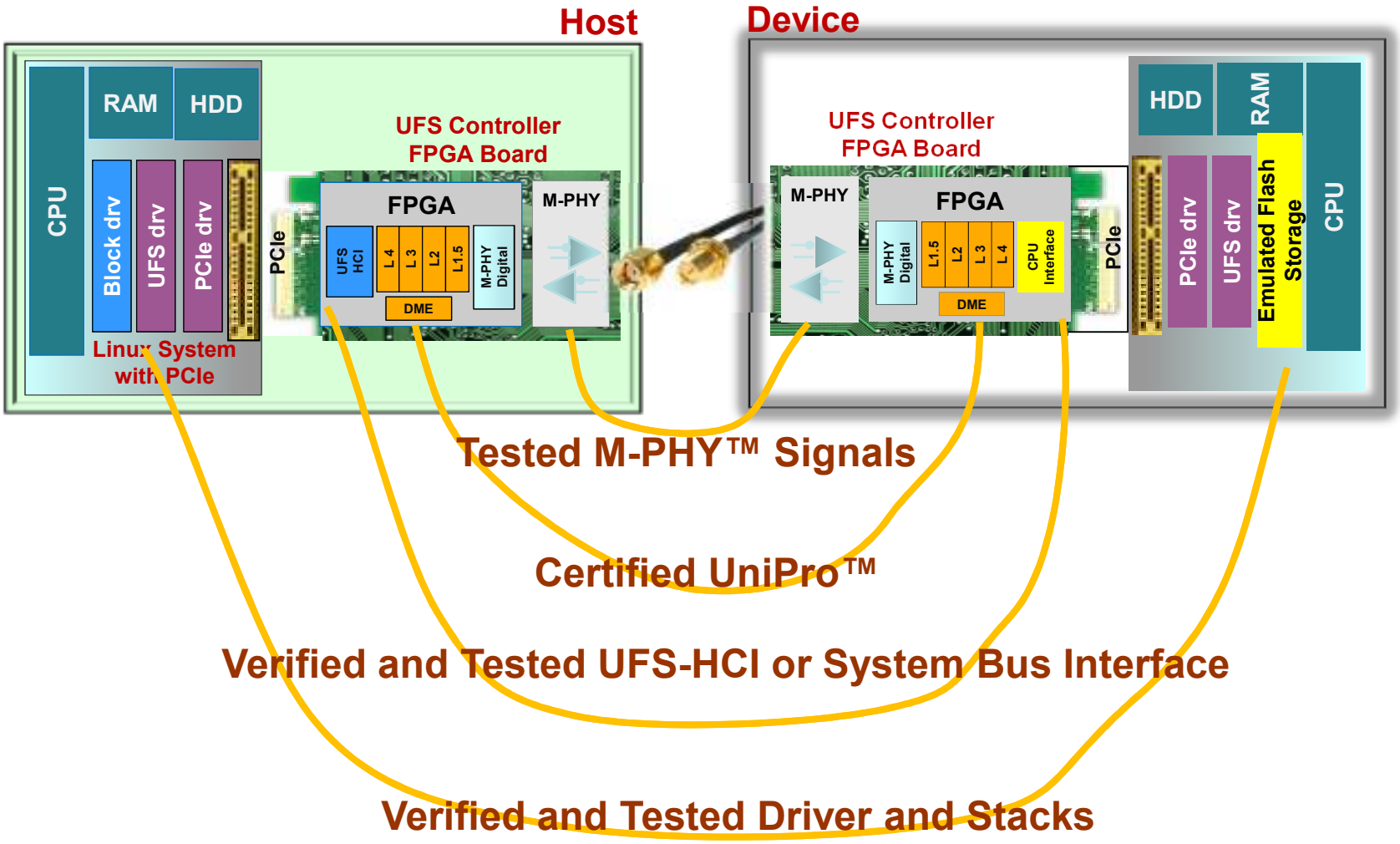
Migrate to FPGA based System

- A black-box approach enables quick access to a validation platform
- FPGA with Verified UFS IP





FPGA based System for Device Validation & Software Development



Enabling UFS/e.MMC Design Ecosystem

- FPGA based Development Platform productized into **Validation Platform**
  - IP, software stacks and PHY come together
- Used **by IP vendor** (eg. Arasan) for Interoperability testing with other pioneers
- Used **by Test & Measurement vendors** as target platforms
  - For validation of protocol generators and analyzers
- Ultimately used **by SoC/Device vendors** as target or reference platforms for silicon validation
  - Assured of IP interoperability, compliance, and backward compatibility

Summary

- **New JEDEC storage standards** continue to evolve for new markets
  - **Early IP/SoC validation** enables compliance and compatibility for fast time-to-market
- Different SoC vendors at **different stages of spec adoption**
  - Different spec revisions from different OEM's
  - **Backward compatibility** and **Interoperability** a must among vendors
- **IP vendors** continue to
  - **Leading the pack to invest** in transforming specs to RTL and GDSII
  - Keeping **Backward Compatibility** with older standards in new designs
  - Enabling **ecosystem-wide Inter-op** and **Compliance** through
    - Software stacks
    - Hardware Validation Platforms

All these are made available before starting your SoC/Device designs !!

Design for Compliance and Compatibility

THANK YOU