What Is Driving Advanced Packaging...

- Connected device proliferation
- Network expansion
- Increased compute and performance requirements
- Big Data Analytics
- Unique hardware configurations

Source: The Register, 5 May, 2014

Source: Intel
Why Advanced Packaging Matters…

- **Consistent Challenges and Opportunities**
  - Reduce power consumption
  - Improve performance
  - Enable more functionality
  - Reduce footprint
  - Control system costs

- **Advanced Packaging Influences**
  - New architectures
  - Increased BW and efficiency
  - Increased integration

- **Differentiates Products**
  - Performance increase
  - Functionality & Features

Source: IDC 2013
The Challenges

- Power consumption and hardware cost are nearly equal
- Memory increasing share of power
- Decreasing memory per core
- Technology scaling is slowing
Server Memory Requirements

Memory Bandwidth and Performance
- System performance
  Scales with Bandwidth, Latency, and Density

Power & Thermal
- System constraints w/ high bandwidth memory & capacity

Quality
- Ensure memory bits
- Long product life cycle
- High customer expectations

Cost and Time to Market
- Achieve lowest cost/bit
- Short time to market

Source: IBM, Inc. Flash Memory Summit 2013
Advanced Packaging Topics

- **NAND**
  - Wire bond die stacks

- **DRAM**
  - Wire bond die stacks
  - TSV die stacks

- **MCMs**
  - 2.5D interposers
  - 2.1D substrates

- Panel Level Packaging
- Chip on Chip Stacks
NAND PACKAGING ADVANCEMENTS FOR SSD
Packaging for SSDs

- SSDs improve data latency
- Thin die stacks <50um/layer
- Wire bond interconnect
- Increased storage density per package
- NAND process technology advancements continue
  - Packaging remains wire bond stacked die

Source: Yuan Xie, PSU
Roadmap for NAND WireBond Stacks

- Wire bond stacked die satisfies near/mid term density requirements
- TSV and Panel Level Packaging Only If Best Performance and Form-factor Required

Source: IBM, Flash Memory Summit
DRAM PACKAGING ADVANCEMENTS
DRAM Trends

- DRAM cell unchanged for 40 years
- DRAM scaling has Slowed
- DRAM per core is decreasing
DRAM Product Roadmap for Large Systems

Wire Bond Die Stacks
- DDR3 & DDR4
- FlipChip + WB

TSV Die Stacks
- DDR4
- 3DS
- TSV Die Stacks

Advanced DRAM
- HBM
- HMC
- Emerging Technology

Global Standards for the Microelectronics Industry
Large System DRAM TSV Memory Types

**DDR4-3DS**
- Existing Memory Architecture
- Evolutionary
- Bottom Die DRAM + Control
- Low TSV Count
- Loose TSV Pitch
- FCCSP-BGA Packaging
- 2 and 4 High Die Stacks
- DIMM Application
- Production Now

**HBM**
- New Memory Architecture
- Revolutionary
- Bottom Die Control Only
- High TSV Count
- Tight TSV Pitch
- WLCSP Packaging
- 5 and 9 High Die Stacks
- 2.5D Interposer Application for GPU
- Low volume manufacturing now

**HMC**
- New Memory Architecture
- Revolutionary
- Bottom Die Logic Control
- High TSV Count
- Tight TSV Pitch
- FC-BGA Packaging
- 5 and 9 High Die Stacks
- MCM and Board Mount for Networking
- LVM Now

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INTERPOSER PACKAGING TECHNOLOGY
2.5D Interposer & Advance Packaging
Product Roadmap

Silicon Partition
Logic + Memory
Emerging

Image Source: Xilinx

Image Source: Altera

Global Standards for the Microelectronics Industry
SOC to 2.5D TSV MCM SiP Migration

• **Focus Process Node Development on Specific Application Functionalities**
  - Reduces complexity and mask layer count of process node
  - Improves performance, power, and area of each application
  - Optimized process node for silicon function
  - Improves wafer yield
  - Reduces wafer cost

![Defect Density and Die Size](image)

**Image Source:** Xilinx

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**Global Standards for the Microelectronics Industry**

JEDEC®
2.5D Logic + Memory Integration

- Tightly couple logic & memory
- Efficient BW per energy consumed
- HBM Memory on TSV si interposer
- Advanced packaging

Image Source: nVidia
ADVANCED PACKAGING COMMERCIAL STATUS
TSV & Advanced Packaging
Commercialization Status

TSV Devices Are In Production!

- DDR4-3DS
- 2.5D Interposers
- HMC-3D
- HBM-3D
- Photonics 2.5D
- Panel FO/PLP
- Advanced MCM

Global Standards for the Microelectronics Industry
Thank You!
Top Trends in HPC

The global economy in HPC is growing again:

- 2010 grew by 10%, to reach $9.5 billion
- 2011 grew by 8.4% to reach $10.3 billion
- HPC revenue for 2012 exceeded $11B
- Q1 2013 -- The lower half of the market is growing well again
- We are forecasting ~7% growth over the next 5 years

Major challenges for datacenters:

- Power, cooling, real estate, system management
- Storage and data management continue to grow in importance

Software hurdles continue to grow

The worldwide Petascale Race is in full speed

Big Data and accelerators are hot new technologies

Data Movement Is Expensive:
In Energy and Time-to-Solution

Energy Consumption

- 1MW = $1 million
- Computing 1 calculation = 1 picowatt
- Moving 1 calculation = up to 100 picowatts

=> It can take 100 times more energy to move the results of a calculation than to perform the calculation in the first place.

Strategies

- Accelerate data movement (bandwidth, latency)

Reduce!

Minimize data movement (e.g., data reduction, in-memory compute, in-storage computation, etc.)

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