Design considerations for LPDDR4/3 PHY and controller sub system

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### Considerations for dual mode LPDDR3/4 designs

<table>
<thead>
<tr>
<th>Items</th>
<th>LPDDR4</th>
<th>LPDDR3</th>
<th>Comments</th>
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<tbody>
<tr>
<td>Channels per die</td>
<td>2</td>
<td>1</td>
<td></td>
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<tr>
<td>Data bus width/channel</td>
<td>16b</td>
<td>32b</td>
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<tr>
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<td>10b</td>
<td>2-tick CMD for LPDDR4</td>
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<tr>
<td>Max DQ data rate</td>
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How do controller and PHY switch from using two independent x16 command channels to a single x32 channel?
PoP PKG Ballout Comparison

What are the tradeoffs in PHY placement when a single SOC die needs to work for both ballouts?
LPDDR4/3 dual mode concept

- LPDDR4 (two channels, 32 byte access)
  - Can fully exploit parallelism in LPDDR4 device
- LPDDR3 (single channel, 32 byte access)
LPDDR4/3 dual mode concept

LPDDR4 mode (two channels, 32 byte access)

- Both controller queues in operation in x16 mode
- DFI mux disabled
- Inter PHY communication disabled
LPDDR4/3 dual mode concept
LPDDR3 mode (single channel, 32 byte access)

- Master CMD queue in 32 bit mode
- Other command queue disabled
- DFI mux active
- X16 bit PHY need inter communication (training)
Simpler LPDDR4/3 system

64 byte access size

- Systems with 64B minimum access size can implement a much simpler dual mode system
- **LPDDR4 mode**: Operate both channels in lock step, same command on both 64 byte access size
- **LPDDR3 mode**: Single channel, 64 or 32 byte access size
Simpler LPDDR4/3 system
64 byte access size

- MC always operates as single channel x32
- Command replication in LPDDR4 mode (Glue logic or phy_top)
- Passes thru in LPDDR3 mode
Simpler LPDDR4/3 system
64 byte access size

**Benefits**
- Single command queue – smaller MC
- Simpler MC-PHY communication
- Simple PHY with IO replication in LPDDR4 mode
- Suited for legacy systems moving to LPDDR4
Physical design implications with PoP and Discrete PKG

• PoP and discrete package ballout for LPDDR4 is quite different than that of LPDDR3
  – To allow single SoC design to support both LPDDR4 and LPDDR3, one must accept PKG routing complexity
  – Same SoC die with different package design is practical
  – Similar issues exist for supporting PoP and Discrete PKG from the same SoC design
LPDDR3 focused SoC PKG design

LPDDR3 focused physical design does not work for LPDDR4 POP!!
LPDDR4 focused SoC PKG design

- LPDDR4 optimized placement can work for LPDDR3
- Still need long routes in package and Soc for LPDDR3
- Per bit deskew capabilities in CA and DQ can be handy
Controller and PHY IP Techniques

- DRAM Controller and PHY IP may employ techniques to ease the burden and provide package/PCB routing flexibility for multi-mode
  - Per bit deskew on CA bus
  - CA bit swapping
  - Dual-mode (SDR and DDR) support for CA
Summary

• Command bus differences and POP/discrete package ballout differences make multi mode LPDDR3/4 challenging

• Optimization to system intent and capabilities can lead to practical implementations

• Cadence offers integrated LPDDR4 controller + PHY + memory models IP that address these issues