Next Big Thing: DDR4 3DS
Agenda

- Memory Requirement
- How to Address
- What’s 3DS
- It’s IN PRODUCTION
DRAM Market & Application

- 47% of DRAM for Server and PC application
Server Application Trend

- Memory RAS and Low TCO are required for server

**Server Virtualization**

- Operating voltage
- Stand-by power
- Core & I/O power

**Moving to Cloud**

- Better S/I
- Reinforced resiliency

**Big Data**

- High bandwidth
- Better efficiency

Source: Gartner('14.1Q)
High Capacity  
High Performance/Watt  
High Reliability  
But Low Cost
4th Generation of DDR SDRAM

- Successor of DDR3 from 2014 supporting all Computing system
**TSV technology for 3DS**

- Enables DRAM stacking with better electrical characteristics

**Conventional Stack Solutions**

- **<QDP Wire-bond Package>**
  - RDL*
  - Wire-Bond

- **<QDP LRDIMM>**
  - Number of loading limits high speed operations

**TSV Solutions**

- **<4H TSV Package>**
  - Slave Chip
  - Master Chip
  - TSV VIA

- **<3DS TSV RDIMM>**
  - Only master chip communicates with controller regardless of number of stacking

*RDL: Re-distribution Layer
3DS DDR4 Architecture

- Mater, sub-control of CA/CTL/Data

(a) address path

(b) data path
3DS DDR4 Architecture

- Micrograph of 3DS DDR4 SDRAM
  - (a) Chip Micrograph
  - (b) Vertical section
  - (c) Shmoo
Check List for 3DS (1)

- Encoded Address: 1CS# + 2Chip ID

Increase Max Density with Limited CS#
Check List for 3DS (2)

- Additional Latency for De-Skew PVT

<table>
<thead>
<tr>
<th>Speed Bin</th>
<th>DDR4-2133P-3DS2A (Optional)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CL-nRCD-nRP</td>
<td>17-15-15</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>min</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal read command to first data</td>
<td>tAA</td>
<td>15.92</td>
<td>21.00</td>
</tr>
<tr>
<td>ACT to internal read or write delay time</td>
<td>tRCD</td>
<td>14.05</td>
<td>-</td>
</tr>
<tr>
<td>PRE command period</td>
<td>tRP</td>
<td>14.05</td>
<td>-</td>
</tr>
<tr>
<td>(tRCD)</td>
<td></td>
<td>(13.7517)</td>
<td></td>
</tr>
<tr>
<td>ACT to PRE command period</td>
<td>tRAS</td>
<td>33</td>
<td>9 x tREFI</td>
</tr>
<tr>
<td>ACT to ACT or REF command period</td>
<td>tRC</td>
<td>47.06</td>
<td>-</td>
</tr>
</tbody>
</table>

Better Matching with RDIMM rather than LRDIMM

Global Standards for the Microelectronics Industry
Check List for 3DS (3)

- MR Setting only for Master

<table>
<thead>
<tr>
<th>DRAM Command</th>
<th>CS_n</th>
<th>C2</th>
<th>C1</th>
<th>C0</th>
<th>Logical Rank0</th>
<th>Logical Rank1</th>
<th>Logical Rank2</th>
<th>Logical Rank3</th>
<th>Logical Rank4</th>
<th>Logical Rank5</th>
<th>Logical Rank6</th>
<th>Logical Rank7</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode Register Set</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>MRS</td>
<td>1, 2</td>
</tr>
<tr>
<td>Mode Register Set</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>2</td>
</tr>
<tr>
<td>Any other command</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>DES</td>
<td>2</td>
</tr>
</tbody>
</table>

- All Logical Ranks enter Self Refresh / Power Down together

<table>
<thead>
<tr>
<th>DRAM Command</th>
<th>CS_n</th>
<th>C2</th>
<th>C1</th>
<th>C0</th>
<th>Logical Rank0</th>
<th>Logical Rank1</th>
<th>Logical Rank2</th>
<th>Logical Rank3</th>
<th>Logical Rank4</th>
<th>Logical Rank5</th>
<th>Logical Rank6</th>
<th>Logical Rank7</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Refresh (REF)</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>SRE</td>
<td>1, 2</td>
</tr>
<tr>
<td>Refresh (REF)</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>1, 2</td>
</tr>
<tr>
<td>NOP</td>
<td>L</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>1, 2</td>
</tr>
<tr>
<td>Any command</td>
<td>H</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>PDE</td>
<td>1, 2</td>
</tr>
</tbody>
</table>

Simpler Initialization / Power control
Check List for 3DS (4)

- Staggering Refresh only within Logical Ranks

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Logical Rank Density</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>4Gb</td>
<td>8Gb</td>
</tr>
<tr>
<td>REF command to ACT or REF command time to same logical rank</td>
<td>tRFC_srl1 (1X mode)</td>
<td>260</td>
<td>350</td>
</tr>
<tr>
<td></td>
<td>tRFC_srl2 (2X mode)</td>
<td>160</td>
<td>260</td>
</tr>
<tr>
<td></td>
<td>tRFC_srl4 (4X mode)</td>
<td>110</td>
<td>160</td>
</tr>
<tr>
<td>REF command to REF command to different logical rank</td>
<td>tRFC_drl1 (1X mode)</td>
<td>90</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>tRFC_drl2 (2X mode)</td>
<td>55</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td>tRFC_drl4 (4X mode)</td>
<td>40</td>
<td>55</td>
</tr>
</tbody>
</table>

No Difference in Package Rank Interleaving
Tips to maximize 3DS performance

- Make Sure your controller support All-Ranks Interleaving
  - Can Maximize Efficiency if you control PKG Ranks and Logical Ranks in the different way

- Use 3DS only at Same Channel

- Reduce Staggering Refresh Interval
Power Efficiency of 3DS Solution

- 3DS solution shows similar performance to buffered solutions
- Significant less power by removing additional ICs

*Performance: SPECjbb benchmark, Latency: ATE, Power: Samsung memory stress PGM @ system

3DS RDIMM performs the same as buffered solutions

4H 3DS DRAM consumes same as conventional 2stack
Performance Benchmark

• 3DS RDIMM shows better overall performance
  – 3DS RDIMM shows best performance with 2DPC (less idle time from large number of ranks)
  – 3DS RDIMM 1DPC performance is similar to DDP LRDIMM (larger idle time from more refresh)
Unveiled 1st TSV product, 64GB RDIMM

- 64GB RDIMM with TSV is IN PRODUCTION
Infrastructure Readiness for HBM

300mm wafer process line is ready for “Mass Production”

Fab process qualification is completed with “State of the art” facilities