Advanced Package Solutions & Its Challenges for Mobile and IoT/Wearable Devices

Presented by Albert Lan

SPIL
14/Mar-2016
What’s the **Next New Technology to change the world** in the Near Future???

IoT?  Wearable devices?  Smart City?...

*Let’s have detail market trend analysis & discussion further...*
Market Trend & Industry Benchmark

KEY Innovative Package Solutions
- SiP Module
- Finger Print
- High Band Width PoP
- Fan-Out WLP
- 3D-IC
- Molded WLCSP

Summary
 Outline

◆ Market Trend & Industry Benchmark

◆ KEY Innovative Package Solutions
  ✓ SiP Module
  ✓ Finger Print
  ✓ High Band Width PoP
  ✓ Fan-Out WLP
  ✓ 3D-IC
  ✓ Molded WLCSP

◆ Summary
Consumer Electronic Product Market Trend (CAGR)

1. IoT / Wearable Device
   
   (35.8% → 39.3% / 58.5% → 55.8%)

2. SMART Phone/Tablet
   
   (12.9% → 9.7% / 19.3% → 1.6%)

3. Networking
   
   (6%)

4. Automotive
   
   (2.7%)

=> Let’s focus on above “Four” High CAGR area for further direction discussion...
Electronics Market Trends

PC → NB → Mobile Phone → IoT

Huge volume from 2020

Source: Morgan Stanley Research; IEK'2014
Mobile Phone is going for several KEY features, including **longer battery life**, **better performance with more functions**, and **small form factors (thinner)**, but **low cost**. → It bring a lot of package & technology challenges !!!
Wearable Devices + IoT + Wireless + Apps + Web Service = Future
Outline

- Market Trend & Industry Benchmark
- **KEY Innovative Package Solutions**
  - SiP Module
  - Finger Print
  - High Band Width PoP
  - Fan-Out WLP
  - 3D-IC
  - Molded WLCSP
- Summary
<table>
<thead>
<tr>
<th>Product Application</th>
<th>2015~2017 PKG Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IoT &amp; Wearable Devices</strong></td>
<td><strong>SiP Module</strong></td>
</tr>
<tr>
<td>Connectivity</td>
<td>Antenna in SiP</td>
</tr>
<tr>
<td>MCU</td>
<td>EMI-SiP (partition shielding)</td>
</tr>
<tr>
<td>Memory</td>
<td>SiP (Stack Die on Passives)</td>
</tr>
<tr>
<td>MEMS</td>
<td></td>
</tr>
<tr>
<td><strong>SMART Phone/Tablet PC</strong></td>
<td><strong>Finger Print</strong></td>
</tr>
<tr>
<td>Application Processor;</td>
<td>Finger Print Module(LGA)</td>
</tr>
<tr>
<td>Baseband;</td>
<td>FPS (Ceramic/Glass type)</td>
</tr>
<tr>
<td>Connectivity</td>
<td>LSD-FCCSP</td>
</tr>
<tr>
<td>PMIC</td>
<td>Stacked Die-LGA</td>
</tr>
<tr>
<td>PA</td>
<td></td>
</tr>
<tr>
<td><strong>Package on Package</strong></td>
<td><strong>Fan-Out WLP</strong></td>
</tr>
<tr>
<td>BD-PoP</td>
<td>FO-Single Die</td>
</tr>
<tr>
<td>ePoP</td>
<td>FO-MCM</td>
</tr>
<tr>
<td><strong>3D-IC</strong></td>
<td>2.5DIC</td>
</tr>
<tr>
<td>IC Interposer</td>
<td>2.5DIC NTI (No TSV Interposer)</td>
</tr>
<tr>
<td>Substrate</td>
<td></td>
</tr>
<tr>
<td><strong>Molded WLCSP</strong></td>
<td><strong>mWLCSP</strong></td>
</tr>
<tr>
<td>mWLCSP</td>
<td>mWLCSP w/BSL</td>
</tr>
</tbody>
</table>

Available  On-going  Candidate
### Product Application

**IoT & Wearable Devices**
- Connectivity
- MCU
- Memory
- MEMS

**SMART Phone/Tablet PC**
- Application Processor
- Baseband
- Connectivity
- PMIC
- PA

### 2015~2017 PKG Roadmap

<table>
<thead>
<tr>
<th>SiP Module</th>
<th>2015~2017 PKG Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anenna in SiP</td>
<td>EMI-SiP (partition shielding)</td>
</tr>
<tr>
<td>SiP (Stack Die on Passives)</td>
<td></td>
</tr>
</tbody>
</table>

#### Finger Print
- Finger Print Module (LGA)
- FPS (Ceramic/Glass type)
- LSD-FCCSP
- Stacked Die-LGA

#### Package on Package
- BD-PoP
- ePoP
- HBW PoP

#### Fan-Out WLP
- FO-Single Die
- FO-MCM
- FO-PoP

#### 3D-IC
- 2.5DIC
- 2.5DIC NTI (No TSV Interposer)

#### Molded WLCSP
- mWLCSP
- mWLCSP w/BSL
## Electronic Products Integration Trend

<table>
<thead>
<tr>
<th>Year</th>
<th>~2000</th>
<th>2010</th>
<th>2015</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Main Stream Products</strong></td>
<td>PC / Notebook</td>
<td>Mobile Phone / Tablet</td>
<td>IoT / Wearables</td>
</tr>
<tr>
<td><strong>Market Features</strong></td>
<td>Feature: Standard Platform, High Volume Customer: Brand Name OEMs</td>
<td>Feature: High Matrix, Low Volume Customer: Many new customers in various application market</td>
<td></td>
</tr>
<tr>
<td><strong>Integration Trends</strong></td>
<td>SoC / PCBA</td>
<td>SoC / SiP</td>
<td>SiP / PCBA / SoC</td>
</tr>
<tr>
<td><strong>SiP Opportunity</strong></td>
<td>Camera, Finger Print, Wireless Connectivity</td>
<td>• <strong>Sensor Related</strong> SiP (Camera, Finger Print)</td>
<td>Wireless Connectivity, PMIC, Sensor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <strong>Analog Based</strong> SiP (Connectivity, Analog, PMIC, PA/LNA)</td>
<td></td>
</tr>
<tr>
<td><strong>Remark</strong></td>
<td>• SoC plays major role on function integration</td>
<td>• Modulize is a trend and SiP plays more important role in this high matrix market</td>
<td>• SiP is only adopted in high end smart phone.</td>
</tr>
</tbody>
</table>
Typical Wearable Device Function Block

1. **MCU**: Micro Controller, usually ARM base, MCU instead of AP
2. **Sensors**: Temp, Vibration, Gyroscope, Moisture, Pressure, Altitude...
3. **Power Management**: High integration on Active + Passives
4. **Memory**: Flash, NVM, SRAM
5. **Wireless, Connectivity**: WiFi, BLE

**IC / SiP Design Requirement for IoT market:**

=> Low Cost + Great Performance + Low Power + Easy design-In = **Low Entry Barrier**
Total Solution: Direct Package to SiP

1. **Wafer Bumping**
   - Characterization
   - Reliability validation
   - Footprint arrangement
   - RDL
   - Bump mask design

2. **Chip/Package Design**
   - Probe card design
   - Test program optimization

3. **Wafer Sort**
   - FOC/Repsv/RLD
   - WLCSP

4. **Module Assembly**
   - System Level Design
   - Schematic/layout design
   - Package/process design

5. **SiP Module & Package Co-Design**
   - SMT
   - D/W Bond
   - Molding
   - EMI Coating

6. **Function Test**
   - Test System Setup
   - Socket / change EVB design
   - Test program Development

7. **Drop Ship**
   - IDM/Wafers/Foundry
Design Simulation for Wearables

Simulation

Thermal
- Critical Thermal
- Temperature Contour
  Flotherm
  ANSYS

Stress
- Max. Warpage
- Solder Fatigue Life
- Mold Flow
  ANSYS
  LS-DYNA

Electrical
- S Parameter
- Signal/Power Integrity
- EMI Simulation
- Antenna Simulation
  HFSS, Power SI
  HSPICE, ADS
  Q3D, TPA

11a/b/g/n MIMO + BT4.0 SiP Module

11b/g + BT SiP Module

EMI, Antenna
Why **Fingerprint** Technology?

- **FP Main function is to ID identification for password alternative solution**
# Industrial FP Sensor Package Type Benchmarking

## Principle

<table>
<thead>
<tr>
<th>Passive Capacitive</th>
<th>Active Capacitive</th>
<th>Ultrasonic Sensor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Finger</strong></td>
<td><strong>Array of Electrodes</strong></td>
<td><strong>Cross section of finger skin</strong></td>
</tr>
<tr>
<td><strong>WB-LGA</strong></td>
<td><strong>SiP</strong></td>
<td><strong>Chip On Flex</strong></td>
</tr>
</tbody>
</table>

## Package Type

- **Passive Capacitive**: WB-LGA
- **Active Capacitive**: SiP, FCCSP
- **Ultrasonic Sensor**: Chip On Flex
New Approach Idea for Finger Print Module?

Finger Touch!!

Idea!!

Land Side Cap Approach

Land Side Die Approach

Similar/maturity process
KEY Innovative Advanced Packaging Technology Roadmap

Product Application

IoT & Wearable Devices
- Connectivity
- MCU
- Memory
- MEMS

IoT & Wearable Devices
- Connectivity
- MCU
- Memory
- MEMS

SMART Phone/ Tablet PC
- Application Processor;
- Baseband;
- Connectivity
- PMIC
- PA

2015~2017 PKG Roadmap

SiP Module
- Antenna in SiP
- EMI-SiP (partition shielding)
- SiP (Stack-Die on Passives)

Finger Print
- Finger Print Module(LGA)
- FPS(Ceramic/Glass type)
- LSD-FCCSP
- Stacked Die-LGA

Package on Package
- BD-PoP
- ePoP
- HBW PoP

Fan-Out WLP
- FO-Single Die
- FO-MCM
- FO-PoP

3D-IC
- 2.5DIC
- 2.5DIC NTI (No TSV Interposer)

Molded WLCSP
- mWLCSP
- mWLCSP w/BSL

Available On-going Candidate
HBW-PoP-CB (Cu Ball) Evolution Trend

0.4mm Top Ball Pitch

Increase Interconnect IO

0.27mm Top Ball Pitch

Benefit:
1. High IO Interconnection
2. High Performance Approach
Benefit:
1. High IO Interconnection
2. High Performance Approach
Why Fan-out Technology?

Why Fan-Out

- Keep sufficient area for PCB board I/O as the die size shrinking (28/20/16/14nm...)
- Thin PKG due to eliminate substrate
- Solution for small die but medium I/O wafer level package

Feature

- Small form factor with medium I/O
- Reconstituted wafer & RDL processing
- Substrate-less by 1L~2L RDL instead
- Multi chips & passives integration
- Bridging technology for embedded 3D or 3D stacking
**Application:**
Keep sufficient area for PCB board I/O as the die size shrinking (28/20/16nm), application for Mobile AP/ Baseband/ PMIC and HDD/SSD Controller.

**Benefit:**
- Small form factor & thinner package (substrate-less).
- High IO/High bandwidth with fine line/multi-layer RDL routability.
  
  \( \text{Line/Space} = <10\text{um}, >2\text{L RDL layer} \)

\[ \text{FO-WLP} = \text{Recon.} + \text{RDL} + \text{Assembly} \]

1. Temporary adhesive
2. D/B
3. Encapsulation
4. Carrier/ De-carrier
## Product Map for FO & Its Alternatives

<table>
<thead>
<tr>
<th>Group</th>
<th>RDL L/S(um)</th>
<th>PKG Solution</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>0.1</td>
<td>FO-MCM</td>
<td>High-End Application: 1. High performance computing 2. Networking 3. Data servers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Silicon Interposer</td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>2</td>
<td>FO-PoP</td>
<td>Mobile Application: 1. Smart Phone &amp; Tablet 2. High End AP/BB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HBW-PoP</td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>&gt;10</td>
<td>FO-SD</td>
<td>Low Pin Count Application: (PMIC/RF/PA...)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FC-ETS</td>
<td></td>
</tr>
</tbody>
</table>

- **SPIL develops own Fan-out technology & identify the product map:**
  - **Group 1 (High-End Application):** endorsed Silicon Interposer / Spilt Die FO-MCM FCBGA.
  - **Group 2 (Mobile Application):** drive FO-PoP / HBW-PoP solution.
  - **Group 3 (Low Pin Count Application):** drive FO-Single Die / FC-ETS solution.
All key enabling technologies been well established
- **Package level TCT 1000X & uHAST 96hrs & HTSL 1000hrs** PASS
- **Board level TCT 1\textsuperscript{st} failure > 500X & Drop 30X** PASS
# 12” FO-SD PLR Reliability Update

<table>
<thead>
<tr>
<th>TEST LEVEL</th>
<th>POD</th>
<th>TEST ITEM</th>
<th>CONDITION</th>
<th>SAMPLE SIZE</th>
<th>DEFECT RATE</th>
<th>SAT</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>PACAKGE LEVEL</td>
<td>0.75/0.65mm</td>
<td>PRECON</td>
<td>Soak: 85°C/85%RH, 168hrs (MSL1) Reflow: 260+5/-0°C * 3cycle</td>
<td>90</td>
<td>0/90 pcs</td>
<td>0/10</td>
<td>PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HTSL</td>
<td>150 (-0/+10°C), 500 Hours</td>
<td>45</td>
<td>0/45 pcs</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HTSL</td>
<td>150 (-0/+10°C), 1000 Hours</td>
<td>45</td>
<td>0/45 pcs</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>uHAST</td>
<td>130 ± 2°C, 85± 5% RH, 33.3psia 168hr</td>
<td>45</td>
<td>0/45 pcs</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCB 500 CYCLE</td>
<td>-55 °C ~ 125 °C, 500 cycles</td>
<td>45</td>
<td>0/45 pcs</td>
<td>0/5</td>
<td>PASS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCB 1000 CYCLE</td>
<td>-55 °C ~ 125 °C, 1000 cycles</td>
<td>45</td>
<td>0/45 pcs</td>
<td>0/5</td>
<td>PASS</td>
</tr>
</tbody>
</table>

- **0.65mm package total height: PLR L1/260C TCB1000 Passed.**
- **0.75mm package total height: PLR L1/260C TCB1000 Passed.**
KEY Innovative Advanced Packaging Technology Roadmap

<table>
<thead>
<tr>
<th>Product Application</th>
<th>2015~2017 PKG Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IoT &amp; Wearable Devices</strong></td>
<td>SiP Module</td>
</tr>
<tr>
<td>- Connectivity</td>
<td>Antenna in SiP</td>
</tr>
<tr>
<td>- MCU</td>
<td>EMI-SiP (partition shielding)</td>
</tr>
<tr>
<td>- Memory</td>
<td>SiP (Stack Die on Passives)</td>
</tr>
<tr>
<td>- MEMS</td>
<td></td>
</tr>
<tr>
<td><strong>SMART Phone/ Tablet PC</strong></td>
<td>Finger Print</td>
</tr>
<tr>
<td>- Application Processor;</td>
<td>Finger Print Module(LGA)</td>
</tr>
<tr>
<td>- Baseband;</td>
<td>FPS(Ceramic/Glass type)</td>
</tr>
<tr>
<td>- Connectivity</td>
<td>LSD-FCCSP</td>
</tr>
<tr>
<td>- PMIC</td>
<td>Stacked Die-LGA</td>
</tr>
<tr>
<td>- PA</td>
<td></td>
</tr>
<tr>
<td><strong>Package on Package</strong></td>
<td>Fan-Out WLP</td>
</tr>
<tr>
<td>- BD-PoP</td>
<td>FO-Single Die</td>
</tr>
<tr>
<td>- ePoP</td>
<td>FO-MCM</td>
</tr>
<tr>
<td>- HBW-PoP</td>
<td>FO-PoP</td>
</tr>
<tr>
<td><strong>3D-IC</strong></td>
<td></td>
</tr>
<tr>
<td>- 2.5DIC NTI</td>
<td>2.5DIC NTI (No TSV Interposer)</td>
</tr>
<tr>
<td>- Molded WLCSP</td>
<td>mWLCSP</td>
</tr>
<tr>
<td>- mWLCSP w/BSL</td>
<td></td>
</tr>
</tbody>
</table>

Available On-going Candidate
2.5DIC is available solution for FPGA/GPU/CPU/Networking products.

NTI (Non-TSV Interconnection) is a known FO-MCM solution to fulfill Ultra High Density Interconnection requirement in multi-chip structure.
All key enabling technologies been well developed in SPIL
NTI -1 (with 4 layer RDLs by Fab. and Substrate)

- PKG size $45 \times 45 \text{mm}^2$
- NTI size $30.8 \times 24.8 \text{ mm}^2$
- ASIC Bump Pitch $= 45 \text{ um}$

- Integrated 4 layers of Cu done by IC fab with 0.4um line width
- Thinnest interconnection with highest density.
Si removal - Si wet etch and stop on oxide layer

- Oxide Surface
- Wafer BS status after Si removal

Contact Open - Oxide layer dry etch

- Contact Open (M1)
- Oxide Surface

Via Last contact open to M1 without oxide residue
**KEY Innovative Advanced Packaging Technology Roadmap**

<table>
<thead>
<tr>
<th>Product Application</th>
<th>2015~2017 PKG Roadmap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IoT &amp; Wearable Devices</strong></td>
<td>SiP Module</td>
</tr>
<tr>
<td>▶ Connectivity</td>
<td>Antenna in SiP</td>
</tr>
<tr>
<td>▶ MCU</td>
<td>EMI-SiP (partition shielding)</td>
</tr>
<tr>
<td>▶ Memory</td>
<td>SiP (Stack-Die on Passives)</td>
</tr>
<tr>
<td>▶ MEMS</td>
<td></td>
</tr>
<tr>
<td><strong>SMART Phone/ Tablet PC</strong></td>
<td></td>
</tr>
<tr>
<td>▶ Application Processor;</td>
<td>Finger Print</td>
</tr>
<tr>
<td>▶ Baseband;</td>
<td>Finger Print Module(LGA)</td>
</tr>
<tr>
<td>▶ Connectivity</td>
<td>FPS(Ceramic/Glass type)</td>
</tr>
<tr>
<td>▶ PMIC</td>
<td>LSD-FCCSP</td>
</tr>
<tr>
<td>▶ PA</td>
<td>Stacked Die-LGA</td>
</tr>
<tr>
<td><strong>Package on Package</strong></td>
<td></td>
</tr>
<tr>
<td>▶ BD-PoP</td>
<td>Package on Package</td>
</tr>
<tr>
<td>▶ ePoP</td>
<td></td>
</tr>
<tr>
<td>▶ HBW-PoP</td>
<td></td>
</tr>
<tr>
<td><strong>Fan-Out WLP</strong></td>
<td></td>
</tr>
<tr>
<td>▶ FO-Single Die</td>
<td></td>
</tr>
<tr>
<td>▶ FO-MCM</td>
<td></td>
</tr>
<tr>
<td>▶ FO-PoP</td>
<td></td>
</tr>
<tr>
<td><strong>3D-IC</strong></td>
<td></td>
</tr>
<tr>
<td>▶ 2.5DIC</td>
<td></td>
</tr>
<tr>
<td>▶ 2.5DIC NTI (no TSV Interposer)</td>
<td></td>
</tr>
<tr>
<td>▶ LSD-Interposer</td>
<td></td>
</tr>
<tr>
<td>▶ LSD-FCCSP</td>
<td></td>
</tr>
<tr>
<td>▶ Stacked Die-LGA</td>
<td></td>
</tr>
<tr>
<td>▶ Finger Print Module(LGA)</td>
<td></td>
</tr>
<tr>
<td>▶ FPS(Ceramic/Glass type)</td>
<td></td>
</tr>
<tr>
<td>▶ LSD-FCCSP</td>
<td></td>
</tr>
<tr>
<td>▶ Stacked Die-LGA</td>
<td></td>
</tr>
<tr>
<td>▶ Finger Print Module(LGA)</td>
<td></td>
</tr>
<tr>
<td>▶ FPS(Ceramic/Glass type)</td>
<td></td>
</tr>
<tr>
<td>▶ LSD-FCCSP</td>
<td></td>
</tr>
<tr>
<td>▶ Stacked Die-LGA</td>
<td></td>
</tr>
</tbody>
</table>

**Available** | **On-going** | **Candidate**
Background of WLCSP Dicing Defect Mode

Blade Saw found side wall crack (SWC)

Sidewall crack check by FIB

Side wall crack
New Idea Solution for WLCSP SWC Prevention

1. Stealth dicing
2. Dicing Before Laser
3. Plasma Etching

Process Enhancement

New Idea!!??

4. Wafer From Molding WLCSP
5. Strip From Molding WLCSP
6. FOWLP (SD)
7. FC-MISBGA (1L)

=> Will detail discuss on “item 4 → Molding WLCSP” in below separated page.
**mWLCSP (Molded WLCSP) Technology**

- **Merits of mWLCSP (Molded WLCSP)**
  - Solution for 5S/6S protection on WLCSP devices.
  - Utilize wafer sort to screen out potential issue unit.
  - Potential board level reliability enhancement.
**mWLCSP (Molded WLCSP) Technology - 5S**

- **Left Side of Die**
- **mWLCSP X-section**
- **Right Side of Die**

- **Chip level TCT 1000X & uHAST 96hrs & HTSL 1000hrs** **PASS**
- **Board level TCT 1000X & Drop 30X** **PASS**
**mWLCSP (Molded WLCSP) Technology - 6S**

**MT-WLCSP X-section**

1. Ball height
2. Side wall thickness
3. Molding thickness
4. Total molding thickness
5. BSL thickness
6. Expose ball height
Outline

- **Market Trend & Industry Benchmark**
- **KEY Innovative Package Solutions**
  - SiP Module
  - Finger Print
  - High Band Width PoP
  - Fan-Out WLP
  - 3D-IC
  - Molded WLCSP
- **Summary**
Smart phone & Tablet devices are big volume growth, but observe wearable & IoT devices (w/ connectivity functions) will become a mainstream in the near-term future.

**Future Assembly Trend:**
SiP / Finger Print / HBW PoP / Fan-Out / 2.5D IC / Molded WLCSP
Thank You For Your Attention!!!

Albert Lan

albertlan@spil.com.tw