Flash Technology: 200-400Mbps and Beyond

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NAND Flash Primer (1/2)

- NAND requires Erase before Programming
  - Erase
  - Program
NAND Flash Primer (2/2)

- NAND Flash is page-based for Read & Program Operation
  - The internal data register holds one page of data
  - A Page is the unit of transfer between the data register and the memory array. All program and read operations transfer a page of data between the data register and a page in the memory array.
NAND Interface Evolution (~200Mbps)

- As performance requirements increase, the legacy NAND interface (SDR—single data rate) becomes bottleneck, esp. for read performance.
- JEDEC NAND Flash I/F specification is scheduled to be ratified by early 2011

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<thead>
<tr>
<th></th>
<th>Legacy SDR (~66Mbps)</th>
<th>Toggle-mode DDR (~200Mbps)</th>
<th>Synchronous DDR (~200Mbps)</th>
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<td>Dout</td>
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</tbody>
</table>

Supported interface is identified by Read ID
Growing Need for Higher NAND I/F Speed

- Conventional NAND Flash memory application
  - High capacity (low cost), small form factor & low power consumption
    - Common in most CE devices

- New CE devices
  - High performance
    - Full browsing
    - 3D gaming

- System performance devices
  - High-performance computing
  - Massive data processing
Growing Need for Higher NAND I/F Speed

• Performance demand with the growth of storage interface
• With continuing innovations in such as the NAND architecture and enhanced I/O speed, performance can be achieved.
Introducing High-Speed NAND Flash Interface

• New features to enable 400 Mbps
  – Complementary DQS and RE signals
  – Vref (SSTL)
  – On Die Termination
  – DQS latency adjustment

Note: Features are under discussion and subject to change without notice.
Differential Signaling

- Independent enablement of RE and DQS
- Immunity to GND Noise and Cross Talk

<table>
<thead>
<tr>
<th>Legacy SDR</th>
<th>DDR (Toggle/Sync)</th>
<th>High-Speed DDR</th>
<th>Type</th>
<th>Description</th>
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<th>ALE</th>
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<th>WE#</th>
<th>WP#</th>
<th>R/ B#</th>
<th>DQS</th>
<th>DQ[0:7]</th>
<th>Toggle DDR NAND</th>
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</table>

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<th>DQ[0:7]</th>
<th>Toggle DDR 400 NAND</th>
</tr>
</thead>
</table>

- DQ DQ DQ I/O Data Input/Output
- DQS DQS I/O Data Strobe
- /DQS I/O Data Strobe Complement
- RE I Read Enable Complement
- Vpp I External High Voltage
- Vref I Voltage Reference

Note: Features are under discussion and subject to change without notice.
Vref

- **SSTL**
  - 400 Mbps only supported at 1.8V VccQ
  - Industry standard that is easily adaptable
  - Allows for higher speeds and lower power consumption

- **External Vref**
  - VccQ/2
  - Allows for tighter setups/holds due to controlled reference
  - Reduces effects from external GND bounce

Note: Features are under discussion and subject to change without notice.
On Die Termination

- Once ODT is enabled by Set Feature, no other operation by host required.
- For example, if program command is issued, ODT is turned on only during data transfer period.

Note: Features are under discussion and subject to change without notice.
High-Speed Interface Simulation with On Die termination

Test Condition
1. $C_{in} : 3.5\,\text{pF/Die}$
2. Host $C_{in} : 8\,\text{pF}$
3. PKG Cap: $2.03\,\text{pF}$
4. $V_{ccQ} : 1.8\,\text{V}$
5. Transmission Line: $50\,\text{ohm}$ (X-talk included)
6. Termination: $100\,\Omega$
7. Freq: $400\,\text{Mbps}(200\,\text{MHz})$
Write Operation without ODT

Ron=18Ω
77.6% UI (1.94n)

Ron=25Ω
75.2% UI (1.88n)

Ron=35Ω
68.4% UI (1.71n)

Ron=50Ω
52.0% UI (1.3n)
Write Operation with ODT

- **Ron=18Ω**
  - 87.6% UI
  - (2.19n)

- **Ron=25Ω**
  - 85.2% UI
  - (2.13n)

- **Ron=35Ω**
  - 81.6% UI
  - (2.04n)

- **Ron=50Ω**
  - 76.0% UI
  - (1.9n)
Latency DQS Cycle

- Pre-toggles of DQS until valid DQS is stabilized
  - Appropriate duty ratio can be obtained
  - Latency provided for current specification is from zero to 4 cycles.
  - Latency DQS Cycle can be programmed for Data In and Data Out respectively.

Note: Features are under discussion and subject to change without notice.
External Vpp for NAND

- Using external power supply reduces current consumption for Program/Read operation
  - On-chip charge pumps have relatively low power efficiency (<30%)
  - In server SSD applications, high voltage source is provided.
  - If NAND can utilize these high voltage source, overall SSD power efficiency can be lowered. (no staggered program operation)

**Parameter** | **Symbol** | **Min** | **Typ.** | **Max** | **Unit**
--- | --- | --- | --- | --- | ---
External Vpp | Vpp | 11.5 | 12 | 12.5 | V

*Functional Block Diagram*

Note: Features are under discussion and subject to change without notice.
Features Enable/Disable

• New signals and functions can be enabled selectively
  – Features introduced with High-Speed I/F for NAND flash will be available to be enabled or disabled with Feature address 02h.

Note: Features are under discussion and subject to change without notice.
Backward Compatibility

- High-Speed NAND Flash supports backward compatibility
  - New signals and functions are user-selective
  - Set feature command is used for changing interface

- ONFi-JEDEC Joint Task Group collaborating to provide a single, industry standard, high-speed NAND interface with backward compatibility.
Join JEDEC for early access to the spec

- For an early and close look at the spec or contribution to standard, please join JEDEC or contact your NAND suppliers
Thank You