JEDEC STANDARD

Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits

JESD8C.01

(Minor Revision of JESD8C, June 2006)

SEPTEMBER 2007

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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INTERFACE STANDARD FOR NOMINAL 3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS CONTENTS

Contents

INTERFACE STANDARD FOR NOMINAL 3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

(From JEDEC Board Ballot JCB-98-120, and JCB-05-76, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard (a replacement of JEDEC Standards 8, 8-1, 8-1A, and 8B) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3 V/3.3 V and driving/driven by parts of the same family. Clause 2 describes normal DC electrical characteristics and clause 2.4 (added by revision C) describes the optional characteristics for Schmitt trigger operation. The specifications in this standard represent a minimum set, or 'base line' set, of interface specifications for LVTTL compatible and LVCMOS compatible circuits.

Conversion to this standard will not occur at any specific time. Instead, manufacturers forced to reduce operating voltages for any of the reasons summarized in clause 4 should convert to this 'base line' standard as a basis for their designs to ensure compatibility in a nominal 3 V/3.3 V power supply environment.

The purpose is to develop a standard of specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design.

2 Standard specifications

All voltages listed are referenced to ground (0 V) except where noted.

2.1 Absolute maximum ratings (Notes 1 & 2)

Supply Voltage: V_{DD}.....-0.5 V to 4.6 V
DC input Voltage: V_I .....-0.5 V to V_{DD} + 0.5 V (≤ 4.6 V max.)
DC Output Voltage: V_O .....-0.5 V to V_{DD} + 0.5 V (≤ 4.6 V max.)
DC Input Current: I_I at $V_I < 0$ V or $V_I > V_{DD}$ .....±20 mA
DC Output Current I_O at $V_O < 0$ V or $V_O > V_{DD}$ .....±20 mA

NOTE 1 Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the operational sections of this standard is not implied.

NOTE 2 I_I is for any single input and I_O is for any single output.

2 Standard specifications (cont'd)

2.2 Recommended operating conditions

Table 1 — Recommended operating conditions

Power supply range	Symbol	Narrow Range	Normal Range	Extended Range
Nominal supply voltage	V_{DD}	3.3 V	3.3 V	3.0 V
Power supply voltage	V_{DD}	3.15 V to 3.45 V	3.0 V to 3.6 V	2.7 V to 3.6 V
Operating temperature	T_A	See Note	See Note	See Note

NOTE As specified by manufacturer to be Commercial, Industrial and/or Military grade.

2.3 DC electrical characteristics

All specifications in the following tables apply across the operating temperature range.

Table 2 — LVTTL & LVCMOS input specifications

Symbol	Parameter	Test condition (note 1)	MIN	MAX	Units
V_{IH}	Input High Voltage	$V_{OUT} >= V_{OH\ (min)}$ or $V_{OUT} \leq V_{OL\ (max)}$	2	V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or $V_{IN} = V_{DD}$ (Note 2)		±5	µA
3.0 V nominal supply: $V_{DD\ (min)}$ = 2.7 V and $V_{DD\ (max)}$ = 3.6 V 3.3 V nominal supply: $V_{DD\ (min)}$ = 3.0 V and $V_{DD\ (max)}$ = 3.6 V 3.3 V nominal supply: $V_{DD\ (min)}$ = 3.15 V and $V_{DD\ (max)}$ = 3.45 V					

NOTE 1 For conditions shown as 'min or 'max', use the appropriate value shown in Tables 3 and 4.

NOTE 2 Excluding common Input/Output terminals.

Table 3 — LVTTL output specifications

Symbol	Parameter	Test condition	MIN	MAX	Units
V_{OH}	Output High Voltage	V_{DD} = min, I_{OH} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	V_{DD} = min, I_{OL} = 2 mA		0.4	V
3.3 V nominal supply: $V_{DD\ (min)}$ = 3.0 V and $V_{DD\ (max)}$ = 3.6 V 3.3 V nominal supply: $V_{DD\ (min)}$ = 3.15 V and $V_{DD\ (max)}$ = 3.45 V					

2 Standard specifications (cont'd)

2.3 DC electrical characteristics (cont'd)

Table 4 — LVCMOS output specifications

Symbol	Parameter	Test condition	MIN	MAX	Units
V_{OH}	Output High Voltage	V_{DD} = min, I_{OH} = -100 µA	V_{DD} - 0.2		V
V_{OL}	Output Low Voltage	V_{DD} = min, I_{OL} = 100 µA		0.2	V
3.0 V nominal supply: $V_{DD\,(min)}$ = 2.7 V and $V_{DD\,(max)}$ = 3.6 V 3.3 V nominal supply: $V_{DD\,(min)}$ = 3.0 V and $V_{DD\,(max)}$ = 3.6 V 3.3 V nominal supply: $V_{DD\,(min)}$ = 3.15 V and $V_{DD\,(max)}$ = 3.45 V					

2.4 Optional DC electrical characteristics for Schmitt trigger operation

2.4.1 Optional Schmitt trigger operation - Normal range

Table 5 — Input/Output Specification [$V_{DD\,(min)}$ = 3.0 V and $V_{DD\,(max)}$ = 3.6 V]

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{DD}	Supply Voltage	---	3.0	3.6	V
Vt+ (Vp)	Positive Going Threshold Voltage	$V_{OUT} \geq V_{OH\,(min)}$	0.9	2.1	V
Vt- (Vn)	Negative Going Threshold Voltage	$V_{OUT} \leq V_{OL\,(max)}$	0.7	1.9	V
Vh (ΔVt)	Hysteresis Voltage	Vt+ - Vt-	0.2	1.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA I_{OH} = -2 mA	V_{DD}-0.2 2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA I_{OL} = 2 mA		0.2 0.4	V

NOTE 1 V_{DD} of the sending and receiving devices must track within 0.1V to maintain adequate dc margins.

NOTE 2 For Vt+ (Vp) and Vt- (Vn), V_{DD} refers to the receiving device. For V_{OH} and V_{OL}, V_{DD} refers to the sending device.

NOTE 3 Operating temperature range as specified by manufacturer to be Commercial, Industrial and/or Military.

2.4 Optional DC electrical characteristics for Schmitt trigger operation (cont'd)

2.4.2 Optional Schmitt trigger operation – Extended range

Table 6 — Input/Output Specification [$V_{DD\ (min)}$ = 2.7 V and $V_{DD\ (max)}$ = 3.6 V]

Symbol	Parameter	Test Condition	MIN	MAX	Unit
V_{DD}	Supply Voltage	---	2.7	3.6	V
Vt+ (Vp)	Positive Going Threshold Voltage	$V_{OUT} \geq V_{OH\ (min)}$	0.9	2.1	V
Vt- (Vn)	Negative Going Threshold Voltage	$V_{OUT} \leq V_{OL\ (max)}$	0.7	1.9	V
Vh (ΔVt)	Hysteresis Voltage	Vt+ - Vt-	0.2	1.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{DD}-0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA		0.2	V

NOTE 1 V_{DD} of the sending and receiving devices must track within 0.1V to maintain adequate dc margins.

NOTE 2 For Vt+ (Vp) and Vt- (Vn), V_{DD} refers to the receiving device. For V_{OH} and V_{OL}, V_{DD} refers to the sending device.

NOTE 3 Operating temperature range as specified by manufacturer to be Commercial, Industrial and/or Military.

3 Test conditions for optional Schmitt trigger operation

3.1 Positive Going Threshold Voltage: Vt+ (Vp)

As the input signal is raised from a ground level in the measurement circuit shown in Figure 1, the input voltage value at which the output logic changed is determined as Vt+ (Vp).

3.2 Negative Going Threshold Voltage: Vt- (Vn)

As the input signal is dropped from a power supply voltage level in the measurement circuit shown in Figure 1, the input voltage value at which the output logic changed is determined as Vt- (Vn).

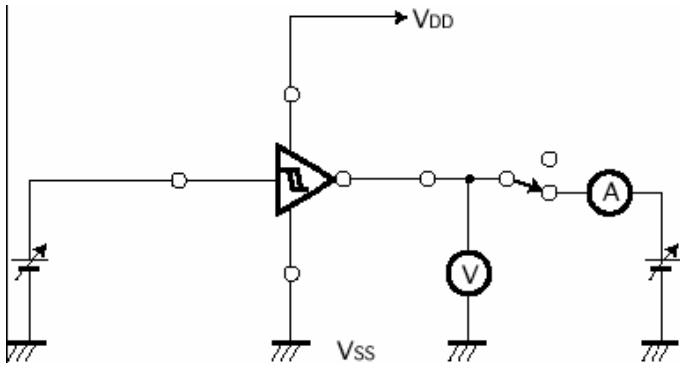

Figure 1 — DC characteristic measurement circuit of Schmitt trigger input

4 Background

4.1 Requirements of scaling

To obtain better performance and higher density, semiconductor technologists are reducing the vertical and horizontal dimensions of integrated device structures. If constant supply voltages and interface levels are maintained, on-chip electric fields will increase and higher system level slew rates will lead to increased electromagnetic interference and device-induced noise such as ground bounce. Additionally, with increasing numbers of on-chip functions, on-chip power dissipation may increase. All these factors - increased electric fields, electromagnetic interference, device-induced noise and power dissipation - lead to reduced reliability at the chip and system level. Thus, to continue the semiconductor scaling trend, a reduction of chip power supply voltage will be required. This JEDEC Standard will ease the transition from the existing 5 V ± 10% TTL standard by achieving agreement among the manufacturers and users.

4.2 LVTTL compatibility

One justification for revising JEDEC Standard Nos. 8 and 8-1 is to maintain TTL compatibility with adequate noise margins. In addition, this standard is intended for components at all levels of integration. This will include memories, microprocessors, peripherals, standard logic functions, gate arrays, and programmable logic circuits. No preference for any implementation technology is implied.

Table 3 is intended to be 'LVTTL-compatible' in the sense that the output logic 1 (V_{OH}) and output logic 0 (V_{OL}) levels have been specified at the same voltage levels that have been commonly recognized as logic 1 and logic 0 in the 5-V environment. Devices that meet the specifications in Tables 2 and 3 can generally be expected to drive 5-V "TTL-compatible" components. However, while 5-V "TTL-compatible" components should be able to meet the minimum input logic switching levels (V_{IH} and V_{IL}) of compounds that meet this standard, the logic-1 output voltage of many 5-V compendiums will exceed the maximum input voltage of a Standard 8C compliant device. Depending on the technology and circuit implementation, the 5-V "TTL-compatible" components may drive their outputs anywhere from about 3 V to the V_{DD} supply level into a high-impedance load.

CAUTION: Before connecting a 5-V component to a 3-V or 3.3-V component, always check to be sure that the maximum V_{OH} of the 5-V device does not exceed the specified V_{IH} maximum of the 3-V or 3.3-V device under the anticipated operating conditions.

4 Background (cont'd)

4.3 LVCMOS compatibility

Components designed to meet the output requirement described in Table 4 of this standard are said to be "LVCMOS-compatible" because they are required to swing rail to rail under light dc load conditions in the manner commonly expected of "CMOS I/O" components. This feature facilitates the design of systems for minimum static power consumption.

In regard to CMOS input compatibility, Standard No. 8C components can also be said to be "CMOS-compatible" because:

1) The minimum V_{IH} for Standard 8C components is 2 V over the operating voltage range. Under the worst-case conditions for V_{IH}, i.e., at V_{DD} = max, a V_{IH} of 2 V is lower than the traditional CMOS V_{IH} of 0.7 x V_{DD}. The minimum guaranteed logic-1-level noise margin is 0.5 V (2.7 V -0.2 V -2.0 V) over the extended power supply range, 0.8 V (3.0 V -0.2 V -2.0 V) over the normal supply range, and 0.95 V (3.15 V -0.2 V -2.0 V) over the narrow supply range.

2) The maximum V_{IL} for components in this document is 0.8 V. Under the worst-case conditions for V_{IL}, i.e., at V_{DD} = min, a V_{IL} of 0.8 V is higher than the traditional CMOS V_{IL} of 0.2 x V_{DD}. The minimum guaranteed logic-0-level noise margin is 0.6 V (0.8 V -0.2 V) over the power supply ranges.

Therefore in all cases, Standard 8C compliant components exceed the traditional "CMOS I/O "logic level requirements.

4.4 Meeting Standard 8C requirements

Components that meet the requirements of this standard shall meet the input specifications described in Table 2. Components are "LVTTL-compatible" if they meet the output specifications described in Table 3. Components are "LVCMOS-compatible" if they meet the output specifications described in Table 4. A component manufacturer may specify a device that meets both output specifications described in Tables 3 and 4.

4.5 Exceeding Standard 8C requirements

Components may be specified in such a way as to exceed the requirements set forth in this standard. Such components may be said to "meet or exceed the requirements of JEDEC Standard No. 8C".

EXAMPLES

1 A component manufacturer of a 3.3-V device may specify a device to tolerate a 12-V signal as a logic high input, exceeding the Table 1 requirement that a 3.3-V device operate with V_{IH} (max) of V_{DD} + 0.3 V.

2 A 3.3-V device may be specified to meet the Table 3 output logic levels while driving a considerably heavier 20-mA load, thus exceeding the minimum 2-mA output drive current requirement.

Annex A Differences between JESD8C.01 and JESD8C

This table briefly describes changes that appear in this standard, JESD8C.01, compared to its predecessor, JESD8C (June 2006). These changes were approved at the March, 2007 meeting of the JC-16 committee.

Page	Description of change
3	Table 5 in Section 2.4.1 was updated to change four values that were incorrectly listed as fractions of VDD (min values of Vt+, Vt-, Vh, and V_{OH}) to instead be values in V (Volts).
4	Table 6 in Section 2.4.2 was updated to correct three values that were incorrectly listed as fractions of VDD (min values of Vt+, Vt-, and Vh) to instead be values in V (Volts).

Annex A.1 Differences between JESD8C and JESD8B

This table briefly describes most of the changes made to entries that appear in this standard, JESD8C, compared to its predecessor, JESD8B (September 1999). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description of change
All	Document renumbered to be consistent with the JEDEC Style Manual, JM7
2	Table 2, for consistency with other JESD8-series documents, the following were renamed: "High-level Input Voltage" to "Input High Voltage", and "Low-level Input Voltage" to "Input Low Voltage".
2 & 3	Tables 3 & 4, for consistency with other JESD8-series documents, the following were renamed: "High-Level Ouput Voltage" to "Output High Voltage", and "Low-Level Ouput Voltage" to "Output Low Voltage.
4	New section added for: Test conditions for optional Schmitt trigger operation.

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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☐ Other _____

2. Recommendations for correction:

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3. Other suggestions for document improvement:

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