Total IP Solution for Mobile Storage
UFS & NAND Controllers

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Arasan Chip Systems
San Jose, CA

Mobile Forum Taiwan & Korea 2012
Fast Growing NAND Storage Markets

Source: Gartner

CAGR (2012 – 2014)
Mobile Storage Keeps Growing

Global eMMC Memory Shipment Forecast (Millions)

Source: IHS iSuppli Research June 2011

Taiwan & Korea 8/2012
MIPI Adoption Driven by Smart Mobile

MIPI – Mobile Industry Processor Interface Alliance; The standard body defining M-PHY & UniPro adopted by JEDEC UFS
UFS Integrated with MIPI protocols
Using same M-PHY and UniPro® specs
Why UFS?

- JEDEC standard (JES220)
- Leverage and **Reuse** Existing Standards
  - MIPI Architecture – UniPro, M-PHY
  - SCSI Command Sets
- Serial Interface Rx / Tx - SoC **Lower Pin Count**
- **High Bandwidth** Migration Path for eMMC - 1.5/3/6 Gbps
- **Lower Power** for Mobile Applications
Mobile SoC Support Multiple Storage Interfaces and Backward Compatibility

SD
- SD 1.0
- SD 1.1 High speed
- SD 2.0 High capacity
- SDIO 1.0
- SDIO 2.0 50Mhz
- SDIO 3.0 UHS-I
- SDIO 3.0 UHS-I
- SDIO 4.0 UHS II 1.56Gbps

eMMC / UFS
- MMC 4.1 High speed
- MMC 4.2 High Capacity
- eMMC 4.3 Boot-up
- eMMC 4.41 DDR
- eMMC 4.5 HS200 200MB/s
- UFS 1.1 3Gbps

USB
- USB 1.0 12 Mbps
- USB 2.0 480 Mbps
- USB 3.0 5 Gbps

NAND
- ONFi 1.0 50 MB/s
- ONFi 2.x 150 MB/s DDR
- ONFi 3.0 400MB/s DDR

Timeline:
- 1994
- 2000
- 2004
- 2005
- 2006
- 2007
- 2008
- 2009
- 2010
- 2011
- 2012
1. **Complexity of Integration**
   a) Physical Layer Analog Interface
   b) Controller Digital Design
   c) Controller Firmware and OS Software Drivers
   d) OS File Systems & Stacks

2. **Compliance**
   - Meet specifications

3. **Compatibility**
   - Comprehensive Interoperability

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**Total Solution Supporting Mobile Storage**

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**JEDEC**

*Global Standards for the Microelectronics Industry*
UFS Mobile Storage Implementation

UFS Host

ARM Core

AMBA Interface

AXI, AHB, etc

Controller IP Core

M-PHY

HCI

UFS Device

Controller IP Core

M-PHY

Ax, AHB, etc

NAND

Reset

Ref Clock

Dout+/- Din+/-

Din+/- Dout+/-
Layered Architecture

- UFS-SCSI Command Set Layer (UCS)
- UFS Transport Protocol Layer (UTP)
- UFS InterConnect Layer (UIC)
- UniPro
- M-PHY

L4 = Transport
L3 = Network
L2 = Data Link
L1.5 = PHY adapt
L1 = M-PHY

UFS Controller IP Core
UFS M-PHY
UniPro® Ensures Data Integrity

Application Data - Message

L4 – Segment

Header

L3 – Packet

Dest. CPort

Dest. Device

L2 – Frame

Data

17b symbol

L1.5 – symbol

17b symbol

L1 – symbol

8b10b symbol

Tx / Rx Pair

Global Standards for the Microelectronics Industry
UFS Controller with Certified UniPro®
M-PHY Type 1 Key Features for UFS (con’t)

- HS Gear 1, 2, 3
- LS PWM Gear 0-7
- Configurable up to 4 lanes
- Ref clock - 19.2 / 26 / 38.4 / 52 MHz

<table>
<thead>
<tr>
<th>Gear</th>
<th>Rate A Mbps</th>
<th>Rate B Mbps</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.25</td>
<td>1.5</td>
<td>Mandatory</td>
</tr>
<tr>
<td>2</td>
<td>2.5</td>
<td>3</td>
<td>Optional</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>5.8</td>
<td>Optional</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Gear</th>
<th>Bit Rate Mbps</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>below Gear 1</td>
<td>not supported</td>
</tr>
<tr>
<td>1</td>
<td>3 to 9</td>
<td>Mandatory</td>
</tr>
<tr>
<td>2</td>
<td>6 to 18</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>12 to 36</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>24 to 72</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>48 to 144</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>96 to 288</td>
<td>Optional</td>
</tr>
<tr>
<td>7</td>
<td>192 to 576</td>
<td></td>
</tr>
</tbody>
</table>

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M-PHY Type 1 Key Features for UFS

• Differential Serial Interfaces
  – Type 1 M-PHY
    • High Speed NRZ Signaling
    • Low Speed PWM Signaling
  – Up to 4 Lanes

• Power Savings

<table>
<thead>
<tr>
<th>Power States</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stall</td>
<td>HS-Mode power saving state; Allows fast recovery time</td>
</tr>
<tr>
<td>Sleep</td>
<td>LS-Mode power saving state;</td>
</tr>
<tr>
<td>Hibern8</td>
<td>Ultra Low Power State; Configuration still intact</td>
</tr>
<tr>
<td>Disabled</td>
<td>Disabled by Reset; Configuration reset to default</td>
</tr>
<tr>
<td>Unpowered</td>
<td>Power Supply Removed</td>
</tr>
</tbody>
</table>
M-PHY for UFS Implementation

- **1** Synchronization
- **2** Type-1: HS & LS Mode
- **3** Power Saving
- **4** Data Integrity
- **5** Coding for NRZ & PWM
High Performance NAND for UFS Device
## NAND Flash Interface Evolution

<table>
<thead>
<tr>
<th></th>
<th>JEDEC</th>
<th>Proprietary</th>
<th>JEDEC/ONFI</th>
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</thead>
<tbody>
<tr>
<td><strong>Legacy SDR</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pinout</td>
<td>WE#</td>
<td>RE#</td>
<td>CK</td>
</tr>
<tr>
<td></td>
<td>DQ</td>
<td></td>
<td>DQ</td>
</tr>
<tr>
<td><strong>Toggle-mode DDR</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Writes</td>
<td>WE#</td>
<td>RE#</td>
<td>CK</td>
</tr>
<tr>
<td></td>
<td>DQS</td>
<td></td>
<td>W/R#</td>
</tr>
<tr>
<td></td>
<td>Din</td>
<td></td>
<td>DQ</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DQS</td>
</tr>
<tr>
<td>Reads</td>
<td>RE#</td>
<td>DQS</td>
<td>CK</td>
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<td></td>
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<td></td>
<td>W/R#</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DQS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DQ</td>
</tr>
</tbody>
</table>

Source: JEDEC 2010
# ONFI Interface 2.x, 3.0

<table>
<thead>
<tr>
<th>Feature</th>
<th>ONFI 2.0 SDR</th>
<th>ONFI 2.3 NV-DDR</th>
<th>ONFI 3.0 NV-DDR2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Speed</td>
<td>Mode 5 (20ns)</td>
<td>200 MT/s (100Mhz)</td>
<td>400 MT/s (200Mhz)</td>
</tr>
<tr>
<td>CE_n Pin Reduction</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Volume Addressing</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>On-die termination (ODT)</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Differential Signaling</td>
<td>No</td>
<td>No</td>
<td>Yes, optional for DQS and/or RE_n</td>
</tr>
<tr>
<td>I/O VccQ</td>
<td>3.3V / 1.8V</td>
<td>3.3V / 1.8V</td>
<td>1.8V</td>
</tr>
<tr>
<td>External VREFQ</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Versatile NAND Flash Controller IP

NAND Controller IP includes:
- ONFI NV-DDR2 PHY, Toggle DDR 1/2, Legacy SDR
- ECC engine
- ARM interface – AMBA (AXI, AHB)
Challenge of Designing for 400MT/s

Process, Voltage, and Temperature (PVT) lead to clock misalignment.

A synthesized solution cannot meet the 2.5ns DDR data period.

**A hard IP DLL or Delay Circuit** is required to ensure the clock edge is aligned to the center of data for correct sampling.

Clock misaligned due to PVT variations.
Optimized ONFI 3.0 PHY

1. DLL Circuit
   - More accurate than typical delay circuit
   - Allows designer to align and optimize for data sampling;
   - Smaller die size and lower power consumption

2. 2X clock into Tx generates more accurate sampling clock

3. ONFI 3.0 compliant I/O pad
   - 1.8v / 3.3v dual voltage (not a typical DDR pad)
Dynamically Configurable ECC Engine

1. Modular design expandable to 32-bit or more ECC capability
2. Match different ECC requirements for different NAND ICs

High Performance:
Parallel bit processing on BCH encoder

BCH Decoder:
Inversion-less Berlekamp-Massey algorithm for Key Equation Solver
Parallel computation for Key Equation Solver using parallel Chien search algorithm

Low Latency:
Parallel syndrome generation on BCH decoder
UFS / NAND Total IP Solution

Companion Software Stacks

Certified Digital IP Core

InterOperable Analog PHY

IP & Software Validation Platform

UFS Host & Device

UFS-SCSI Command Set Layer (UCS)

UFS Transport Protocol Layer (UTP)

UniPro

L4 = Transport

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THANK YOU