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Global Standards for the Microelectronics Industry

Understanding The New Bit Error Rate DRAM Timing Specifications

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Server Memory Forum 2011

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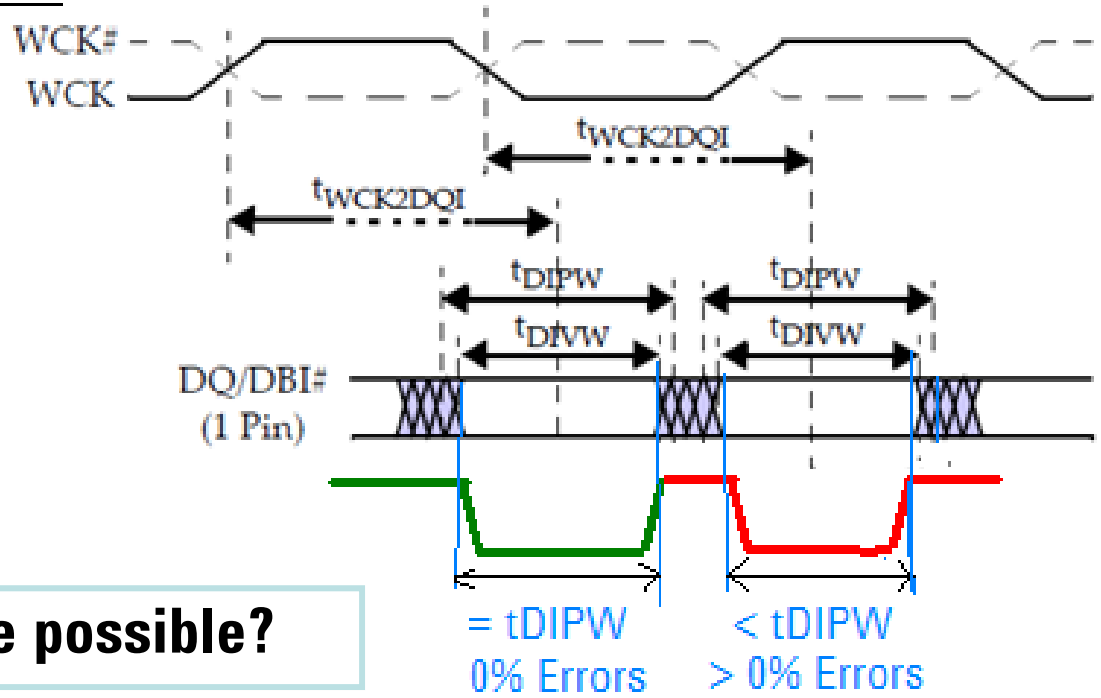
Examining Memory Timing

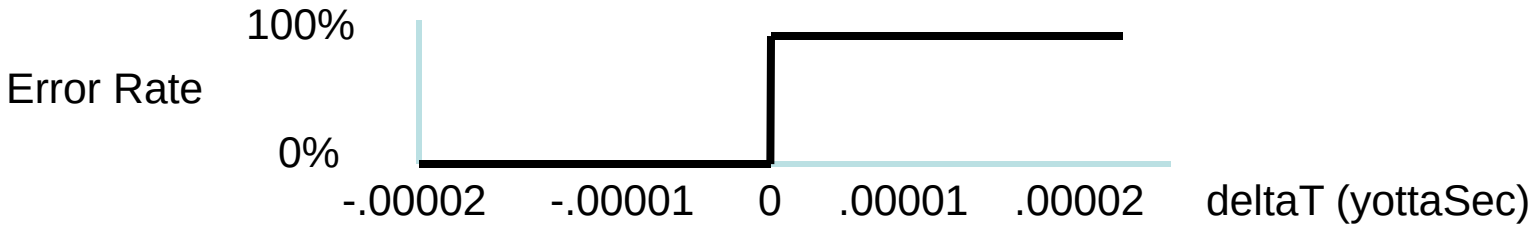
- Data rates are 32x faster while AC timing spec structure is unchanged
- Memory timing specs based on increasingly risky assumptions
  - DQs using Ts/Th or tDIPW assume perfect data capture if the spec is met
  - Clocks specify a total jitter constraint over a small number of cycles
- Random jitter now a significant part of the UI, has not been specified
  - Total jitter is underestimated as well
- Result –> <u>not enough timing margin to go around</u>
  - Overly aggressive component specs -> decreased yield
  - Reliance on “hidden” margin -> System reliability at risk
  - Overly conservative designs -> Later to market, more expensive
- A new set of assumptions and way to specify timings is needed

Traditional Data Transfer Spec

Assumes that meeting Ts/Th, tDIPW/tDIVW, tDYNOFF <u>guarantees</u> zero errors:



Can this be possible?



Why Is This A Problem?

At low speeds it's NOT a problem

Rj is a small enough fraction of UI that it can be ignored

N-Cycle Tj BER Limit

System Reliability Requirement (on each DQ)

Only small amount of margin needed (as fraction of UI) to yield BER << needed rate

Conservative Spec.

Optimal Specification

Worst case simulation

Best case simulation

Impact on binning and yields is small

N-Cycle Tj Works at Low Speeds

A small "guard band" -> stable system at lower speeds

N-Cycle Tj BER Limit

System Reliability Requirement (on each DQ)

Optimal Requirement (BER = 1e-15)

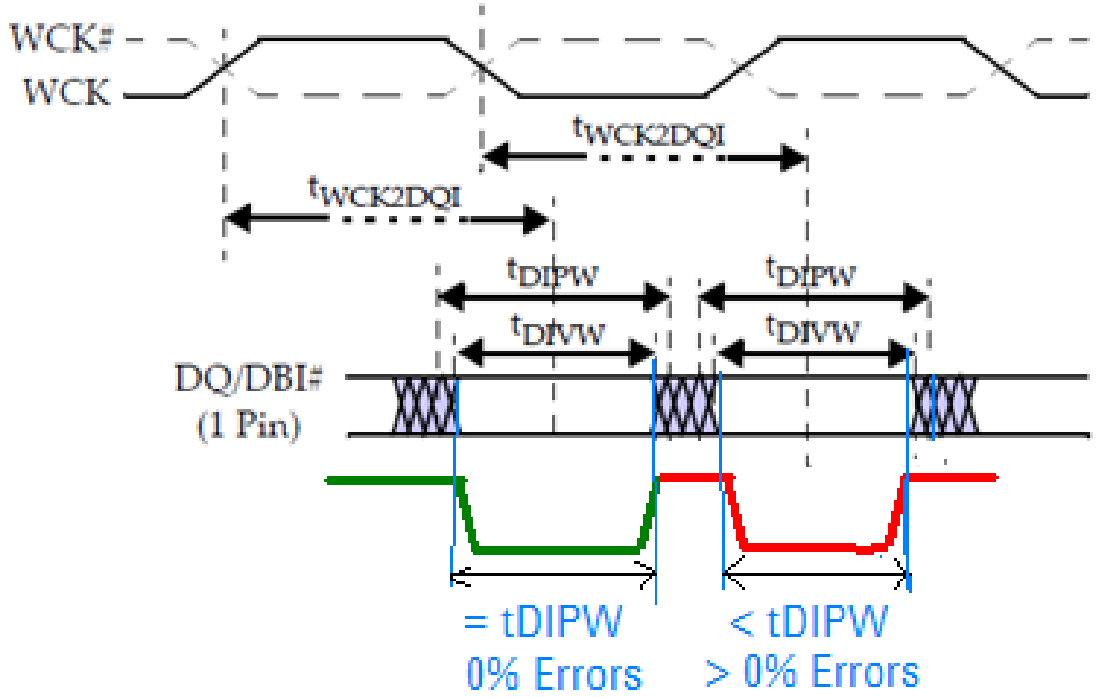
N-Cycle Tj Requirement (BER = 1/N)

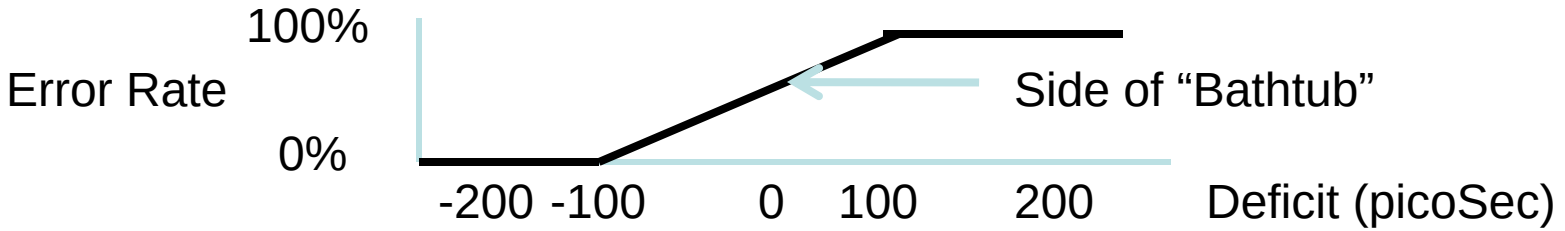
Gap between N-Cycle Tj and optimal (low BER) is negligible

Impact on binning and yields is small

The Reality Above 1 Gb/s

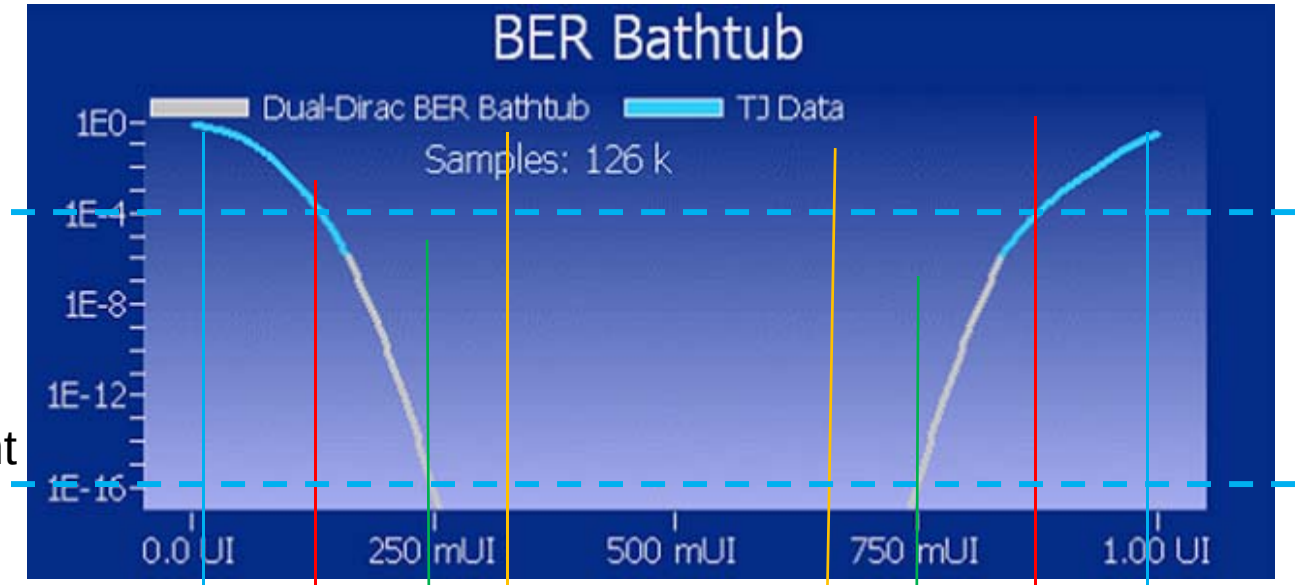
Current Tj specs are often violated over time





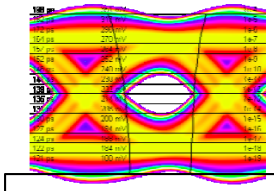
Why Is This A Problem?

Reliability margin in no longer “free”



N-Cycle Tj BER Limit

System Reliability Requirement (on each Y)



Large range of uncertainty in setting DRAM and jitter spec. Channel simulation now necessary.

Overly tight spec

Optimal spec returns margin to budget

Strict use of Tj spec gives High system failure rate!

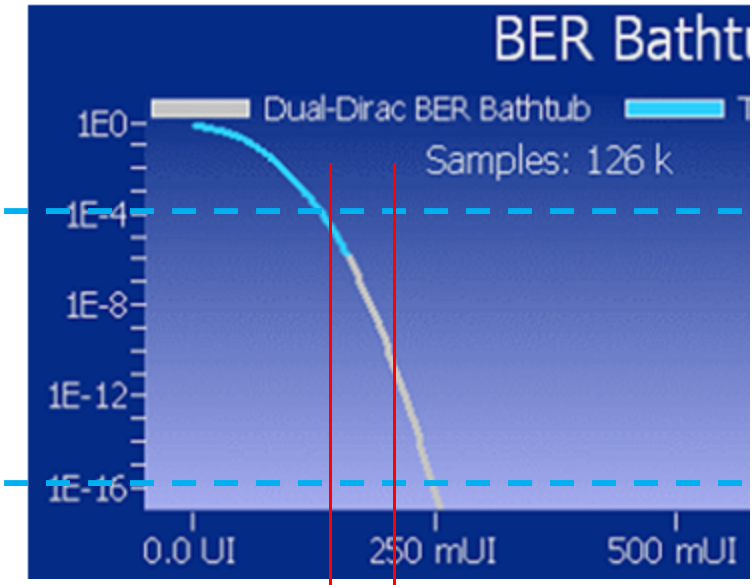
Best case simulation

DD extrapolation is only feasible way to measure

How Big Is It?

N-Cycle Tj
BER Limit

System
Reliability
Requirement



Tj Error

N-Cycle Tj Error vs.
DD model (Rj only)

BER Exponent	Direct Meas. Time (hr)	Rj Missed (ps)	% tHP
2.3	0.00	11.44	1.83%
4	0.00	0.00	0.00%
12	0.52	33.15	5.30%
16	5200.92	45.03	7.20%
18	520092.41	62.26	9.96%

DDR3/1600 @ 5ps Rj (rms)

Data Rate	tIS + tIH	% tDIVW (BER 1E-12)
800	475	7.85%
1067	325	11.48%
1333	205	18.19%
1600	165	22.60%
1867	165	22.60%
2133	155	24.06%

Data Rate	tDIPW	% tDIPW (BER 1E-12)
800	600	6.22%
1067	490	7.61%
1333	400	9.32%
1600	360	10.36%
1867	320	11.66%
2133	280	13.32%

Data Rate	tDS + tDH	% tDIVW (BER 1E-12)
800	225	16.58%
1067	125	29.84%
1333	95	39.26%
1600	55	67.81%

Over 33ps of timing left on the table. That's 15-50% Ts+Th!

Adding Dj components < 1E-4 BER will make it worse

What is Jedec Doing About It?

- **Next generation DRAM specifications understand Rj and BER**
  - **Specify tDIVW instead of Ts/Th**
  - **tDIVW is at a specific BER**
  - **Dual Dirac model can be used to extrapolate to any desired BER**

GDDR5 Specification

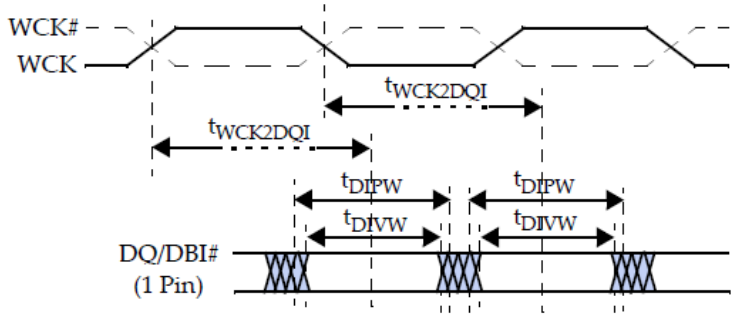


Figure 36: Data Input Timings

Table 1 -- Key Jitter Characterization Parameters

Parameter	Symbol	Min	Max	Unit	Note
Number of half periods per Jitter Measurement	M_{jtr}	$1e^{+6}$			1
Number of half periods across which Cumulative Error is Measured with PLL Off	$N_{top\text{-}off}$	50			
Number of half periods across which Cumulative Error is Measured with PLL On	$N_{top\text{-}on}$				2
Bit Error Ratio	BER				3,4

1. A half period, in this context, is one half of one clock cycle.
2. Vendor specified value.
3. Vendor specified Bit Error Ratio.
4. Bit Error Ratio is the probability for a single bit to be received in error. It is recommended that this value not be less than 1e-12

Table 2 -- Maximum Allowable Clock Input Jitter for N-Cycle Half Period Jitter
tCK/tWCK = tbd Ghz
Temp = tbd, VDD = tbd, VDDQ = tbd

N	RJ^N RMS	TJ^N
1		
2		
3		
4		
5		
...		
Ntop		

The Bottom Line

- **While Bit Error Rate based timings are new to memory, they are well established in high speed digital standards**
- **GDDR5 and DDR4 will implement these concepts in the spec and/or measurement procedures for AC timing**
- **This will simplify system design, silicon characterization and qualification, and validation**
- **It's time to apply these concepts to <u>your</u> designs as well**