DDR4 Module Level Trends and Features

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Agenda

• Mode Register PDA
  – Per DRAM Addressability

• C/A Parity

• Expanded Addressing
  – CID for stacks

• Potential module density options

Note: This document provides a high level overview and does not include all aspects that are reflected in the device datasheet. Before operation of a DDR4 device, please refer to a complete datasheet.
Mode Register PDA
(Per DRAM Addressability)
How are the mode registers within the DRAM programmed for DDR, DDR1, DDR2 and DDR3?

- The memory controller must provide a Mode Register Set (MRS) command with valid bank addresses, the DRAM chip select low and applicable data on the address inputs.

  - BA[3:0] Bank addresses are used to select the individual mode registers within the DRAM (MR0, MR1, MR2...).
  
  - A[15:0] Addresses are used as operands for actual register content to be programmed.
**Example 1** (Programming DDR3 mode registers)

- **BA[3:0] = 010** for Mode Register 2

- **A[14:0] = 0090h** sets:
  - CWL to 7 clocks
  - ASR to Disabled
  - SR Temp to 95°C
  - Dynamic ODT Disabled
  - Other others to default conditions

- MRS command to DRAM
• **The problem** (prior to DDR4 memory)
  
  – DDR3 Example 1, all eighteen DRAM in Rank 0 will have their mode registers programmed exactly the same way, no exceptions.
Mode Register PDA

- DDR4 solves this problem by utilizing the strobes and DQ[0] of each DRAM which allows the host to uniquely select individual DRAM to be programmed.
  - This feature is called **Per DRAM Addressability** which requires three (3) steps
    - **Step 1)**
      Place DRAM in PDA mode (similar to MRS function in DDR3).
    - **Step 2)**
      Program the unique DRAM locations by using posted MRS commands, address inputs and DQ[0].
    - **Step 3)**
      Take DRAM out of PDA mode (similar MRS function in DDR3).
• **Example 2** (Programming DDR4 mode registers)
  - **Step 1**, Place DRAM into PDA mode.

  BG[1:0], BA[1:0] = 3h addresses Mode Register 3

  MRS command to DRAM

  A[17:0] must reflect applicable values for all registers, but to place the DRAM in PDA mode **A4 must be set to “1”**

  BG[1:0], BA[1:0] = 3h addresses Mode Register 3
All of Rank 0 DRAM will be in **PDA mode**

- DDR4 Example 2 will program all eighteen DRAM in Rank 0 exactly the same way (in this case place them in PDA mode).
• **Example 3 (Utilizing PDA mode)**
  - **Step 2**, Program selected DRAM (in this case the ECC bits will have their mode register programmed differently than the others).

  - **MRS command to DRAM.** The MRS command and address inputs are held in the DRAM until \( T_{b+1} \) at such time they are validated with \( DQ[0] \).

  - In PDA mode, the status of \( DQ_0 \) is clocked in with the edge of \( DQS \).

  - Only the DRAM with \( DQ_0=0 \) will have their mode registers programmed
    - \( DQ[64:0] \) bits are all high
    - \( EEh = 1110\ 1110 \) which make \( DQ_0 \) for each of the ECC DRAM equal to zero.
Mode Register PDA

- Programming selected DRAM within PDA mode
  - Example 3, using PDA mode with applicable addressing on the data bus, only the mode registers in the ECC DRAM are being programmed.
**Example 4** (Turning off PDA mode)

- **Step 3**, Turn off PDA mode for all DRAM within the rank

At time $T_a$, the host sends a posted MRS command (which is held in the command queue of the DRAM to be gated and validated with DQ[0]).

$T_{b+1}$ the host tells only DRAM with its DQ[0] = 0 to process the MRS command.

At $T_c$, the DRAM is ready for either another PDA command, or to take the Rank out of PDA mode.
Mode Register PDA

- Disabling PDA mode
  - Example 4, turns off PDA mode for all eighteen DRAM in Rank 0.
Mode Register PDA

• Mode Register, Per DRAM Addressability (PDA)

  – Pros
    • No additional pins to support
    • No performance impact
    • Can be enabled or disabled if not required by the system

  – Cons
    • None
C/A Parity
The problem (prior to DDR4)

- C/A Parity is only checked at the channel level and the DRAM may process erroneous commands.

The secondary side of the register is not covered prior to DDR4 technology.
• The solution
  - DDR4 can support C/A Parity through the DRAM.
**Command / Address Parity**

- DDR3 RDIMM Command/Address parity example

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The register compares the next PAR_IN status bit with the previous command, address inputs. If the registers parity calculation does not match, it will drive the ERROUT# signal low to flag the host controller.

*Note: The bad C/A is passed through and will be processed by the DRAM.*
Command / Address Parity

- DDR4 C/A parity feature.
  - In addition to detecting a C/A parity error, the DRAM flags the error, halts process of commands and logs the occurrence in a mode register.
  - When used in conjunction with a register the register may also be required to be configured.
• Steps to use C/A include configure DRAM, monitor status, clear error and resubmit commands/data as applicable.
• DDR4 component level example.

➢ Normal Operation through T2
➢ At Ta0 the DRAM detects a parity error, blocks the bad command and pending incoming commands. The DRAM logs the error and asserts the ALERT# signal to flag host of parity error. The ALERT# signal is asynchronous and will appear at some after Ta1.
➢ After Tc0 the DRAM has closed open rows, releases the ALERT# signal, and is ready for new commands.
➢ Depending on ALERT# timing, at Td0 or Td1 the DRAM will receive new commands. Note until the host has cleared the Parity Error Status the DRAM will not be checking parity and could process erroneous commands.
Command / Address Parity

- DDR4 module level example.

The register passes the PAR_IN status bit through to the DRAM along with the command, address inputs. If the DRAM parity calculation does not match, the DRAM drives the ALERT# pin low and the register will drive the ERRROUT# signal low to flag the host controller.

Note the DRAM does not process the command when an parity error is detected.
Command / Address Parity

• DDR4 Command / Address parity feature

  – Pros
    • Enhances the reliability of a system as it extends parity all the way to the DRAM.

  – Cons
    • The processing of the command at the DRAM is delayed by the time it takes the DRAM to calculate parity and release the command for execution (typically 4 to 6 clock cycles). Note this latency is applicable for all commands.
    • Additional signals compared to DDR3.
Expanded Addressing
(CID for stacks)
Expanded Addressing (CID for stacks)

- DDR4 supports multiple package options which include
  - Monolithic Single Die Package (SPD)
  - Standard Dual Die Package (DDP)
  - 3DS Packages (Three Dimensional Stacks)
    - 2-High (Two Logical Ranks with single signal loads)
    - 4-High (Four Logical Ranks with single signal loads)
    - 8-High (Eight Logical Ranks with single signal loads)
Unlike prior DDRx stacks that utilizes an unique Chip Select (CS#) for each rank within the stack, DDR4 uses a single Chip Select per package and Chip ID inputs to select each logical rank within the stack.

- Chip ID decodes as shown below.

<table>
<thead>
<tr>
<th>Access To:</th>
<th>C2</th>
<th>C1</th>
<th>C0</th>
<th>CS#</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logical Rank 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 4</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 6</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>Logical Rank 7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Low</td>
</tr>
</tbody>
</table>

Note: For a 2-High only C0 is required, for a 4-High only C0 and C1 are required.
Expanded Addressing (CID for stacks)

- Possible DDR4 package density with CID

<table>
<thead>
<tr>
<th></th>
<th>4Gb</th>
<th>8Gb</th>
<th>16Gb</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDP</td>
<td>4Gb</td>
<td>8Gb</td>
<td>16Gb</td>
</tr>
<tr>
<td>3DS (2-H)</td>
<td>8Gb</td>
<td>16Gb</td>
<td>32Gb</td>
</tr>
<tr>
<td>3DS (4-H)</td>
<td>16Gb</td>
<td>32Gb</td>
<td>64Gb</td>
</tr>
<tr>
<td>3DS (8-H)</td>
<td>32Gb</td>
<td>64Gb</td>
<td>128Gb</td>
</tr>
</tbody>
</table>
Expanded Addressing CID for stacks

- **Pros**
  - Fewer signals are required to select logical ranks.
  - Provides for extreme density options.

- **Cons**
  - None.
Potential module density options
## Potential module density options

- Reflects typical server module configurations using x4 and x8 DRAM.

<table>
<thead>
<tr>
<th>DRAM Density</th>
<th>4Gb</th>
<th>8Gb</th>
<th>16Gb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td>x4</td>
<td>x4</td>
<td>x4</td>
</tr>
<tr>
<td>Single Rank</td>
<td>8GB</td>
<td>16GB</td>
<td>32GB</td>
</tr>
<tr>
<td>Dual Rank</td>
<td>16GB</td>
<td>32GB</td>
<td>64GB</td>
</tr>
<tr>
<td>Quad Rank</td>
<td>36GB</td>
<td>72GB</td>
<td>128GB</td>
</tr>
<tr>
<td>Octal Rank</td>
<td>64GB</td>
<td>128GB</td>
<td>256GB</td>
</tr>
</tbody>
</table>
Thank You