Developed Hybrid Memory System for New SoC.

-Why choose Wide I/O?

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Agenda

◆ 4K (UHD) market and changes in requirement
◆ Development goal and our challenges
◆ Approach to the next generation applications and conclusion
Panasonic’s System LSI?

Deploy ASIC business by utilizing system LSI design technologies and assets.

Market proven high quality global TV platform

4K business

Digital Signage

SoC Platform

4K-TV

Security

Media Player Transcoder

4K Tablet

HDMI 2.0

WiGig

STB

DTV/Smart TV

OA equipment

Industrial machinery

Medical device

growing Market

Deploy ASIC business by utilizing system LSI design technologies and assets.

Global Standards for the Microelectronics Industry

JEDEC
Exploding 4K2K (UHD) Market

4K2K-DTV market is growing faster than expected

✓ Forecast has been revised upward from quarter to quarter.
  2013Q3  20M unit @2017
  2014Q1  60M unit @2017

✓ 4K2K-shift of smart phone will also be rapid.
  2014Q1  150M unit @2017

✓ 4K2K-shift in other markets will also be the same.
  Medical market (Endoscope, Telemedicine)
  Amusement market
  Digital signage market, etc.

Source: Display Search
4K increases data traffic and bandwidth

Shift to 4K resolution will increase the video streaming data volume rapidly.

✓ Increase in "Internet traffic" with conventional codec.

HEVC, a new CODEC with higher compression rate, will reduced the data volume by half.

✓ The appliances require more bandwidth

17GB/s for 4K-HEVC & video processing

HEVC-decode, Post processing, OSD, Video-out

25GB/s for 4K-HEVC whole system

CPU processing (OS/Web Browsing), etc.
Development Goal

✓ DRAM requirements

✓ 2 types of application
  A) Video Processing (HEVC decode/Graphics)
      memory bandwidth = Hi, memory size = Mid
  B) CPU Processing (OS/Web Browsing)
      memory bandwidth = Best-effort, memory size = Large

✓ Low power consumption for mobile use
✓ In mass production @ 2014Q2

✓ Typical use case

Case1: long time "HEVC video playback"
  - Band Width 17GB/s
  - Power 500mW or less (Memory budget)
  - Density 4Gbit

Case2: CPU processing (OS/Web browsing) in addition to Case1
  - Band Width 25GB/s
  - Power 1000mW or less (Memory budget)
  - Density 12Gbit
Rough estimation: memory selection

CASE1: DRAM configuration for 17GB/s

<table>
<thead>
<tr>
<th>B/W</th>
<th>Memory</th>
<th>bit rate</th>
<th>pieces</th>
<th>state</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>17GB/s</td>
<td>WideIO1</td>
<td>266Mbps</td>
<td>X1</td>
<td>available</td>
<td>300mW</td>
</tr>
<tr>
<td></td>
<td>WideIO2</td>
<td>533Mbps</td>
<td>X1</td>
<td>2015</td>
<td>300mW</td>
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<tr>
<td></td>
<td>LPDDR3</td>
<td>2133Mbps</td>
<td>X2</td>
<td>available</td>
<td>800mW</td>
</tr>
<tr>
<td></td>
<td>LPDDR4</td>
<td>2133Mbps</td>
<td>X2</td>
<td>2015</td>
<td>480mW</td>
</tr>
<tr>
<td></td>
<td>DDR3L</td>
<td>2133Mbps</td>
<td>X4</td>
<td>available</td>
<td>1400mW</td>
</tr>
<tr>
<td></td>
<td>DDR4</td>
<td>2133Mbps</td>
<td>x4</td>
<td>available</td>
<td>800mW</td>
</tr>
</tbody>
</table>

✓ Only Wide I/O meet CASE1

CASE2: DRAM configuration for 25GB/s

<table>
<thead>
<tr>
<th>B/W</th>
<th>Memory</th>
<th>bit rate</th>
<th>pieces</th>
<th>state</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>25GB/s</td>
<td>WideIO1</td>
<td>—</td>
<td>—</td>
<td>available</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>WideIO2</td>
<td>800Mbps</td>
<td>X1</td>
<td>2015</td>
<td>400mW</td>
</tr>
<tr>
<td></td>
<td>LPDDR3</td>
<td>2133Mbps</td>
<td>X3</td>
<td>available</td>
<td>1200mW</td>
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<tr>
<td></td>
<td>LPDDR4</td>
<td>3200Mbps</td>
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<td></td>
<td>DDR3L</td>
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<tr>
<td></td>
<td>DDR4</td>
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<td>X6</td>
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<td>1200mW</td>
</tr>
</tbody>
</table>

✓ No configuration meet CASE2 except next-generation DRAMs

✓ Combination of Wide I/O and other DRAM (DDR3/L) has a potential.

However, there are some concerns:

1. Efficiency of DRAM
2. Performance gaps between Wide I/O and DDR3
3. TSV technology is required
Panasonic Challenges

Develop hybrid memory system using Wide I/O that can realize 4K applications

✓ Challenge-1:
  Realize "Case-1" only with Wide I/O memory
  Gaps between required bandwidth and Wide I/O bandwidth

✓ Challenge-2:
  Conceal the memory specification differences from access masters
  These different in memory specification results in system performance loss

✓ Challenge-3:
  Establish assembling technology of Wide I/O without using TSV process
  In the TSV method, there are concerns about mass production like quality, yield, and also reliability.
Challenge-1

Insufficient bandwidth of Wide I/O memory if you consider the bandwidth overhead

- HEVC decoder: 10GB/s per channel
  Need Wide I/O x3 channels.
- Video processing & CPU: 7.5GB/s and more
  Need Wide I/O x2 channels.
But total Wide I/O bandwidth is 4.25GB/s x4 (17.0 GB/s)

New

Developed optimized Wide I/O memory system

1. Adopted 266 MHz speed class Wide I/O
2. Bind 2 physical channel into one logical channel
3. Developed a new memory controller with improved bandwidth efficiency
   - 10bit rectangle access for HEVC Main10
   - DRAM data allocation for preventing bank conflict.
   - Optimized access size from masters

Realized 4K@60p HEVC Main10 decode & Playback only with Wide I/O.
Challenge - 2

System performance decreases by the differences of memory performance.

Factor of the performance decreases

(A) Difference of DRAM configuration

(B) Different situation of access competition to the memory

(C) Different congestion in the system bus

Developed High performance intelligent memory controller and system bus for the hybrid memory configuration

(A) QoS scheduling of each access master

(B) Control latency by dynamically changing priority

(C) High performance intelligent Bus

- High bandwidth system bus: 320bit at 1GHz speed
- Flow control function

Concealed the memory spec. differences from access masters
Achievement of Challenge-1 & 2

- Realized low power 4K HEVC decode and video processing only with Wide IO that is important for mobile use.
- System can minimize the power consumption by selectively activating each memory based on its application.

Realized flexible hybrid memory system with minimized power consumption.
Challenge-3

Developed non-TSV package to assemble Wide I/O memory
✓ Can achieve lower assembly cost compared with TSV technology by utilizing:
  • wire bonding and substrate of 4Layer through hole
  • face to face joint of μ-Bumps
✓ Can assemble even in the case that memory die size is larger than SoC die size.
  • Chip resin expansion

<table>
<thead>
<tr>
<th>New</th>
<th>Non-TSV package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assembly</td>
<td>Face to Face Joint</td>
</tr>
<tr>
<td></td>
<td>RDL routing on SoC</td>
</tr>
<tr>
<td>Substrate</td>
<td>4 Layer through hole</td>
</tr>
<tr>
<td></td>
<td>Cu Wire Bonding</td>
</tr>
<tr>
<td>SoC</td>
<td>IO is beneath μ-Bump</td>
</tr>
</tbody>
</table>

Wide I/O memory can be adopted in all size of SoCs by utilizing our tech.
Hybrid Memory System Summary

- Using JEDEC standard Wide I/O@266Mbps and DDR3@2133Mbps x32
- Optimized Wide I/O and DDR3/L memory controller
- Concealed the memory spec. differences from access masters
- Non-TSV package using chip resin expansion and wire bonding technology

Achievement:
1. 4K@60p HEVC Main10 decode & playback only with Wide I/O
2. Consistent control of Wide I/O memory and DDR3 memory
3. Flexible hybrid memory system with minimized power consumption
Panasonic New Product

Developed System LSI which support HEVC Main10 4K@60p decode

Demonstrated in exhibitions. http://www.youtube.com/watch?v=38zjAE5EWms
New SoC expand 4K business

Panasonic new SoC with hybrid Memory System expands 4K market with its flexibility and low power consumption.

- Wide I/O only solution (17GB/s, 4Gbit, 200mW)
- Hybrid memory solution (Wide I/O+DDR3)

Panasonic SoC supports variety of applications and provide high user experience.
Next Generation

- The future application, such as multi-4K and 8K, will require over 50GB/s.
- Wide I/O2 using “like LPDDR2 technology" is relatively low risk.
- “Non-TSV package technology" supports Wide I/O2.
- Memory capacity is extendable by utilizing external memories.

Hybrid Memory System with Wide I/O2 will open the door to the future applications.
Conclusion

Developed world's 1st complete 4K 60p SoC.

- The 4K HEVC 60p 10bit video playback realized only with "single Wide I/O"
- Realized consistent controlling of Wide I/O memory and DDR3 memory
- Established non-TSV package assemble technology of Wide I/O memory
- Flexible hybrid memory system with minimized power consumption

Hybrid memory system for Wide I/O and Wide I/O2 will open the door to future applications.
Thank You