Sophie Dumas
ST-Ericsson
JC42.6 Chairman

Mobile Memory Forum: LPDDR3 and WideI/O
June 2011
Agenda

- ST-Ericsson: about us...
- Mobile Market Trends drive Low Power DRAM
- JC 42.6 Activities:
  - LPDDR3
  - WideIO
- Questions
ST-Ericsson: about us...

- ST-Ericsson is a leading global supplier of platforms and semiconductors for wireless
- JV owned equally by STMicroelectronics and Ericsson
- Global workforce of 6700 employees with more than 85% of employees in R&D

Our aim

- Leadership in smartphones and tablets
- Drive innovation in mobile broadband
- Enable coolest, richest, affordable devices
ST-Ericsson: The Best of Both Worlds

**Premium/High**
Best-in-class application processors matched with the latest modems

**Mainstream**
Integrated solutions for industry-leading BoM and size with the best performance in every tier

- Time to market
- Performance
- Flexibility
- Size
- Bill of Materials
- Cost

Reuse & integrate

ST-Ericsson: The Best of Both Worlds

Novathor™ by ST-Ericsson

Novathor™ by ST-Ericsson

Novathor™ by ST-Ericsson
ST-Ericsson approach: performance and flexibility

Leading thin modems for any device

Best-in-class application processors with the latest broadband modems

Integrated solutions for industry-leading bill of material and size with best performance in every tier

Full complement of connectivity and enhancements

Customers like it: 7 of top 9 device manufacturers actively engaged with us on new platforms
Mobile Market Trends drive Low Power DRAM
High Speed Internet experience

Amazing Mobile Market Applications

Ultra-responsive user Interfaces

Immersive gaming

4G

Gestures-controlled UI

Telepresence

Augmented Reality

Ambient Interaction

HD cameras and camcorder

Location-based services

Full HD mediacenter

Computer Vision

Global Standards for the Microelectronics Industry
ARM Core & Low Power DRAM: Parallel Performance Growth

Source: Hynix
Mobile Display: Size and Resolution trends

- Smartphones and Tablet drive display size: WVGA or higher display increasing rapidly
- 4.0” or larger display becoming mainstream of smartphones

Display resolution will double (Smartphones), quadruple (Tablets)

➡️ use significant more memory bandwidth
Smartphones: Display Thickness and Size trends

Display Size will increase, and linked to higher Resolution
⇒ more memory bandwidth

- Display Thickness of randomly selected major Smartphones
- After mid 2010: display thickness decreasing and size increase
Video & Display Resolution vs Memory BW

High graphics and video performance ➔ High DRAM BW for Smartphones & Tablets

Dimensioning Use Case:
3D video streaming playback to external display via wireless (WiFi or DLNA) + online 3D gaming local

Includes: video, graphics and display sub-systems

Source: ST-Ericsson

JEDEC
Global Standards for the Microelectronics Industry
OS + Applications vs Memory Density

Applications performances ➔ Density increase for Smartphones & Tablets

Density: GBytes (Typical)

1 GB

Phone (Volume)

Source: ST-Ericsson, Hynix
Low Power DRAM Drivers

High Bandwidth & High Density for Smartphones and Tablets driven by:

Video performance increase
Display: High Resolution (HD), stereoscopic (3D)
Graphics: High quality 3D
User Application, multi-tasking

..... impact on DRAM....
After LPDDR2: LPDDR3 and WideIO...

- Graphics performance & Display resolution require higher memory BW in 2013
- ..... \textbf{BUT} quad-channel LPDDR2 is not an option (pin count, power efficiency)

- \textbf{DC LPDDR2 @533MHz}
  - 80 mW/GBps
- \textbf{SC LPDDR2 @400MHz}
  - 3.2GBps
  - 1.5 GBps
- \textbf{Dual Channel LPDDR3 @ 800MHz}
  - 12.8GBps
  - 70 mW/GBps
- \textbf{WideIO @ 200MHz}
  - 10GBps
  - 40 mW/GBps

Note: Bandwidth for HOST CPU not included
Note: IO power conditions: LPDDR2 (5pF), LPDDR3 (4pF), WideIO (2-die stack, 2pF)
JC-42.6 Activities

- JC42.6 charter: Low Power DRAM
- Chairman: Sophie Dumas, ST-Ericsson, CTO Office
- 2 active TG: LPDDR3, WideIO

### Bandwidth (GBps)

- **LPDDR1**: 1.6
- **LPDDR2**: 8.5
- **LPDDR3**: 12.8
- **WideIO SDR 200**: In Progress

### Timeline

- **2008**: LPDDR1
- **2010**: LPDDR2
- **2012**: LPDDR3

### Features

- Pop and Discrete low cost packaging
- Low power 3D Integration Stacking Technology
- High Volume Ramp Up Devices
LPDDR3
LPDDR3 positioning

- Increased memory BW requirements (graphics, display resolution increase)
- LPDDR2 will run out of bandwidth before WideIO is available
- LPDDR3 fills the gap by upgrading the LPDDR2 standard and supporting higher operating frequencies
## LPDDR3 target electrical specification

<table>
<thead>
<tr>
<th>Parameters</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock speed</td>
<td>200-533 MHz</td>
<td>400-800 MHz</td>
</tr>
<tr>
<td>Max BW 1 ch (2 ch)</td>
<td>4.2 GBps (8.5 GBps)</td>
<td>6.4 GBps (12.8 GBps)</td>
</tr>
<tr>
<td>DRAM array architecture</td>
<td>1.2V core with 1.8V wordline</td>
<td>boost</td>
</tr>
<tr>
<td>DRAM IO architecture</td>
<td>1.2V, HSUL_12</td>
<td>=</td>
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<tr>
<td></td>
<td>No DLL in DRAM device</td>
<td>=</td>
</tr>
<tr>
<td>CLK/DQS scheme</td>
<td>Diff/ Bi-dir</td>
<td>=</td>
</tr>
<tr>
<td>ADD/CMD scheme</td>
<td>DDR, single ended</td>
<td>=</td>
</tr>
<tr>
<td>Data scheme</td>
<td>DDR, single ended</td>
<td>=</td>
</tr>
<tr>
<td>Low Power Modes</td>
<td>self-refresh, PASR, DPD</td>
<td>=</td>
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<tr>
<td>Internal bus width</td>
<td>X128 (4n prefetch)</td>
<td>X256 (8n prefetch)</td>
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<tr>
<td>Max density</td>
<td>8 Gbits</td>
<td>32 Gbits</td>
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<tr>
<td>Package</td>
<td>POP &amp; MCP</td>
<td>=</td>
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<tr>
<td>Burst types</td>
<td>BL4, BL8, BL16</td>
<td>BL8</td>
</tr>
</tbody>
</table>
LPDDR3 Benefits

- LPDDR3 is a simple evolution of LPDDR2
- Higher BW than LPDDR2:
  - 800 MHz LPDDR3 vs 533 MHz LPDDR2 = +50%
  - 667 MHz LPDDR3 vs 533 MHz LPDDR2 = +25%
- LPDDR3 is higher density than LPDDR2
- Equivalent pin-count as LPDDR2
- Lower IO capacitance to improve IO power and SI
- Same BW than WideIO in dual-channel configuration
- Lower assembly and test costs than Wide I/O
LPDDR3 Availability

- LPDDR3 Task Group created in Q4 2010
- Dan Skinner, Micron, TG Chair
  Wendy Elsasser, Cadence, Vice Chair

- Standard definition is progressing full speed

- Specification target:
  - Preliminary Spec: Sept 2011
  - Final Spec: Dec 2011

- Devices:

  2011  
  LPDDR2  
  3.2 GBps

  2012  
  LPDDR2  
  4.3 GBps

  2013  
  LPDDR3  
  6.4 GBps

  2014  
  WideIO  
  12.8 GBps

Expected Device Mass Production
Wide IO
WideIO Positioning

WideIO offers twice the BW of LPDDR2 for same power

<table>
<thead>
<tr>
<th>BW (GBps)</th>
<th>Memory power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12.8</td>
<td>850</td>
</tr>
<tr>
<td>8.5</td>
<td>660</td>
</tr>
<tr>
<td>6.4</td>
<td>530</td>
</tr>
<tr>
<td>3.2</td>
<td>250</td>
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</table>

Note: IDD4 (Data toggle 50%), Memory controller + DRAM, LPDDR2 8pF, Wide IO 2pF (2-die stack)
WideIO is Low Power

- Reduced interconnect capacitance (TSV)
- IO buffering in both SoC and DRAM
- Reduced operating frequency
- SDR sampling mode

Power Consumption @ same BW
2x LPDDR2 400MHz versus
WideIO SDR 200MHz

Source: Samsung Wide-IO Memory for Mobile Products - A Deeper Look by i-Micronews
# Stacking or Hybrid Configurations

<table>
<thead>
<tr>
<th></th>
<th>Stacking (DRAM Cube)</th>
<th>Hybrid</th>
</tr>
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</table>
| **Application**  | **WideIO as system memory**  
-SiP package with DRAM “cube”  
-up to 4 stacked dice  | **Cache memory for multimedia**  
- SiP bottom package  
- FC SoC die (Controller) with TSVs  
- Single stacked DRAM  
- Additional Memory top package: POP single or dual LPDDR2 (+ flash) |
| **Pros**         | Simple SW & memory Interface in chipset  
Small & thin form-factor  
High performance (BW & power)  | Higher BW  
Low Memory cost |
| **Cons**         | High Memory Cost  
Maturity in TSV technology  | Increases chipset cost (multiple memory IF) |

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**Diagram**

[Diagram showing Stacking (DRAM Cube) configuration: x512 Wide IO SDR, Controller.]

[Diagram showing Hybrid configuration: LPDDR2/3, x512 Wide IO SDR, Controller.]

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Global Standards for the Microelectronics Industry
WideIO Cross Section

- WideIO DRAM die is stacked on top of the mobile processor in the same package to reduce interconnect capacitance
- Face-to-Back stacking with Through Silicon Vias (TSVs) in the mobile SoC flip-chip die
- ST-E preferences: µbumps directly on SoC TSV tips (could also be re-distributed with backside SoC metal layer)

![WideIO Cross Section Diagram]

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Global Standards for the Microelectronics Industry
WideIO electrical specification

- Large bus interface (512 bits) at low frequency (200 MHz) in SDR
- 4 independant and fully asynchronous channels
- BW = 12.8 GBps (200Mbps per pin)
- VDD1 = 1.8V, VDD2 = 1.2V, VDDQ = 1.2V
- Low Power Features: PASR, Auto TCSR
- Balls allocated for future DDR extension
- Total number of balls including supply: 1200 (193/ch signal)
- Density: up to 32 Gbit monolithic
- Up to 4 DRAM dice stacked on top of the mobile processor
- Boundary Scan
- IO physical location
  - Each channel has 6 rows and 50 columns
  - 40µm min pad/bump/TSV pitch
Temperature sensors

ST-Ericsson WideIO SoC floor plan

- One Smart Memory Engine (SME) per channel
- Includes the Network IF + Controller

Courtesy of ST-Ericsson
WideIO specification Availability

- WideIO Task Group created in Q4 2008

- DooHee Hwang, Samsung, TG Chair
  Ken Shoemaker, Intel, Vice Chair

- Specification Availability Target :
  - Preliminary Spec: Sept 2011
  - Final Spec: Dec 2011
Thank You!
Questions?