Evolutionary Migration from LPDDR3 to LPDDR4

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- Mobile Application Trend
- Introduction of LPDDR4
- New Features of LPDDR4
Mobile Application Trend
Smart Mobile Devices as Heart of Life
Unlike PC devices, mobile device performance has been rapidly improving.

Enormous Improvement on Performance of SOC with higher clock speed and multi-core processor.

[Source : Specfp®]
Mobile Evolution

The mobile evolution is expanding to more powerful devices with endless innovation of low power consumption and high performance.
What’re Key Values from Mobile DRAM …..

- Higher and Clearer Resolution
- Panorama Photograph
- Multi-screen Display

Better Media Experience

- 2160p UHD: 20GB/s
- 1080p FHD: 8.8GB/s @ 60fps, 4.4GB/s @ 30fps
- 720p HD: 1.9GB/s @ 30fps

Required DRAM Bandwidth

Global Standards for the Microelectronics Industry
Next Generation Mobile DRAM

Mobile DRAM Evolutionary Path

2006 LPDDR
- 1.8V
- ~400 Mbps / pin
- ~1.6 GBps (x32)

2010 LPDDR2
- 1.2V
- ~1066 Mbps / pin
- ~4.3 GB/s (x32)
- ~8.5 GBps (x64)

2013 LPDDR3
- 1.2V
- ~1866 Mbps / pin
- ~7.5 GB/s (x32)
- ~15 GBps (x64)

2015 LPDDR4
- 1.1V
- ~3200 Mbps / pin (ODT)
- ~12.8 GBps (x32)
- ~25.6 GBps (x64)

Wide IO
- 1.2V
- 266 Mbps / pin
- 17 GB/s (x512)

Wide IO2
- 1.1V
- 800 Mbps / pin
- 25.6 GBps (x256)
- 51.2 GBps (x512)
Future Mobile Positioning

WIO2
Extremely High B/W & Low Power

LPDDR4
Density Scalability at Affordable price

Power Efficiency

Cost

Wide IO2

Global Standards for the Microelectronics Industry
Mobile System’s Density Requirement

3GB and 4GB Mobile system is just around the corner.
Key Factors for Next Mobile Solution

3 key factors are driving next mobile solutions

- Performance: Requiring over 20GB/s BW
- Power Efficiency: Power budget is critically necessary
- Cost Budget

JEDEC
Global Standards for the Microelectronics Industry
Introduction of LPDDR4
Advantages of LPDDR4

**Power Efficiency**

- **1.2V → 1.1V**
- Lower Power Supply
- (mw/GBps)

- **LPDDR4**
  - 35% Better Power Efficiency
- LPDDR3

**Low Frequency Mode**

- **Power Saving in Low Frequency Mode**
- High Frequency Mode (3200Mbps w/ term.)
- Low Frequency Mode (1600Mbps w/o term.)

Global Standards for the Microelectronics Industry
# Mobile DRAM Features Comparison

<table>
<thead>
<tr>
<th></th>
<th>LPDDR2-S4B</th>
<th>LPDDR3</th>
<th>LPDDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Rate (per pin)</strong></td>
<td>333~1066 Mbps</td>
<td>800~2133 Mbps</td>
<td>400~3200 Mbps (~4266Mbps)</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>64 ~ 8Gb</td>
<td>4Gb ~ 32Gb</td>
<td>8Gb ~ 32Gb</td>
</tr>
<tr>
<td><strong>Interface</strong></td>
<td>HSUL_12 w/ optional ODT</td>
<td>HSUL_12</td>
<td>LVSTL</td>
</tr>
<tr>
<td><strong>Command/Address Bus</strong></td>
<td>DDR</td>
<td>DDR</td>
<td>SDR (Multi cycle command)</td>
</tr>
<tr>
<td><strong>Data Bus</strong></td>
<td>DDR</td>
<td>DDR</td>
<td>DDR</td>
</tr>
<tr>
<td><strong>Voltage (VDD1/2/CA/Q)</strong></td>
<td>1.8V/1.2V/1.2V/1.2V</td>
<td>1.8V/1.2V/1.2V/1.2V</td>
<td>1.8V/1.1V/1.1V</td>
</tr>
<tr>
<td><strong>I/O organization</strong></td>
<td>x16 / x32</td>
<td>x16 / x32</td>
<td>2 ch. x16 (total x32 per die)</td>
</tr>
<tr>
<td><strong>Number of Banks</strong></td>
<td>4/8</td>
<td>8</td>
<td>8 / ch. (total 16 banks per die)</td>
</tr>
<tr>
<td><strong>Pre-fetch</strong></td>
<td>4</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>Burst Length</strong></td>
<td>4/8/16</td>
<td>8</td>
<td>16 / 32 / On the fly</td>
</tr>
<tr>
<td><strong>CA ODT</strong></td>
<td>-</td>
<td>-</td>
<td>Supported</td>
</tr>
<tr>
<td><strong>DQ ODT</strong></td>
<td>-</td>
<td>Supported (Optional)</td>
<td>Supported</td>
</tr>
<tr>
<td><strong>On die ECC</strong></td>
<td>-</td>
<td>-</td>
<td>for future DRAM process (vendor specific / transparent spec)</td>
</tr>
<tr>
<td><strong>Package Types</strong></td>
<td>MCP/PoP</td>
<td>MCP/PoP</td>
<td>MCP/PoP</td>
</tr>
</tbody>
</table>
New Features of LPDDR4
New 2 Channel Dual Edge Pad Architecture

Reduced routing distance allows lower core power and high speed operation

**LPDDR2/3**
- CA
- DQ Byte3
- DQ Byte1
- DQ Byte0
- DQ Byte2

**LPDDR4**
- CA_A
- DQ_A Byte1
- DQ_A Byte0

**Long Data Path** for each side

**Short Data Path** for each side
New Command Definitions for Lower Pin Count

To minimize pin count increase, CA pins are reduced from 10 to 6.

<table>
<thead>
<tr>
<th>SDRAM Command</th>
<th>SDR Command Pins</th>
<th>DDR CA pins</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CKE CK (1.0, 1)</td>
<td>CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8 CA9</td>
</tr>
<tr>
<td>REF 1</td>
<td>L L L L</td>
<td></td>
</tr>
<tr>
<td>REF 2</td>
<td>L L L L</td>
<td></td>
</tr>
<tr>
<td>Refresh (per bank)</td>
<td>L L L L</td>
<td></td>
</tr>
<tr>
<td>Refresh (all banks)</td>
<td>L L L L</td>
<td></td>
</tr>
<tr>
<td>Enter Self Refresh</td>
<td>L L L L</td>
<td></td>
</tr>
<tr>
<td>Animate (sense)</td>
<td>L L L L</td>
<td></td>
</tr>
</tbody>
</table>

LPDDR4’s reduced CA pin count and changed CA protocol (SDR) requires new command definitions.

Reference: JC42.6 committee item no. 1814.21
LPDDR4 for All Frequency Range

LPDDR4 provides an easy option to switch over between different operating frequencies

* Frequency Set Point
New Training Options

To enable high speed operation, various training are needed.

- DQ Read Training
- DQ Write Training
- DQS Interval Oscillator
- $V_{REF} \ (DQ)$ Training
- ZQ Calibration
- Command Bus Training
New Signaling Scheme

Low Voltage swing with VSSQ termination allows better signaling.
New Package / SOC Architecture

2ch. architecture will require new ball matrix for package
Spec. Ready for Future DRAM Technology

PPR (Post Package Repair)

Even Customers Can Repair Failed Cell via SW setting (MRS)

On die ECC (Error Correction Code)

DATA

Error Bit by DRAM Physical Limitation

Error Correction Code

Corrected DATA

Bit Correction
Thank you. - 감사합니다.