LPDDR3 Design Considerations

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LPDDR3 Symposium 2012
Introduction

• This section discusses practical advice on how to construct the memory subsystem of an SoC around LPDDR3
Low power memory

• Never bet against user demand for:
  – Less Cost
  – More Bandwidth
  – Less Power
  – More Capacity

... and a memory that works better when it’s hot
Terminology

• SoC: System-on-Chip containing CPU and other processing elements
• Memory Controller: Digital Logic between on-chip bus and DFI
• PHY: Mixed-signal logic between DFI and IO pads
• DFI: Standard for connection of memory controller and PHY
What is a Memory Controller and PHY?

SoC

CPU and other processors

On-chip bus

Digital Memory Controller Logic

Mixed-signal Physical Interface (PHY)

DFI Interface

LPDDR3

IO pads

Global Standards for the Microelectronics Industry
DFI 3.1 upgrades over DFI 3.0

- DFI 3.1 added support for LPDDR3
- Write Leveling (not present in LPDDR2)
- CA Training (seen previously in GDDR5)
- New training handshake for PHY independent mode
- Low Power Control interface enhancements
- Dfi_lvl_pattern added
Transitioning from DDR3

- Many new/different mode registers
- Mode Register Read
- DDR CA Bus
- Low capacitance
- Optional Per-Bank Refresh
- Termination on CA bus?
- Training reused from DDR3
Per-Bank Refresh

• JESD209-3 Refresh Cycle Times:
  – tRFCab = 210ns for 8Gb die
    • All bank: whole DRAM is offline
    • Opportunity to do internal PHY operations
    • Likely to build a backlog of commands
  – tRFCpb = 90ns for 8Gb die
    • Per bank: one bank is offline
    • Issue command 8x more often
    • Less likely to build a backlog
Transitioning from LPDDR2

- Termination
- Training
- Reduced Capacitance
- 8n Prefetch
- 8 Banks
PHY transition

- Transition from DDR3 PHY
  - Less Power
  - Accurate Impedance Matching
- Transition from LPDDR2 PHY
  - Higher Speed
  - Less Capacitance
  - Training
  - Termination
Training Overview

• MRR0 allowed before CA training
  – But don’t try it at speed...
• Train CA bus
• Send ZQ Calibration Command
• DQ Calibration
• Write Leveling
CA Training

- Aligns CA to CLK
- Both Edges
- Per Bit Allowed / Recommended
- Enter/Exit CA training mode with MRW command
  - Specially selected MRW commands are more tolerant to CA mismatch
- Future: 2 cycle CS pulse?
CA Training Sequence

- Note CA Training Sequence in JESD209-3 4.11.3.1
  - There are 10 CA pins (20 edges) to train but only 16 DQs to do it with
  - Need additional training sequence to train CA4 and CA9
CA Training from JESD209-3

Figure 45 — CA Training Timing chart
ZQ Calibration

• Calibrates output impedance – leads to signal integrity
• Periodic retraining
• Consider AOAC devices and ZQ Long after self-refresh
  – Temperature Sensitivity and drift
  – Voltage sensitivity and drift
LPDDR3 devices are subject to temperature drift rate ($T_{\text{driffrate}}$) and voltage drift rate ($V_{\text{driffrate}}$) in various applications. To accommodate drift rates and calculate the necessary interval between ZQCS commands, apply the following formula:

$$\frac{ZQ\text{Correction}}{(T_{\text{sens}} \times T_{\text{driffrate}}) + (V_{\text{sens}} \times V_{\text{driffrate}})} = \text{CalibrationInterval}$$

Where $T_{\text{sens}} = \text{MAX } (dR_{\text{ON}}dT)$ and $V_{\text{sens}} = \text{MAX } (dR_{\text{ON}}dV)$ define temperature and voltage sensitivities.

For example, if $T_{\text{sens}} = 0.75\%/^\circ C$, $V_{\text{sens}} = 0.20\%/\text{mV}$, $T_{\text{driffrate}} = 1^\circ C/\text{sec}$, and $V_{\text{driffrate}} = 15\text{mV/sec}$, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$
tDQSCCK

• tDQSCCK is the skew between the DQS (strobe) and CLK
  – First DQS transition indicates location of first data transition
  – Already an issue in LPDDR2
• tDQSCCK is now multicycle
  – Greater variability than DDR
  – Where is your data???
• Need to manage across byte lanes
tDQSCK – From JESD209-3

Figure 8 — Burst Read: RL = 12, BL = 6, tDQSCK > tCK

Figure 9 — Burst Read: RL = 12, BL = 6, tDQSCK < tCK

Global Standards for the Microelectronics Industry
tDQSCK - From JESD209-3

tDQSCK is 2500ps – 5500ps per JESD209-3

tCK is 1250ps at DDR1600

First rising edge of DQS can arrive between 2 and 4.4 clocks after RL elapses (practically, 2, 3, or 4 clocks)

Need DQ Calibration to determine where it arrives

tDQSCK delta parameters describe drift in tDQSCK
DQ Calibration (Read training) – System Level

- DQ Calibration algorithm reused from LPDDR2
- Data **optionally** returned per bit
  - Training data can appear on select bits or all bits. Should your system require per bit?
  - Remind package/PCB designers that DQ0, DQ8, DQ16, DQ24 are significant
- Decide if CPU, MemCtl, or PHY levels
- Can use DRAM for custom algorithms
DQ Calibration from JESD209-3

Figure 39 — DQ Calibration Timing
Write Leveling – System level

- Aligns Write DQS to CLK
- DFI mode can assist with leveling
- Enter with MRW
- Send DQSs – DRAM responds with DQ to indicate if DQS is received before or after CLK
- How Often? When to train?
- Where to train: CPU, Controller or PHY?
Write Leveling from JESD209-3

Figure 46 — Write Leveling Timing
ODT – System Level

• 2 Rank Package:
  – Always terminate on Rank 0
  – Cannot have Rank 0 in self-refresh while accessing Rank 1

• Single Rank
  – Can pull ODT high
  – Must use MRR to disable ODT for ZQ Calibration
### CMD-CMD Timing in LPDDR3

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LPDDR3</th>
<th>LPDDR2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read Latency</td>
<td>3-12</td>
<td>3-8</td>
</tr>
<tr>
<td>Write Latency</td>
<td>1-6, 1-9 opt</td>
<td>1-4</td>
</tr>
<tr>
<td>tWR min</td>
<td>Up to 12 nCK</td>
<td>Up to 8 nCK</td>
</tr>
<tr>
<td>tRP min</td>
<td>Up to 22 nCK</td>
<td>Up to 13 nCK</td>
</tr>
<tr>
<td>tRC min</td>
<td>Up to 53 nCK</td>
<td>Up to 36 nCK</td>
</tr>
<tr>
<td>tRAS min</td>
<td>Up to 34 nCK</td>
<td>Up to 23 nCK</td>
</tr>
<tr>
<td>tCCD min</td>
<td>4 clocks</td>
<td>2 Clocks</td>
</tr>
<tr>
<td>tFAW min</td>
<td>Up to 40 nCK</td>
<td>Up to 27 nCK</td>
</tr>
</tbody>
</table>

Don’t forget to plan for future expansion…

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Global Standards for the Microelectronics Industry
8n Prefetch in LPDDR3

- LPDDR2 has 4n Prefetch
  - Burst lengths 4, 8, 16 supported
- LPDDR3 has 8n Prefetch
  - Burst length 8 only and no BST/Interrupt
  - Minimum 32 Byte burst on X32 DRAM

- System-level effect:
  - OK for most CPUs
  - Consider video and network traffic
Chip Construction

- Need to plan for CA bus being on opposite edge from the data bus
- Two possible methods:
  - Place Memory Controller centrally and flop long paths on chip if necessary
  - Place Memory Controller at edge and route using package layers
Central Memory Controller placement

- Align pads with LPDDR3 ballout
- Flop long paths internally
  - Adds latency

Note: Only one channel shown. Not to scale.
Edge Memory Controller placement

- Produce compact layout for memory controller & PHY
- Route long paths in package layers

Note: Only one channel shown
Conclusions

- LPDDR3 requires many changes from DDR3 or LPDDR2
- Remember Training, ODT, and Capacitance
- Consider Design IP for your next project
About Cadence

- Cadence Memory Solutions include:
  - LPDDR3/LPDDR2/DDR4/DDR3 Controller and PHY
  - Wide-IO Controller and PHY
  - Flash Controller and PHY
  - Memory Models
  - Verification IP
  - Signal Integrity Reference Designs
  - Design, Verification, Physical Verification, and Test tools for TSV-based chip designs