High speed AND low power DDR DRAM? Let’s do it with LPDDR4X!

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LPDDR4/4X Introduction

• LPDDR4 standard JESD209-4 published August 2014
  – Revised Feb 2017 to JESD209-4B
  – Data rates up to 4266Mt/s

• LPDDR4X standard addendum JESD209-4-1 published Jan 2017
  – reduces I/O Buffer voltage from 1.1v to 0.6v

• In the DDRx world, we are accustomed to achieving higher speed with higher voltage. Can we meet the speed with LPDDR4X?
# Feature Comparison

<table>
<thead>
<tr>
<th></th>
<th>LPDDR3</th>
<th>LPDDR4</th>
<th>LPDDR4X</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd1 (Core 1 power)</td>
<td>1.8v</td>
<td>1.8v</td>
<td>1.8v</td>
<td>2.5v (Vpp)</td>
</tr>
<tr>
<td>Vdd2 (Core 2 power / Input buffer power)</td>
<td>1.2v</td>
<td>1.1v</td>
<td>1.1v</td>
<td>1.2v</td>
</tr>
<tr>
<td>Vddq (I/O buffer power)</td>
<td>1.2v</td>
<td>1.1v</td>
<td><strong>0.6v</strong></td>
<td>1.2v</td>
</tr>
<tr>
<td>Max data rate per current standard</td>
<td>2133Mt/s</td>
<td>4267Mt/s</td>
<td>4267Mt/s</td>
<td>3200Mt/s</td>
</tr>
</tbody>
</table>

- LPDDR4x reduced IO buffer voltage saves $V^2/R$ power
LPDDR4/4X Markets - Mobile

• Battery-operated mobile devices are the primary market for LPDDR
• LPDDR4X is already shipping in high-end phones*
• System requirements:
  – Occasional use at very high data rates
  – low power in moderate use
  – extended standby power

(source*: http://www.techinsights.com/technology-intelligence/overview/latest-reports/samsung-18-nm-dram-analysis/)
LPDDR4 Markets - Consumer

- “Smart Screen” applications
- Tablets based on mobile devices
- VR/AR
- Cameras, displays, TV

System Requirements:
- Memory Bandwidth
- Cost
LPDDR4 Markets - Automotive

- ADAS and Autonomous Driving control
- Processing sensor data
- System requirements:
  - High reliability
    - ASIL Certification
    - In-line ECC function
  - High temperature
    - AEC Q100 Certification
  - High data rates up to 4266
LPDDR4X Interface General Requirements

• Achieve high data rate
  – up to 4266MT/s

• Achieve high memory efficiency
  – 80%, 90% or more bandwidth

• Reduce memory power
  – Effective use of memory bank structure
  – Effective use of LPDDR low-power modes
  – Frequency change protocols
  – Low-power DDR Controller and PHY
Finding power savings in LPDDR4X

- Power savings are in the SoC LPDDR4X I/O and in the LPDDR4X DRAM device.
LPDDR4X Power Savings

• Expected on memory side: LPDDR4X 15-20%* Power Saving compared to LPDDR4
  – Power savings greatest in read/write mode
  – Little if any power saving in standby (powerdown, self-refresh)

*Sources:
https://www.mediatek.com/blog/the-benefits-of-using-lpddr4x
LPDDR4X PHY and I/O Power Savings

47% IO Power Reduction

47% Savings for I/O write power
4267MT/s, Typical conditions
100% activity, 50% switching 1100

I/O is about 30% of (PHY+IO) power
so generally we are expecting about
15% reduction in write power of
LPDDR4X PHY compared to
LPDDR4

SoC – CPU - ASIC

LPDDR4 Controller
LPDDR4 PHY
LPDDR4 I/O

LPDDR4/
LPDDR4X
DRAM
device
16nm testchip Test Board
Design Margin – LPDDR4X vs LPDDR4

- LPDDR4X-4267
- Quad Die Package
- Memory Down
- TT, Nominal

- LPDDR4-4267
- Quad Die Package
- Memory Down
- TT, Nominal
- Stretched to same scale
Conclusions

• LPDDR4X can be used as lower power replacement for LPDDR4 in most applications where the PHY is designed for 0.6v LPDDR4X I/O voltage
• Industry expectation for 15%-20% LPDDR4X memory power reduction on read
• Cadence data shows ~15% LPDDR4X PHY power reduction on write
• Cadence testchips for LPDDR4/LPDDR4X combo PHY and controller are fully characterized for 4266MT/s operation in multiple technologies