Transitioning from e-MMC to UFS: Controller Design

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Agenda

- eMMC vs. UFS
- Flash Trend & Challenges
- Key Requirements for Embedded Controller Design
Common Memory Interface

**Today**

- System
  - DRAM
  - NAND
  - eMMC
  - SD card

  ~50MB/s

**UFS**

- System
  - DRAM
  - UFS

- NAND
  - UFS
  - UFS Controller

V1 ~ 300MB/s, V2 ~ 600MB/s
NAND Organization Trend

- Larger page sizes improves sequential throughput.
- More pages per block affects random write performance.
Embedded vs. Consumer Applications

- Requirements for embedded applications are different than typical consumer applications in several ways
  - Higher density
    - More die
  - Faster random operations
    - Page-based block management
    - DRAM cache?
    - Faster/More I/O channels
    - Multiple ECC engines
    - Simultaneous operations
  - Better endurance and reliability
    - Stronger ECC
    - FSP
  - More consistent use over time
    - Balanced block management to reduce write amplification
8LC (TLC) Normal Read Thresholds

After Program

MSB Thresholds

LSB Threshold

CSB Thresholds
Using the same set of thresholds before and after EW cycling and/or retention may not be a good idea.
Reliability Challenges

BER equalized $V_{th}$

Equally spaced $V_{th}$
Flash Signal Processor (FSP)

- Adaptive read threshold positioning
- Adaptive program lobe positioning
- Efficient management of threshold history
- Adjustable programming speed/accuracy
- Randomizer to reduce interference
- Parameters of different flash regions
Solutions for Handling Flash Reliably

- NAND Technologies
- SLC/MLC/TLC
- Applications
- Consumer
- Embedded
- ...

Design Management
- FSP (Flash Signal Processing)
- ECC
- Advanced Firmware Algorithm

Technology & Trend

Delivery
- Reliability
- Endurance
- Performance

Flash Storage Summits 2010
Recycling/Garbage Collection

- The process of removing invalid blocks in flash to create empty blocks to write to
- It’s better to steal flash bandwidth from the host (background garbage collection)
- Blocks should be chosen wisely
  - Should take into account both free space and cycle counts for Wear leveling
    - TRIM command helps in space domain
    - Real Time Clock may help in time domain
Effective Wear-leveling

- Global wear-leveling
  - Balance block usage over space domain
- Static wear-leveling
  - Balance block usage over time domain
  - may increase write amplification factor and hence
    - kill flash life
    - lower down performance if it’s not managed appropriately

Note: Write Amplification Factor = \( \frac{\text{FlashWrite}}{\text{HostWrite}} \)
Endurance vs. Random IOPS

- Lower Write Amplification Factor
- Fewer NAND Cycle
- Faster Write Performance
- High Random IOPS ~ Endurance Efficiency
Power Cycling Complicates Memory Management

• Protect User's Data
  – Guaranteeing data integrity is a MUST
    • TLC much harder than MLC
  – Required in embedded applications
    • Previously written data
    • Data in flight

• Advanced Error Recovery Techniques are needed
  – Full Map resident in Flash
  – Cache full map in SRAM/DRAM
  – Cache partial map in DRAM
  – Upload to host
Power Management

• To control max power
  – Ration power among active flash die and controller

• Smart state based power management
  – PHY power management
  – In general, a trade-off between
    • power consumption
    • wake-up latency
eMMC/eUFS are differentiated by optimizing for different flash devices and applications
- Should be achieved through manufacturing time customizations
- Firmware and MP tool must be flexible enough to fulfill different requirements
Putting It All Together

- Reliability
- Performance
- Endurance
- Flexibility
- Power Consumption

Key embedded attributes that make things great

- FSP
- Advanced Firmware Algorithm
- ECC

eMMC/ UFS Controller
NAND

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