Server Memory Trends (Past and Future)

Server Memory Forum 2011
Memory Requirement for Server Application

- High End - DB server
- Mid End - Application server
- Front End - Web server

HPC/ MC
- In-Memory System
- TeraByte System
- Large Capacity

Conventional
- Virtualization & Consolidation
- Moderate Capacity / Low TCO
- High Bandwidth / Scalability

Cloud computing - Low End
- Small Form-Factor
- ECC SODIMM / MiniDIMM
- Scalability / Low Power

Memory requirements are getting more diversifying, so important to figure out the right solution for each segment together.

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Clouding Impact on GB/ system Forecast

- Clouding, requires More Memory in Server / Slowing Down of Density in PC but may increase # of systems

Driving Factor Cloud computing

High Density Requirement of Server Memory will increase

[Source: DQ 1Q'11]
Ever Green Memory Solution for Server

- Samsung keeps the same total power budget even though GB/system keeps growing.
  - Technical evolution: TSV, DDR4, Process migration, Low-voltage etc.
Server Memory Evolution Path: Type

- ECC UDIMM (Unbuffered DiMM)
- RDIMM (Registered DiMM)
- FBDIMM & LRDIMM (Load Reduced DiMM)

Cost / Density / Reliability / Speed

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Server Memory Evolution Path: SI

Low Frequency Module

SDR DRAM Module

33MHz clock

100MHz clock

100MHz clock

200MHz clock
Server Memory Evolution Path: SI - Cont’

- DDR2-400
- DDR2-800
- DDR3-800
- DDR3-1600

DDR4 Adopts Fly-by
## Server Memory Evolution Path: SI - Cont'

### Diagram:

- **DDR1**
  - Z₀ = 60 ohm
  - 22 ohm
  - Z₀ = 50~60 ohm
  - 15~25 ohm

- **DDR2/3 or 4**
  - Z₀ = <60 ohm
  - 15~22 ohm
  - Z₀ = 40~50 ohm

### Table:

<table>
<thead>
<tr>
<th></th>
<th>DDR1</th>
<th>DDR2</th>
<th>DDR3</th>
<th>DDR4</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>2.5V</td>
<td>1.8V</td>
<td>1.5V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Slot #</td>
<td>4-Slot</td>
<td>2-Slot</td>
<td>2-Slot</td>
<td>2-Slot</td>
</tr>
<tr>
<td>Cio</td>
<td>~ 5pF</td>
<td>~ 3pF</td>
<td>~ 2pF</td>
<td>~1.xpF</td>
</tr>
<tr>
<td>Threshold (AC/DC)</td>
<td>310/150</td>
<td>250(200)/125</td>
<td>175(150)/100</td>
<td>TBD</td>
</tr>
<tr>
<td>Termination</td>
<td>MBT</td>
<td>ODT</td>
<td>2 ODTs</td>
<td>3 ODTs</td>
</tr>
<tr>
<td>DRAM ODT</td>
<td>N/A</td>
<td>150/75/50</td>
<td>120/60/40/30/20*</td>
<td>TBD</td>
</tr>
<tr>
<td>MCH ODT</td>
<td>Optional</td>
<td>Support</td>
<td>Support</td>
<td>Support</td>
</tr>
</tbody>
</table>

- Speed ↑
- Voltage ↓
- # of Slot ↓
- Cio ↓
- Threshold ↓
- ODT ↓

*Dynamic ODT support*
## DDR4: Server Oriented Solution

- DDR4 is the first device which adopts proposals from “Server Union”

<table>
<thead>
<tr>
<th>Category</th>
<th>DDR4 Features</th>
<th>DDR3 Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Capacity</strong></td>
<td>DDR4: Max 24Ranks/ch</td>
<td>DDR3: Max 8Ranks/ch</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>DDR4: POD (-40% IO Power), 0.5KB page (-10% core power), 3DS (-25% Overall Power)</td>
<td>DDR3: 3DS</td>
</tr>
<tr>
<td><strong>Reliability</strong></td>
<td>DDR4: CRC/CA Parity/MPR,MRS Readout</td>
<td>DDR3: -</td>
</tr>
<tr>
<td><strong>Performance</strong></td>
<td>DDR4: Fine Granularity Refresh, Temp controlled Refresh</td>
<td>DDR3: -</td>
</tr>
</tbody>
</table>
DDR4: Server Oriented Solution – Cont'

Power

[Samsung calculation @ Same process node]

Capacity/Performance

[1DIMM/ch]

[2DIMM/ch]

[3DIMM/ch]

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**DDR4 : Server Memory for 2013**

- DDR4 cannot be delayed for Server Memory Differentiation

<table>
<thead>
<tr>
<th></th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
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<tbody>
<tr>
<td>Process</td>
<td>40nm</td>
<td>30nm</td>
<td>20nm</td>
<td>20’nm</td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>32GB RDIMM 16GB RDIMM @ 2DPC</td>
<td>32GB LRDIMM 16GB LRDIMM @ 3DPC</td>
<td>←</td>
<td>32GB RDIMM 16GB RDIMM @ 3DPC</td>
<td>←</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>1066Mbps</td>
<td>1600Mbps</td>
<td>1866Mbps</td>
<td>←</td>
<td>2133/ 2400Mbps</td>
</tr>
<tr>
<td>Power</td>
<td>1.35V</td>
<td>1.25V</td>
<td>←</td>
<td>1.2V</td>
<td></td>
</tr>
</tbody>
</table>

**DDR3L**  **DDR3U LRDIMM**  **DDR3-1866 (TSV)**  **DDR4**

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DDR4 is On Track

- Samsung verified DDR4 interface @ Jan’11
- Working Sample compatible to the latest JEDEC spec is successfully under evaluation
- DI MMM Characteristics (@ATE, 1DI MM/ ch)

<table>
<thead>
<tr>
<th>Max Freq. ~3.33Gbps</th>
<th>Sufficient Data Rx Eye @ 2.6Gb/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD 500ps 750ps 1000ps 1250ps 1500ps</td>
<td></td>
</tr>
<tr>
<td>1.50V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.45V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.40V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.35V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.30V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.25V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.20V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.15V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.10V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.05V</td>
<td>*****************************************</td>
</tr>
<tr>
<td>1.00V</td>
<td>*****************************************</td>
</tr>
</tbody>
</table>

Data Rate 3.33Gb/s at VDD=1.1V
### DDR3 vs DDR4 Module

#### Changes

<table>
<thead>
<tr>
<th>No</th>
<th>Item</th>
<th>DDR3</th>
<th>DDR4</th>
<th>Change</th>
<th>Objectives</th>
<th>Note*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DIMM Pin Count (Pin Pitch)</td>
<td>240 pin (1.0 mm)</td>
<td>284 pin (0.85 mm)</td>
<td>+ 44 pins (- 0.15 mm)</td>
<td>SI (XTK) S/G ratio ↑</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>204 pin (0.6 mm)</td>
<td>256 pin (0.5 mm)</td>
<td>+ 52 pins (- 0.1 mm)</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>PCB Bottom Edge</td>
<td>Flat</td>
<td>Step &amp; Ramp</td>
<td>Step</td>
<td>Insertion force ↓</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>3</td>
<td>DIMM Width</td>
<td>67.6 mm</td>
<td>68.6 mm</td>
<td>+ 1.0 mm</td>
<td>Number of pin ↑</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>DIMM Height</td>
<td>30.35 mm</td>
<td>31.25 mm</td>
<td>+ 0.9 mm</td>
<td>DIMM routing ↑</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>5</td>
<td>DIMM Thickness</td>
<td>1.0 mm</td>
<td>1.2 mm</td>
<td>+ 0.2 mm</td>
<td>Number of layers ↑</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>Data Buffer</td>
<td>1 Buffer</td>
<td>9 Buffers</td>
<td>+ 8 Buffers</td>
<td>SI (Stub)</td>
<td>1</td>
</tr>
</tbody>
</table>

#### No change
- DRAM Ball Count (78/ 96 balls) & Ball Pitch (0.8 mm)
- DIMM Topology (Fly-by CA)

* Note
1. LRDIMM
2. RDIMM
3. UDIMM
4. SO-DIMM

[JEDEC Logo]

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TSV: Another Hook for DDR4 Server Solution

- Can achieve High Performance & Low Power & High Density
  - More stacking → High Density with less electronic loss
  - Master-Slave enables High performance/Low Power

- High Cost is the Challenge to overcome
  - Key bottleneck: Thin wafer/die handling, Drilling/Filling/Align

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TSV: Another Hook for DDR4 Server Solution

- 2H-TSV has been verified in several Modules in DDR3
- Confirmed 3DS Architecture & Power Saving & Performance Increase in Actual System level
- DDR4 supports 3 Chip ID which enables Max 8H-stack
  - 2H-TSV will be real Soon but 4H will need more patient for production within reasonable cost

>30% Power Save over LRDIMM @ 2DPC

Global Standards for the Microelectronics Industry
DDR4 Micro-server Solution

• Current : Various Small Form Factor Solution in DDR3

<table>
<thead>
<tr>
<th>MDL type</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECC SODI MM</td>
<td>67.8x30 2028mm²</td>
</tr>
<tr>
<td>VLP ECC UDIMM</td>
<td>133.35x18.75 2500mm²</td>
</tr>
<tr>
<td>Mini DIMM</td>
<td>82x17.9 1469mm²</td>
</tr>
</tbody>
</table>

• DDR4 : ECC SoDI MM might be the most feasible one
  • VLP/ Mini DI MM may face Routing/ SI issue in DDR4 speed (More CA, VPP)
  • ECC SoDI MM will be more popular than DDR3
Summary & Call For Action

• Server, Ever Hungry for High Density with Low Power
  – DDR4, Adopted VOC of Server from Spec definition

• Server, Need DDR4 from 2013 for Memory Differentiation
  – Cannot be delayed to keep Server GB/sys with same power budget

• TSV in Server will become real with 2H-TSV/DDR4
  – Industry may need more patient for 4H-TSV
THANK YOU!