Techniques for Verification and Debugging of LPDDR3 Memory Designs

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Tektronix

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Agenda

- LPDDR3 Key Feature Review
- Signal Integrity Considerations
- Debugging Techniques
- Signal Access & Probing
- JEDEC-Specific Test Practices
- What’s Next/Summary
Mobile Memory = Faster, Smaller, Less Power

LPDDR3 Key Features

- Speed and Capacity
  - Bandwidth of 6.4 – 8.5 Gbps per die
  - LPDDR3 achieves a data rate of 1600 Mbps (vs. 1066 Mbps for LPDDR2)
- 4, 8, 16, 32Gb Package Options
- Battery Conservation
  - Low Voltage (300mV – 1.2V MAX)
  - Voltage Ramp and Device Initialization
    - Temperature-compensated and partial array self refresh modes
    - Deep power down mode which sacrifices all memory contents
- Compact Packaging
  - PoP and Discrete Packages
LPDDR3 Specification

Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR:
- 1.8 V
- 200MHz

Diagram showing signal levels and timing:
- DDR Ref Level Designations:
  - $V_{IH\,(ac)\,\min}$
  - $V_{IH\,(dc)\,\min}$
  - $V_{REF\,(dc)}$
  - $V_{IL\,(dc)\,\max}$
  - $V_{IL\,(ac)\,\max}$

- DP0JET Ref Level Designations:
  - High (Rise)
  - High (Fall)
  - Low (Rise)
  - Low (Fall)
LPDDR3 Specification

Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR2:
- 1.2 V
- 533MHz
LPDDR3 Specification

Pushing the system power envelope

- Lower operating voltage and higher bandwidths
  - Measurement Challenge

LPDDR3:
- 1.2 V
- 800MHz
LPDDR3 Specification

Faster Clock Frequencies

- Verifying Clock Cycles on shorter (1.25 ns) Clock Periods
  - Measurement Challenges: Do I have the right instrument settings to capture with proper margin?

11.4 LPDDR3 Read and Write Latencies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Clock Frequency</td>
<td>166</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>400</td>
<td></td>
</tr>
<tr>
<td></td>
<td>533</td>
<td></td>
</tr>
<tr>
<td></td>
<td>600</td>
<td></td>
</tr>
<tr>
<td></td>
<td>667</td>
<td></td>
</tr>
<tr>
<td></td>
<td>733</td>
<td></td>
</tr>
<tr>
<td></td>
<td>800</td>
<td></td>
</tr>
<tr>
<td>Max. Data Rate</td>
<td>333</td>
<td>Mbps</td>
</tr>
<tr>
<td></td>
<td>800</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1066</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1200</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1333</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1466</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1600</td>
<td></td>
</tr>
<tr>
<td>Average Clock Period</td>
<td>6</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.875</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.67</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.36</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.25</td>
<td></td>
</tr>
<tr>
<td>Read Latency</td>
<td>3</td>
<td>t CK(avg)</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Write Latency</td>
<td>1</td>
<td>t CK(avg)</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1  RL=3/WL=1setting is an optional feature. Refer to supplier’s Mode Register 2 settings.
**Recommended Oscilloscopes for LPDDR2/3**

- LPDDR2/3 Depending on Error Tolerance Levels
  - 8GHz (MSO70804C)
  - 12.5GHz (MSO71254C)

<table>
<thead>
<tr>
<th>Metric</th>
<th>LPDDR2</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max SE Slew Rate (V/ns)</td>
<td>3.5</td>
<td>4</td>
</tr>
<tr>
<td>Typical Clock Rate (MHz)</td>
<td>400</td>
<td>800</td>
</tr>
<tr>
<td>Period (ns)</td>
<td>2.5</td>
<td>1.25</td>
</tr>
<tr>
<td>Rise Time, 10% - 90% (ps)</td>
<td>738</td>
<td>369</td>
</tr>
<tr>
<td>Tyyp. Signal Swing (V)</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>Min. Rise Time (ps)</td>
<td>229</td>
<td>200</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Scope BW (GHz)</th>
<th>T_r-scope (10% - 90%)</th>
<th>RT_{sig}</th>
<th>R_{total}</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>160</td>
<td>229</td>
<td>279</td>
<td>22%</td>
</tr>
<tr>
<td>3.5</td>
<td>145</td>
<td>229</td>
<td>271</td>
<td>18%</td>
</tr>
<tr>
<td>4</td>
<td>98</td>
<td>229</td>
<td>249</td>
<td>9%</td>
</tr>
<tr>
<td>6</td>
<td>65</td>
<td>229</td>
<td>238</td>
<td>4%</td>
</tr>
<tr>
<td>8</td>
<td>49</td>
<td>229</td>
<td>234</td>
<td>2%</td>
</tr>
<tr>
<td>12.5</td>
<td>32</td>
<td>229</td>
<td>231</td>
<td>1%</td>
</tr>
</tbody>
</table>

**Misc Notes:**
- For GDDR5, JEDEC doesn't specify a max slew rate. Instead, the actual 10%-90% risetime from some real interfaces was used.

Typical signal swing is subjectively estimated based on some actual signal samples.

Typical signal swing is subjectively estimated based on some actual signal samples.

Equation for calculating the risetime of a cascaded system (root sum of squares) is from Appendix B of "High Speed Digital Design: A Handbook of Black Magic" (Howard Johnson, Prentice Hall).

Typical signal swing is subjectively estimated based on some actual signal samples.
Signal Integrity

Accurate Read/Write Burst Identification

- Locate the right kind of bursts (read vs. write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc.)

DDR3 Read Burst

DDR3 Write Burst
Signal Integrity

Capture LPDDR3 Reads/Writes
Advanced Search and Mark (ASM) dynamically applies a search algorithm to each acquired waveform, and marks specific features with visual delimiters.

ASM searches have been developed specifically for DDR Reads and Writes.

User controlled parameters to fine tune search algorithm.

DDRA application can read these marks and use them as measurement gates.

Single trigger post-process analysis of all parameters.
Signal Integrity

Visual Trigger – DDR Eye Example

- Hexagon shaped area applied to DQ used as a keep-out zone to isolate only target rank of interest.
- Use additional areas to target specific DQ patterns.

Before

After w/Visual Trigger
Signal Integrity

Visual Trigger – Characterizing LPDDR3

• Quick evaluation of DQ Signals
Signal Integrity

Visual Trigger – Characterizing LPDDR3
LPDDR3 Specification

Efficient Messaging

- 10-bit Command Addressing Bus
  - Measurement Challenge: PHY decoding with 10+ address pins
LPDDR3 Command Bus Capture & Display

Tektronix Mixed Signal Oscilloscopes

- 16 Digital Channels in addition to 4 Analog Channels
- Ideal for Accurate LPDDR Command Bus Capture & Display

### TSF Format

<table>
<thead>
<tr>
<th>Type</th>
<th>File Radix</th>
<th>Version</th>
<th>PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command</td>
<td>Command</td>
<td>Pattern</td>
<td>CS, CA1, CA2, CAn</td>
</tr>
</tbody>
</table>

#### Command List

- MODE_REG: 0000
- REFRESH: 0001
- PRECHARGE: 0010
- ACTIVATE: 0011
- WRITE: 0100
- READ: 0101
- NOP: 0111
- DESELECT: 1XXX

![Tektronix Mixed Signal Oscilloscopes Image](image)
LPDDR3 Address Bus Capture & Display

Burst Detect Using Command Bus

- Using command bus state, specific transactions can be isolated
  - Analysis of analog signals is then used for fine burst positioning to gate measurements
LPDDR3 Specification

Smaller Packages, Greater Density

- Access to ball pads; especially PoP
  - Measurement Challenge: Ensuring consistent “observation point accuracy”
  - No back-side vias for many BGA designs
Signal Access & Probing

BGA Access Using Oscilloscope Interposers

- Unique, re-usable socket design allows for multiple chip exchanges
  - Signal paths and termination requirements are key and central to the designs
  - Modeling to predict analog performance
  - Oscilloscope filters to enable views with and without interposer circuit effects
Signal Access & Probing

PoP Interposer Assembly
## Signal Access & Probing

### LPDDR Interposer Support

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>LPDDR Support</th>
<th>Tektronix Oscilloscope</th>
<th>Tektronix Logic Analyzer</th>
</tr>
</thead>
<tbody>
<tr>
<td>60 Ball</td>
<td>LPDDR</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>POP 136</td>
<td>LPDDR2</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>POP 168</td>
<td>LPDDR2</td>
<td>Now</td>
<td></td>
</tr>
<tr>
<td>POP 216</td>
<td>LPDDR2</td>
<td>Now</td>
<td>In development</td>
</tr>
<tr>
<td>POP 240</td>
<td>LPDDR2</td>
<td>Now</td>
<td>In development</td>
</tr>
<tr>
<td>POP 220</td>
<td>LPDDR3</td>
<td>Now</td>
<td>In development</td>
</tr>
<tr>
<td>134 Ball</td>
<td>LPDDR2</td>
<td>Under Consideration</td>
<td></td>
</tr>
<tr>
<td>178 Ball</td>
<td>LPDDR3</td>
<td>In development</td>
<td>In development</td>
</tr>
<tr>
<td>253 Ball</td>
<td>LPDDR3</td>
<td>Under Consideration</td>
<td></td>
</tr>
</tbody>
</table>
LPDDR2/3 specification include unique measurements & methods

- Measurement Challenge: Ensuring consistent test practices without losing focus on performance

Table 10 — AC Timing (cont'd)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write leveling output delay</td>
<td>tWL0</td>
<td>MN</td>
<td>0</td>
<td>1533</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX</td>
<td>1681</td>
<td></td>
</tr>
<tr>
<td>Hold regime set command delay</td>
<td>tH0</td>
<td>MIN</td>
<td>max</td>
<td>VCC(t)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MAX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Deviation[2]</td>
<td>tVDDHS</td>
<td>MAX</td>
<td>1622</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>tVDDCL</td>
<td>MAX</td>
<td>930</td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td>tAH</td>
<td>MAX</td>
<td>1681</td>
<td>on</td>
</tr>
<tr>
<td></td>
<td>tAH0</td>
<td>MAX</td>
<td>1681</td>
<td>on</td>
</tr>
<tr>
<td></td>
<td>tAH0+</td>
<td>MAX</td>
<td>1681</td>
<td>on</td>
</tr>
<tr>
<td></td>
<td>tAH0-</td>
<td>MAX</td>
<td>1681</td>
<td>on</td>
</tr>
</tbody>
</table>

Some notes:
- Note 1: Propagation delay is reference only. Clock cycle time (t_Cyc) is used to determine device capabilities.
- Note 2: All AC timings assume a supply line delay of 50ns.
- Note 3: 2200Ω, VDD, and supply voltages are referenced to VSS.
- Note 4: Temperature deviation is based on the difference between two I/O port measurements (in two lines) within a contiguous sequence of boards in a 100% test window. Temperature deviation is not tested and is guaranteed by design. Temperature deviation in the system is +/-10°C. Values do not include clock skew.
- Note 5: Temperature deviation is the absolute value of the difference between two I/O port measurements (in two lines) within a 100% test window. Temperature deviation is not tested and is guaranteed by design. Temperature deviation in the system is +/-10°C. Values do not include clock skew.
- Note 6: 2200Ω, VDD, and supply voltages are referenced to VSS.
- Note 7: For GS1-GS4 and GS5-GS8, the line reference is in the point where the power source plus for GS1-GS4 and GS5-GS8 is located.
- Note 8: These values are not tested, because the signal distribution group is used in the test group, then the ordered reference level applies also here.
JEDEC Test Verification of LPDDR

DDRA Analysis Software

- Easily identify, mark & measure LPDDR Read / Write bursts
  - Uses Advanced Search & Mark feature
  - Uses Digital Channels (on MSO model scopes)
  - LPDDR JEDEC Measurements performed on ALL reads/writes
  - JEDEC Tests + Debug Tools
JEDEC Test Verification of LPDDR

DDRA Analysis Software
JEDEC Test Verification of LPDDR Support for Multiple DDR Generations

- DDRA = One Application SW Package
  - DDR
  - DDR2
  - DDR3
  - DDR3L (2H CY12 – 1H CY 13)
  - DDR4 (2H CY12 – 1H CY 13)
  - LPDDR
  - LPDDR2
  - LPDDR3 (2H CY12 – 1H CY 13)
  - GDDR3
  - GDDR5
JEDEC Test Verification of LPDDR

Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements

• Example measurements list for LPDDR2:

  • Read Write Bursts
    - Data Eye Width
    - Data Eye Height
  • Diff DQS Input
    - Slew-Diff-Fall (DQS)
    - Input-Slew-Diff-Rise (DQS)
    - tDHDiff (base)
    - tDHDiff (derated)
    - tDHDIFF (Vrefbased)
    - tDQS
    - tDQSL
    - tDSDiff(base)
    - tDSDiff(derated)
    - tDSDiff(Vrefbased)
    - tDSS-Diff
    - tDQSS-Diff
    - tDSH-Diff
    - tDQSKDiff
    - tDQSDiff
    - tAC-Diff
    - tQH
    - SRQdiff-Rise (DQS)
    - SRQdiff-Fall (DQS)

  • Single Ended DQS
    - Slew rate Hold-SEFall (DQS)
    - Slew rate Hold-SERise (DQS)
    - Slew rate Setup-SEFall (DQS)
    - Slew rate Setup-SERise (DQS)
    - Single Ended DQS (cont)
      - tDHSE (base)
      - tDHSE (derated)
      - tDSSE (base)
      - tDSSE (derated)
      - tDIPW-SE
      - tDQSS-SE
      - tDSS-SE
      - Slew Rate DQ
      - Slew Rate Hold-Fall (DQ)
      - Slew Rate Hold-Rise (DQ)
      - Slew Rate Setup-Fall (DQ)
      - Slew Rate Setup-Rise (DQ)
      - tWPRE
      - tWPST
      - tDQSCK-SE
      - tDQSO-SE
      - Slew Rate (DQ)
      - SRQse-Rise (DQS)
      - SRQse-Fall (DQS)
      - SRQdiff-Rise (CK)
      - SRQdiff-Fall (CK)
      - tRPRE
      - tRPST Clock (Diff)
      - tCH (abs)
      - tCH (ave)
      - tCK (abs)
      - tCK (ave)
      - tCL (abs)
      - tCL (ave)
      - tERR
  • Single Ended DQS (cont)
    - tERR
    - tJIT
    - tHP
    - VID (ac)
    - Input Slew Diff-Rise (CK)
    - Input Slew Diff-Fall (CK)
    - Clock (SE)
    - AC-Overshoot (CK#)
    - AC-Overshoot (CK)
    - AC-Overshoot Area (CK#)
    - Vix (ac) CK
    - Vox (ac) CK
    - VSWING (MAX) CK
    - VSWING (MAX) CK#
    - VSEH (AC) CK
    - VSEH (CK#)
    - VSEH (CK)
    - VSEL (AC) CK
    - VSEL (AC) CK#
    - VSEL (CK#)
    - VSEL (CK)
    - DQS (SE)
    - AC-Overshoot (DQS#)
    - AC-Overshoot (DQS)
    - AC-Overshoot Area (DQS#)
    - AC-Overshoot Area (DQS)
    - Vix (ac) DQS
    - Vox (AC) DQS
    - VSWING (MAX) DQS
    - VSWING (MAX) DQS#
    - AC-Overshoot
    - AC-Overshoot Area
    - AC-Undershoot
    - AC-Undershoot Area

Global Standards for the Microelectronics Industry
LPDDR Analog Verification & Debug Solution

- **Signal Access & Probing**
  - BGA Interposers
  - High BW Solder-in Probes
  - Digital Probing

- **DDRA Analysis SW**
  - LPDDR standards support
  - JEDEC conformance measurements
  - Advanced Debug Tools
    - Search & Mark
    - Visual Trigger
    - DPOJET

- **Mixed Signal Oscilloscopes**
  - Command Bus Triggering on CA0-CA9
  - Command Bus Timing Measurements
What’s Next?

- Tektronix (2H CY12 – 1H CY13)
  - LPDDR3 Interposers
  - DDRA Update

Resources Available

www.tek.com/technology/ddr
anshuman.bhat@tektronix.com