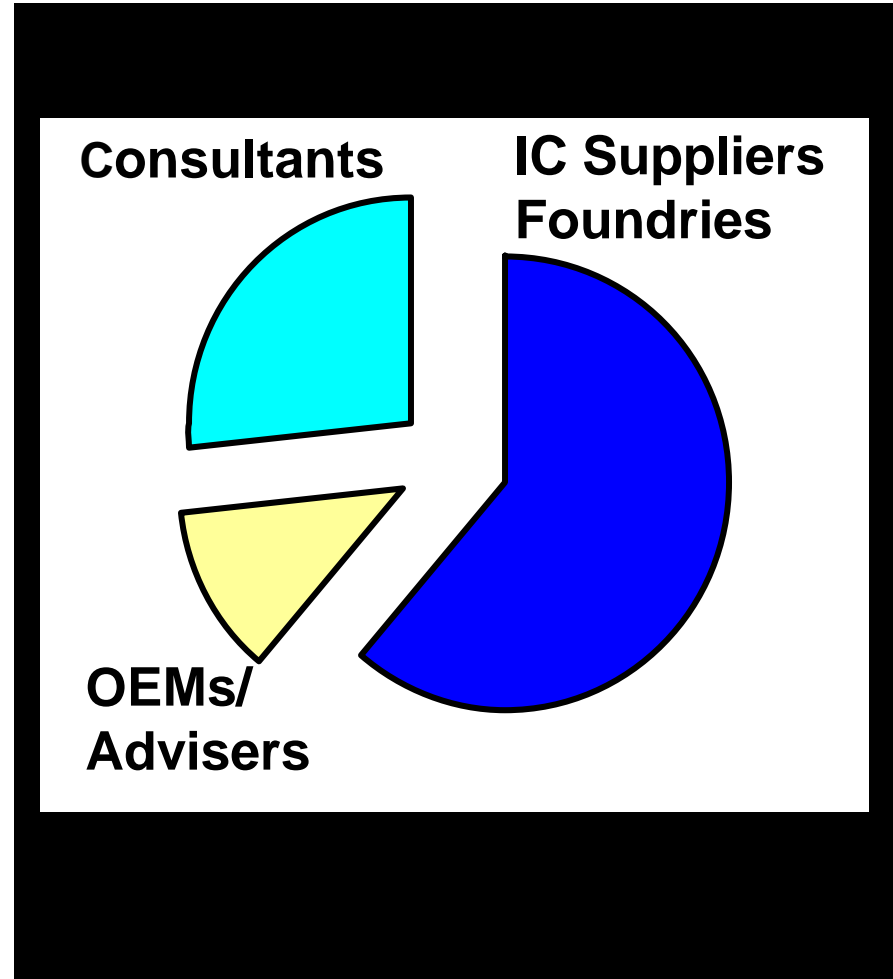
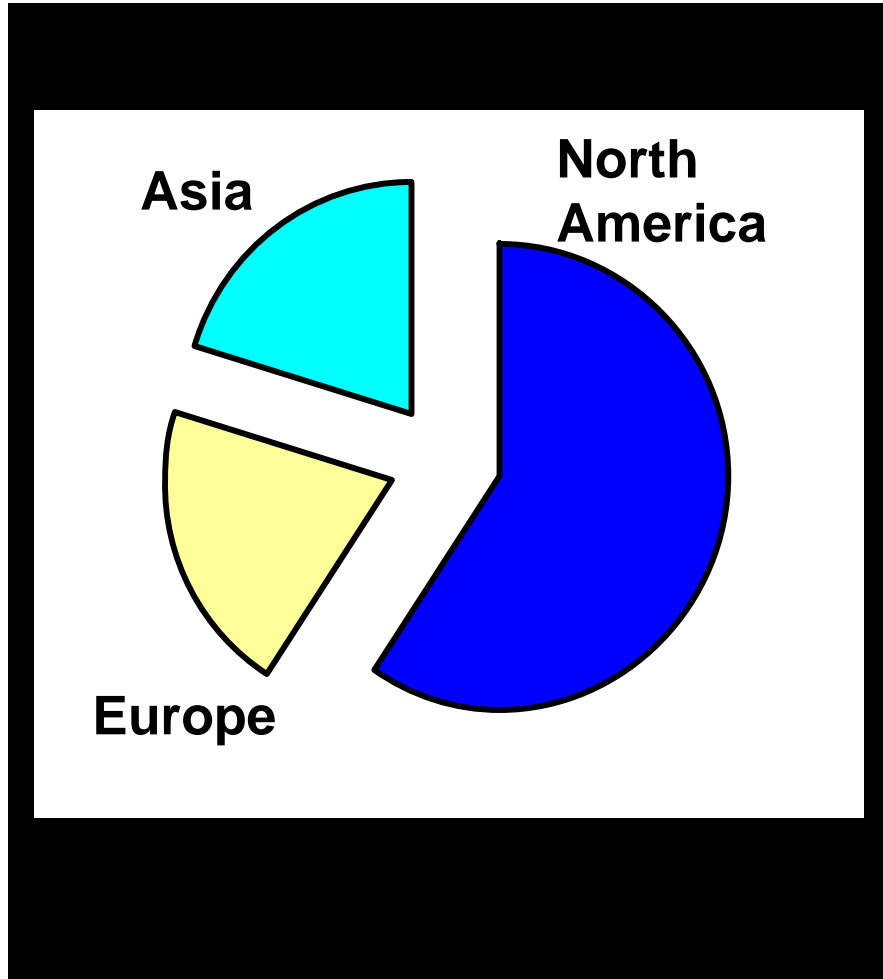


# **Human Body Model (HBM) Qualification Issues**

# Council Demographics and Details



# Contract Manufacturers and ESD Static

## Control Experts contributing to White Paper

	<b>Ron Gibson: 25+ years of ESD control</b>
	<b>Arnie Steinman: 25+ years of static control</b>
	<b>Ted Dangelmayer: 25+ years ESD Management</b> <b>Terry Welscher: 25+ years ESD management</b>
	<b>Dave Swenson: 30+ years of static control</b>
	<b>John Kinnear: 25+ years ESD control</b>
 Never stop thinking	<b>Reinhold Gaertner: 15+ years ESD control</b>
	<b>Jeremy Smallwood: 25+ years ESD training and consulting</b>

# The Story of ESD

- During late 1970s ESD started being a problem for advanced LSI
- ESD control programs were focused on
  - Risk from people
  - Protective packaging
  - Standards for control items
- ESD control standards
  - New and improved standards were developed in 1999
  - **By 2007 certification programs had been established to handle even 100V devices**

# The Story of ESD

- During the early years, the devices had relatively smaller number of pins and were assembled in uncontrolled environments
- Gradually, the number of device pins and the level of automation both increased
- More recently, with the better ESD control programs, **the likelihood of large amplitude HBM events dropped.**
- In addition, **many devices can now only be assembled with the use of automated manufacturing systems**

# The Story of ESD

- With increasing pin count, the number of protection devices, the area and the test complexity have all increased
- So when devices fail to meet the old target levels, the cost of redesign and delay have continuously increased
- **Therefore a reduction in ESD targets to practical but still safe levels would mean savings in cost, faster release to production, and improvements for device performance**

# Question

## **Why is the Industry Council pushing reduction of the component ESD levels now?**

- *It has been widely observed for almost 10 years that the current requirements, while nearly universally accepted by customers, have been over specified and that lower levels are very safe.*
- *As technology scaling continues and demands for even higher circuit performance prevail, it has become necessary that these specifications be reexamined and modified to realistically meet the current practices.*

# The Impetus for Change in ESD Targets

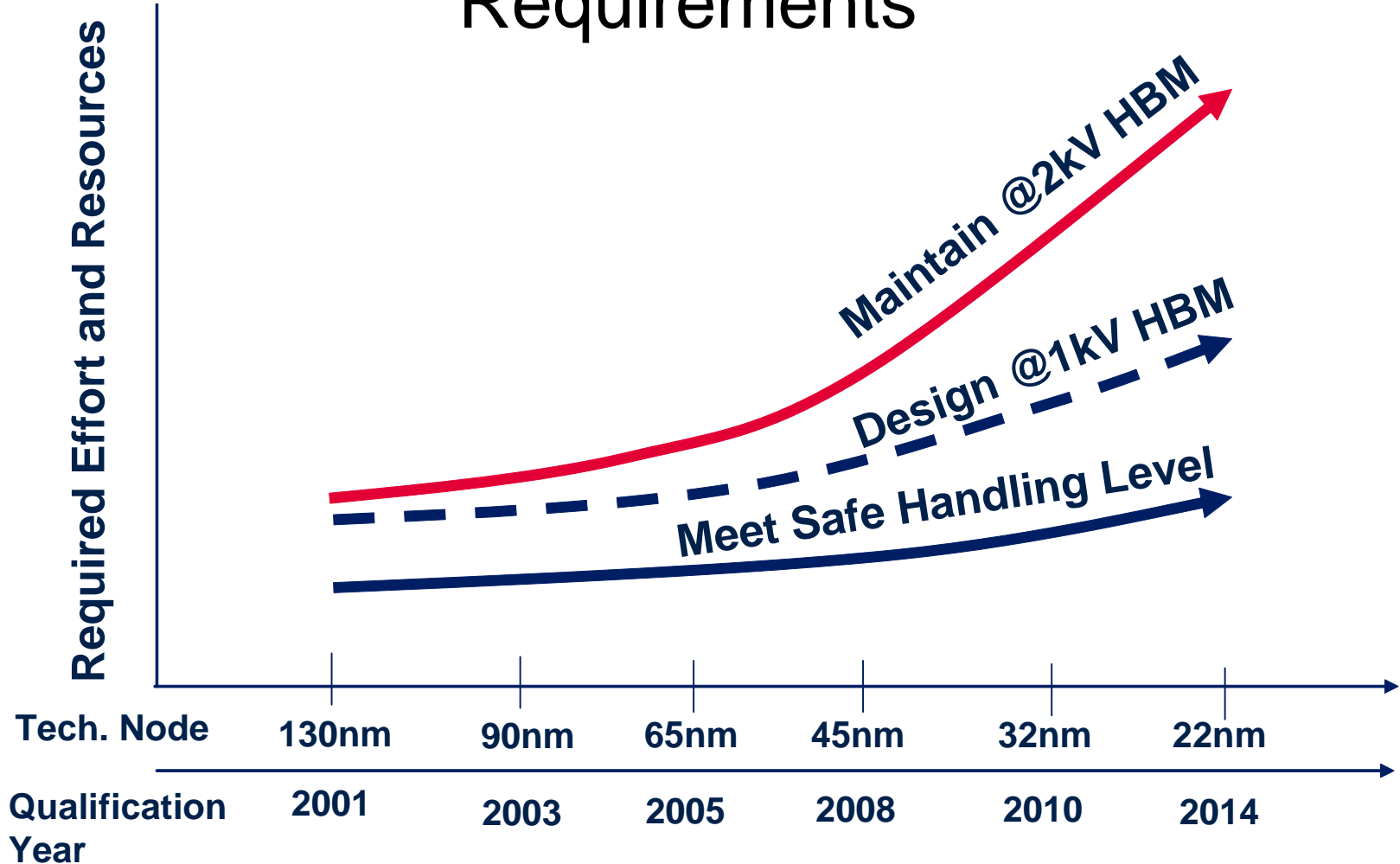
- Since 2003 there has been an increased awareness that many IC products are routinely failing ESD qualification
- This pattern was found to be consistent from company to company
- And while the associated cost of ESD has been mounting, **products shipped with lower than specification level ESD have not experienced higher field return rates**



# The Impetus for Change in ESD Targets

- At the same time the IC customers have been continuously demanding the same expected levels adding time-to-market delays
- In parallel, silicon technology scaling along with circuit demands for ever-increasing speed and performance all started to compound the ESD cost
- This “cost” is really an increased effort from the supplier that can result in delays in time to market as well as a negative impact on IC performance

# Challenge and Effort of Meeting ESD Level Requirements



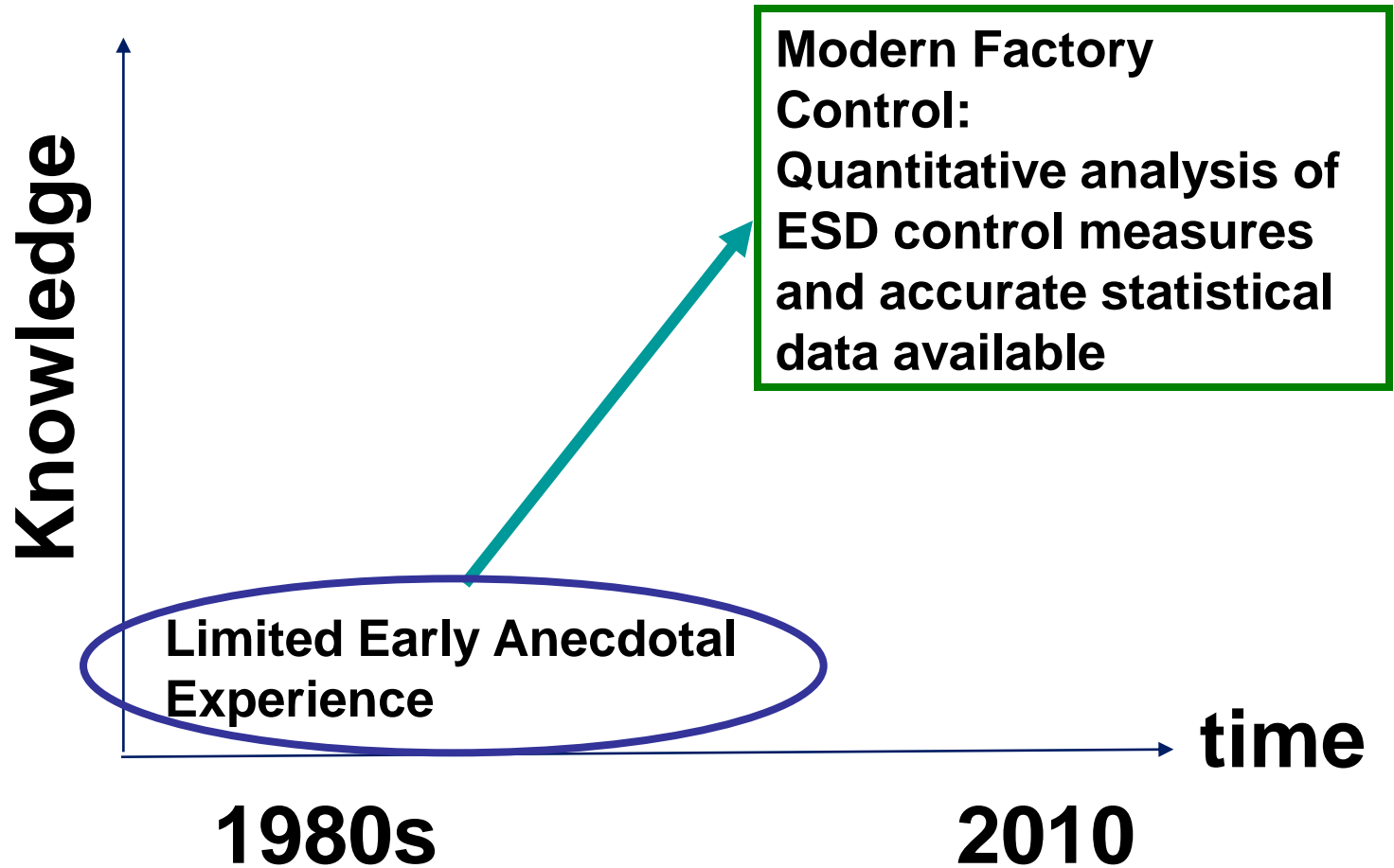
**Reducing to 1kV will alleviate a lot of ESD effort but as technologies are scaled down further the challenge will continue...**

# Question

**Is there an impact on factory control cost?  
Why should the OEM accept lower levels?**

- *From the experienced Contract Manufactures on the Council: “The recommended new safe lower levels have no impact on the cost of factory control”*
- *The improved knowledge in basic factory controls developed during the last 30 years supports the conclusion lower levels will lead to no additional manufacturing issues.*


# Increase of Knowledge in ESD Control



During the last 30 years the ESD control methods have vastly improved

# Basic ESD Control Program is just .....

①  
Grounding Person  
Wrist Strap to Ground  
(or flooring/footwear)

②  
Grounded Work Surface 

③ ESD Protective  
Packaging



# Basic ESD Control Program

- Avoid personnel charging and discharging into the device by **grounding personnel**
- Avoid discharges between different items by having them at the same potential, e.g. by using **ESD safe work surfaces**
- Use **ESD safe packaging materials** when removing devices from the ESD safe workplace

**Electronics manufacturers use at least this level across the globe, while most do more than this basic level.**

# Basic ESD Control Program

- If the bullets below are fulfilled, personnel will not charge to more than 100V.
- This means it is clearly safe to handle devices with an HBM robustness  $\geq 500V$  if:
  - Personnel are grounded through wrist straps or properly selected footwear/flooring systems
  - All work surfaces are grounded
  - ESD-safe Packaging Materials are used

**If these are not fulfilled, the control program has no meaning and even 2kV HBM devices may be in jeopardy.**

# Question

**Would basic ESD control methods be sufficient to tolerate 1kV to 500V HBM, or would one need special precautions?**

- *Basic ESD controls ensure that devices with a HBM robustness of at least 500V can be handled safely.*
- *With advanced ESD controls, such as the ANSI ESD S20.20 and IEC 61340-5-1, even devices with a HBM robustness of 100V can be safely handled with only a minimal incremental cost.*

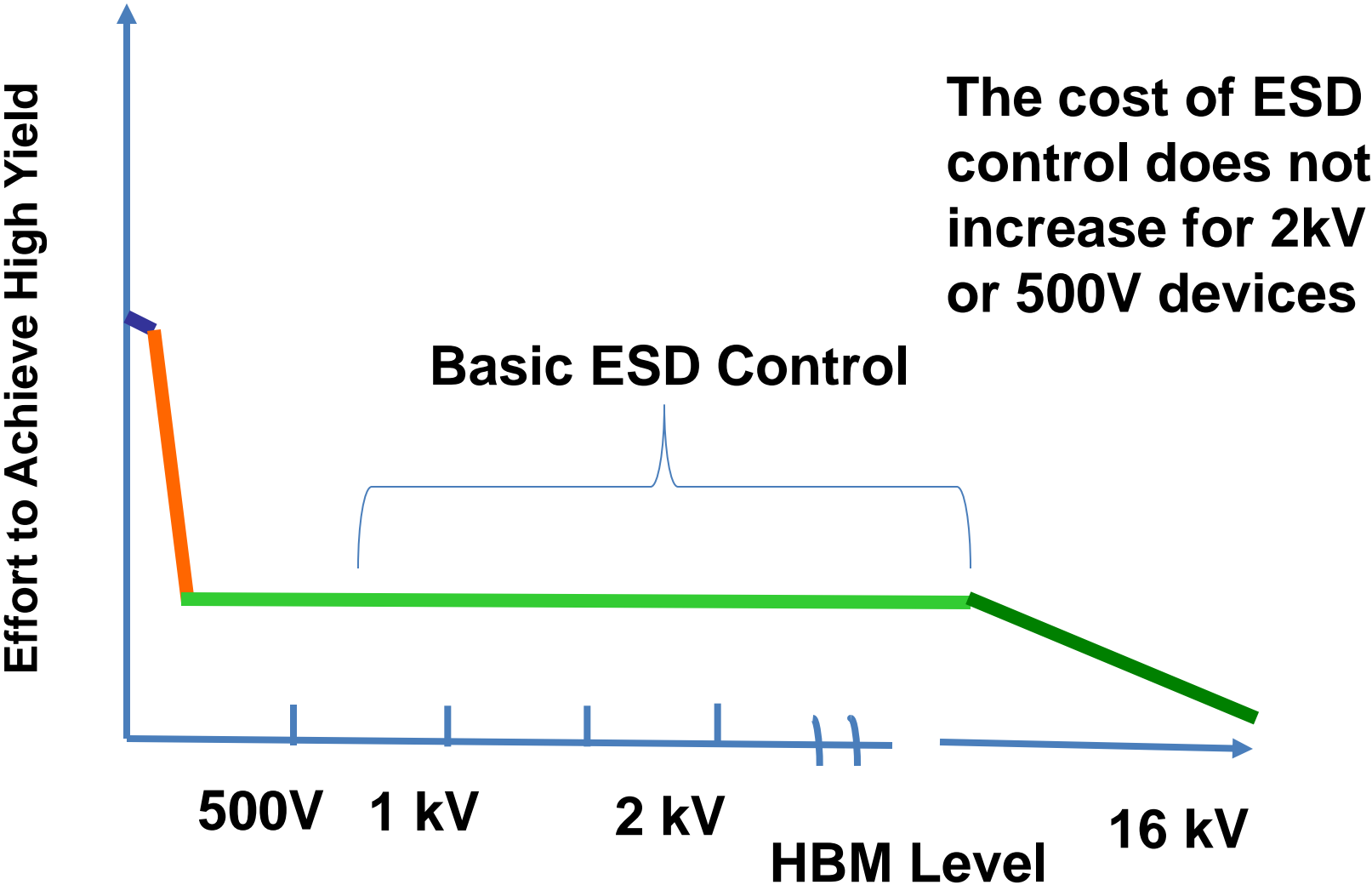


# Question

**We have a factory that has control program in place to handle 2kV HBM devices. If we now are to accept 1kV devices what shall we do?**

- *Nothing. If you are qualified for 2kV you are automatically qualified for 1kV devices. In fact, even also for 500V devices.*

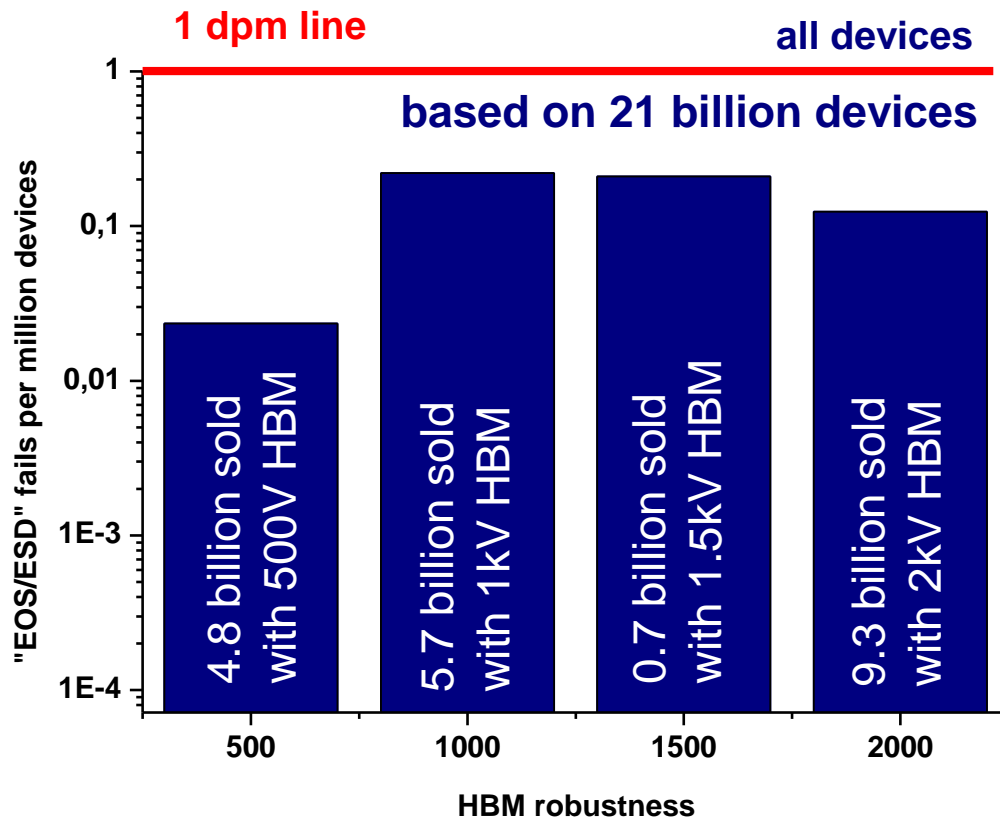
# Cost of ESD Control



# What is Basic Control?

- Any electronic manufacturer has to follow at least basic controls
- The basic program can be
  - Following one of the known standards
  - A customized in-house program following the basic control requirements
- With either of the above basic programs, 1kV HBM devices are safe and require no additional precautions
- Variations in the basic programs for different production areas is of no concern in the change from 2kV to 1kV HBM
- Vast amounts of industry data for the last 10 years supports the conclusion that even 500V HBM devices are safe if the basic program is followed

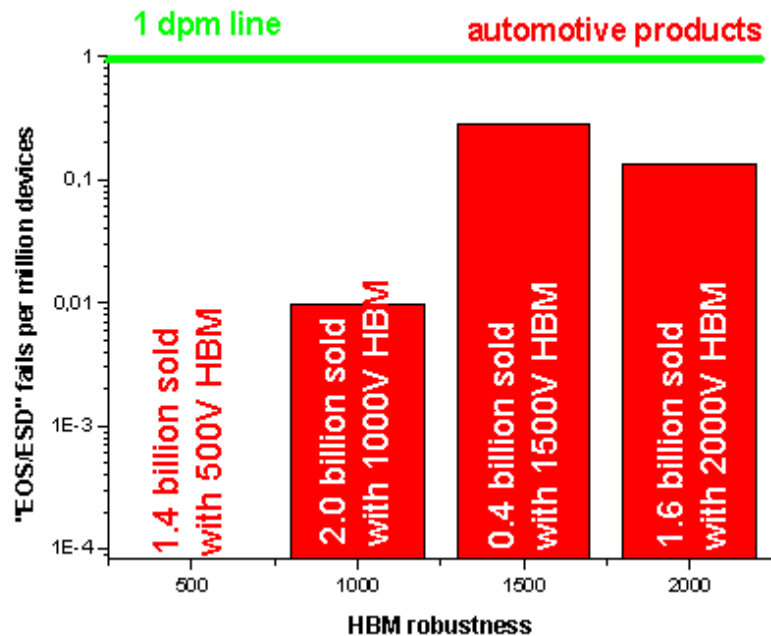
# Data on 21 Billion Products Shipped Worldwide With Basic ESD Control



- ESD/EOS failures as provided by various members of the Industry Council
- Includes both automotive products and consumer ICs
- A vast majority of the returns are often found to be due to EOS
- Total return rate due to EOS/ESD fails < 1 dpm
- **No obvious correlation of EOS/ESD returns to HBM levels between 500 V and 2 kV**

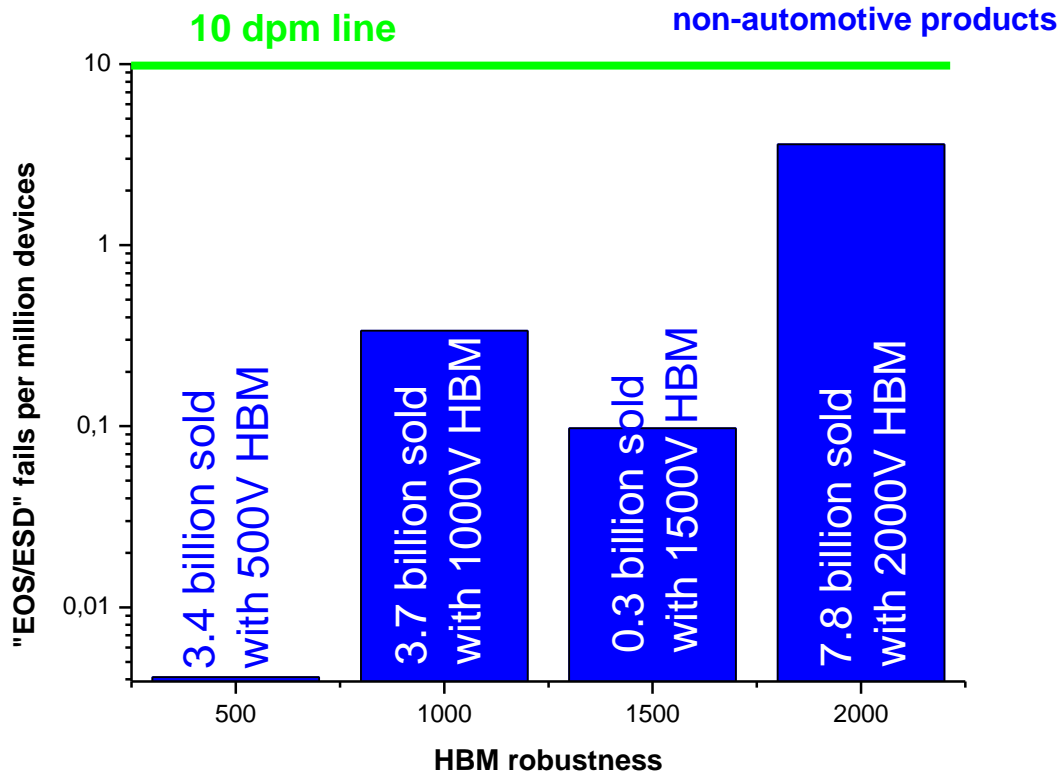
**This data represents products shipped at various ESD levels handled with the same basic factory control measures**

# Data Exclusively on Automotive Products



- Consolidated data from the Industry Council
- There were no failures that were seen for the 500 V products
- Failure rate phenomenon is independent of the product ESD level
- The failures seem to be related to EOS or System Level ESD

# Data Exclusively on Consumer Products



- Consolidated data from the Industry Council
- Failure rate phenomenon is independent of the product ESD level
- The failures seem to be related to EOS or System Level ESD

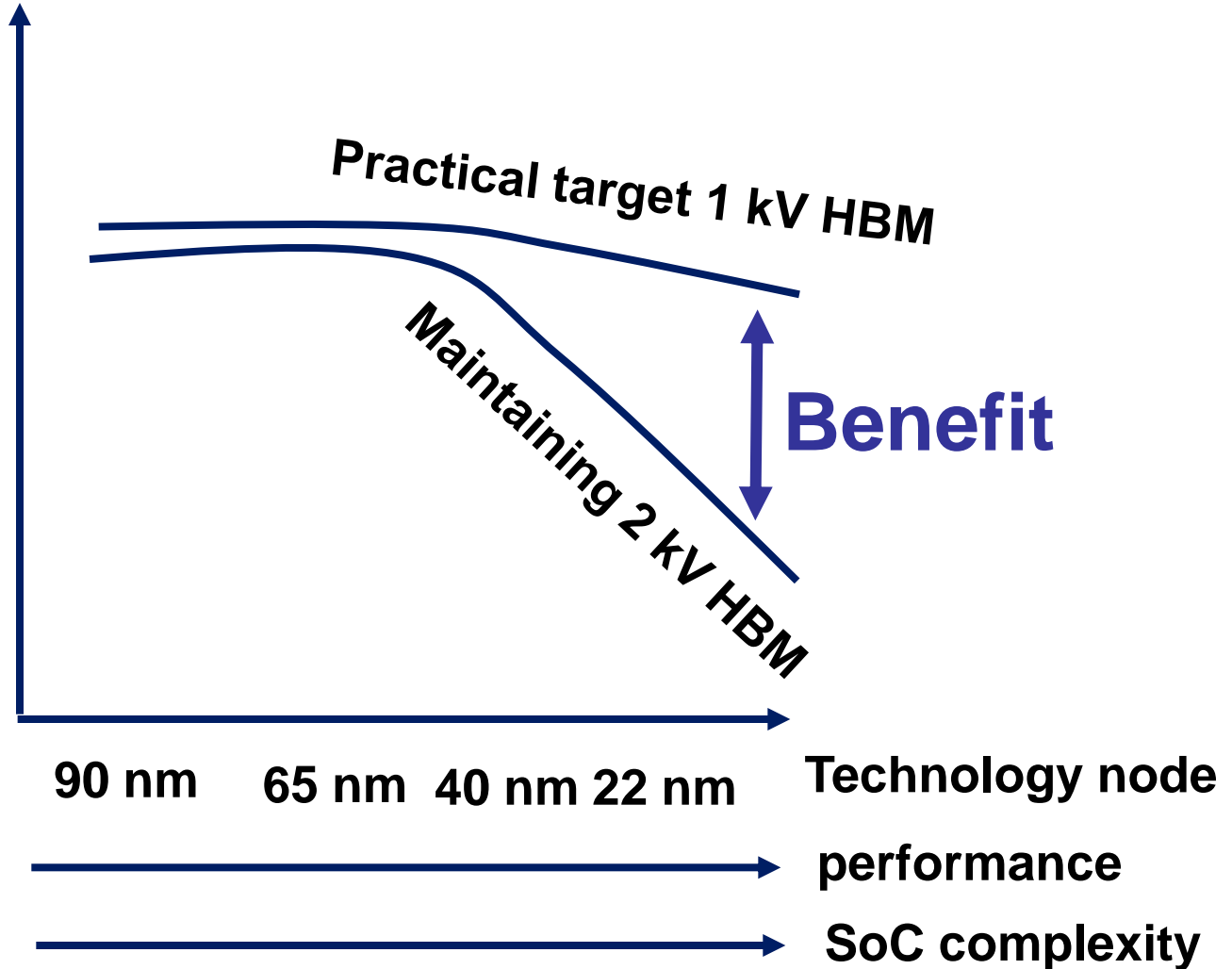
# Question

**Why should the OEM accept lower levels?  
Is there any benefit to the OEM?**

- *One benefit comes from reducing the time to market for numerous products*
- *Additional benefits come from maintaining or improving system performance and flexibility*

# Benefit for OEM

- Flexibility
- System performance
- Speed to Market





# Question

**Is the Industry Council making these recommendations to save money for the supplier?**

- *The concept of “ESD Effort” applies to both suppliers and customers. The suppliers go through repeated testing, debugging, and design re-spins to meet the existing specified ESD requirements.*
- *Both customers and suppliers go through joint meetings to understand and negotiate solutions for improvements. These efforts delay the product delivery and can also have an impact on product circuit performance.*

# Effort of Meeting the *ad hoc* ESD Levels

- The required effort to meet ESD levels continues to rise
- This effort is shared by both customers and IC suppliers
- Both parties benefit from realistic ESD targets that avoid over-specification.

## Impact on Suppliers

- Limitations on circuit performance
- Leakage spec and battery life
- Chip area and cost
- Qualification delay of IC
- Time to market for IC
- HBM/CDM focus
- Misdirecting resources

## Impact on Customers

- Limitations on system performance
- System power and functionality
- Chip area and shipping volume
- Qualification delay of system
- Time to market for system
- Lack of relevant system robustness
- Lack of system optimized solutions

# Consequences of Keeping Old Standards

- **As technologies advance and the expected increase in IC circuit speeds occur, the old *de facto* levels can cause constraints related to**
  - **HSS I/O designs limited to below 20 Gb/sec or less**
  - **Inability to apply high speed designs into larger high density packages used for lowering power dissipation**
  - **Inability to design with advanced sub-32nm technologies for denser IC functions**
  - **Difficulty in delivering IC chips meeting all the complex ESD qualification requirements**
    - **HBM pin combination nuances often lead to non-critical or false failures that overload the debug procedures**

# HBM ESD Levels (Current WP1 Version)

HBM Level of IC	Impact on Manufacturing Environment
2 KV	<u>Basic ESD Control</u> methods allow safe manufacturing with proven margin
1 kV	
500 V	
100 V to <500 V	<u>Detailed ESD Control</u> methods are required

**Basic Programs:** Include wrist straps, grounded work surfaces, and safe packaging materials – and are safe with proven margin to 500V.

**Detailed Programs:** JESD625B has a scope of 200V, but does not have a footwear-flooring system test for personnel grounding.

- Processes compliant to ANSI/ESD S20.20 or IEC-61340-5-1 allow handling and manufacturing of ICs even as low as 100V HBM.

# Conclusions for HBM

- 2 kV HBM design is frequently causing unnecessary qualification delays across multiple technologies
- HBM qualification levels between 500 V and 2 kV exhibit the same level of manufacturing quality and field robustness
- Targeting 1kV HBM is safe and is proven to provide sufficient margin

# Automotive ESD Exposure Scenarios

- Concern: Potentially higher ESD risk in OEM lines since they might have no ESD control in their assembly lines
- Reality:
  - only “external” pins affected (system pins)
  - system level robustness is not related to HBM ESD robustness
- Concern: Fear of higher ESD risk during repair, since ESD control is low or zero - especially in non-licensed repair stations
- Reality:
  - only “external” pins affected (system pins)
  - system level robustness is not related to HBM ESD robustness

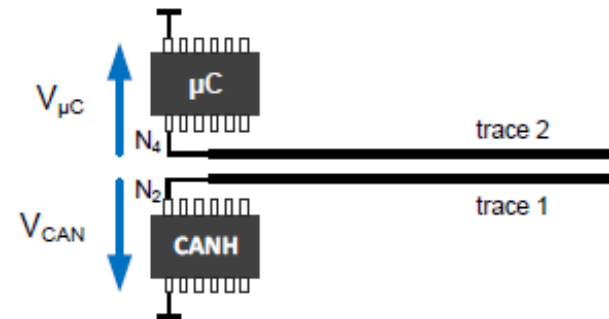
# Automotive ESD Exposure Scenarios

- Concern: Crosstalk between long PCB traces leads to overstress at internal pins during system level ESD stress
- Reality:
  - A typical analysis applied to CAN and  $\mu$ P pins shows low energy coupling between PCB traces when system level ESD pulses are applied [zur Nieden et al.]
  - Thus in general, 1kV HBM ESD robustness of internal pins is sufficient to handle typical induced energies of system level ESD pulses

# Crosstalk to Internal Pins

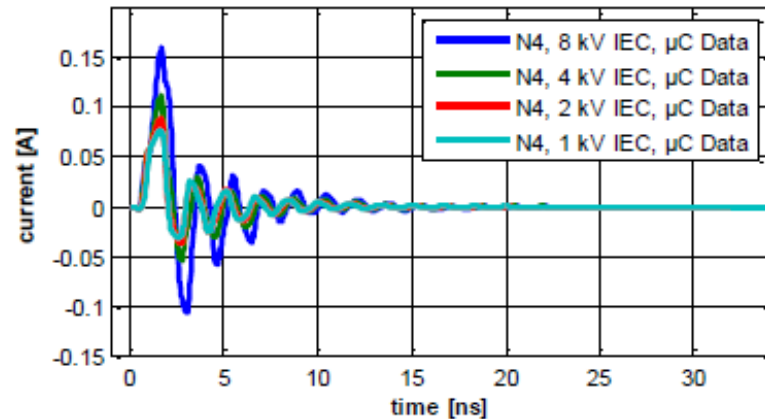
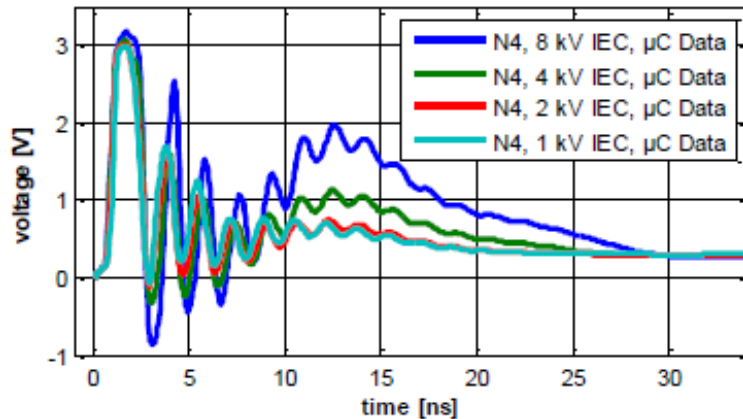
- Simulated quantities at CANH pin

$V_{\text{charge}}$ [kV]	$V_{\text{max}}$ [V]	$I_{\text{max}}$ [A]	$E$ [ $\mu\text{J}$ ]	$E/E_{1\text{kV}}$
1	50,24	3,86	4,67	1
2	77,52	8,03	12,42	2,66
4	132,01	16,36	35,99	7,71
8	240,90	32,96	115,51	24,73



- Simulated quantities at  $\mu\text{C}$  DATA pin

$V_{\text{charge}}$ [kV]	$V_{\text{max}}$ [V]	$I_{\text{max}}$ [A]	$E$ [nJ]	$E/E_{1\text{kV}}$	Energy Coupling Factor ( $E_{N2}/E_{N4}$ )
1	2,98	0,08	0,28	1	16679
2	3,02	0,09	0,29	1,06	42828
4	3,08	0,11	0,37	1,34	97270
8	3,18	0,16	0,68	2,46	169870



Friedrich zur Nieden, Stanislav Scheier, Stephan Frei; „System level ESD on-PCB coupling”, report 2011.



# Epilogue

- The OEMs have been skeptical about these changes but are now gradually gaining confidence that the necessary paradigm shift is not only safe, but is essential for the production of high speed circuits.
- This was necessary because of the continuous and extensive effort throughout the semiconductor industry to meet some unsubstantiated ESD levels that are now clearly understood to be over-specified

# Additional Questions

# FAQ

## **Will the modified ESD levels as recommended here shift the burden to manufacturers?**

- *Manufacturers already have an obligation to provide basic ESD controls.*
- *Verification of these controls in their manufacturing and handling processes are necessary no matter what ESD levels are accepted.*
- *The current ESD target levels have been over specified. The modified levels reflect what is realistic and represent no shift of burden to the customers.*

# FAQ

## **Will all CMs be able to guarantee that there is good control to safely meet these levels?**

- *CMs handling electronic components typically have the expertise required for basic ESD control programs.*
- *The CMs are already generally required to provide and verify ESD control programs as a condition for doing business with their customers.*
- *Just the basic control methods easily ensure that devices with a HBM robustness of 500V can be safely handled.*

# FAQ

**While we agree that 1kV or 500V HBM is adequate and safe, how would one deal with competition that uses ESD as a marketing advantage?**

- *We hope most customers who are informed, especially through the White Paper 1 document, would see that the only things that matter are consistent circuit performance to specifications and on-time product delivery.*

# FAQ

**Suppliers look at products that are shipped at lower HBM levels and say that no field return failures are seen. If not all the pins are weak, how can we be sure if this type of data has any relevance?**

- *The data shows that the tracked field returns are independent of their respective HBM ESD level when the devices were shipped; i.e. most the field returns are due to EOS and not due to ESD.*
- *What is interesting is that these failures are often not seen on the pins with the lowest HBM levels. The returns seen with EOS seem to depend more on the function of the pin on the application board.*

# FAQ

**In the early 70's the 2kV HBM level was discussed as a possible standard, and by the 80's it became the widely accepted level.**

**Why would this not be relevant anymore?**

- *The 2 kV HBM / 200V MM target levels were set when not much was understood about ESD control methods.*
- *These have improved dramatically. At the same time, the assembly methods for the IC chips have undergone major changes as well.*
- *When basic ESD control elements are installed, HBM and MM are no longer a risk for devices in modern assembly lines.*

# FAQ

## **Why do some IP suppliers claim they can deliver a cheaper more efficient ESD protection methodology at the same levels as before?**

- *The interaction between the “target level” and the protection design is related to the same physics. In all cases if the ESD target level is reduced, then the ESD layout area and impact on normal electrical performance may be similarly reduced.*
- *The problem is then to choose the appropriate ESD target level. ESD over-design is inefficient and wasteful.*



# FAQ

## **Will the lowering of component ESD levels have an impact on the overall system reliability?**

- *This is an often misunderstood concept. There has been no proof that components with lower HBM performance have seen more system level failures.*
- *Since the system level test applies only to external interface pins, this protection design strategy is quite different.*
- *The Industry Council is in agreement that system levels ESD protection, cable discharge protection and transient latchup are critical areas where future focus is needed.*

# FAQ

**If system level ESD testing does not guarantee system level (including component) ESD performance, isn't a higher target for component level HBM ESD better than nothing?**

- *This would only give a false sense of security while again going through extensive cost of analysis, customer delays and a potential circuit performance impact.*
- *System level ESD and component level ESD are not related to each other, furthermore, system ESD protection depends on the pin application and requires a different strategy.*
- *System level ESD is clearly important, but focusing on excess component level requirements could pull resources away from addressing and designing better system level ESD.*