Charged Device Model (CDM) Qualification Issues

Purpose /Abstract

- IC design for performance constraints make it increasingly difficult to meet the current CDM levels as the technologies continue to shrink and the circuit speed demands continue to increase
- This work shows that devices with CDM levels below the general target of 500 V can safely be handled with CDM control methods available in the industry today
- **Based on these observations and constraints it will be shown through this work that 250V is a safe and practical target CDM level**

Outline

- Relevance of CDM
- CDM Technology & Design Issues
- CDM Qualification Methods
- ESD Control Methods Addressing CDM
- Analysis of Field Return Data
- Summary
- Conclusion
- Roadmap

Relevance of CDM

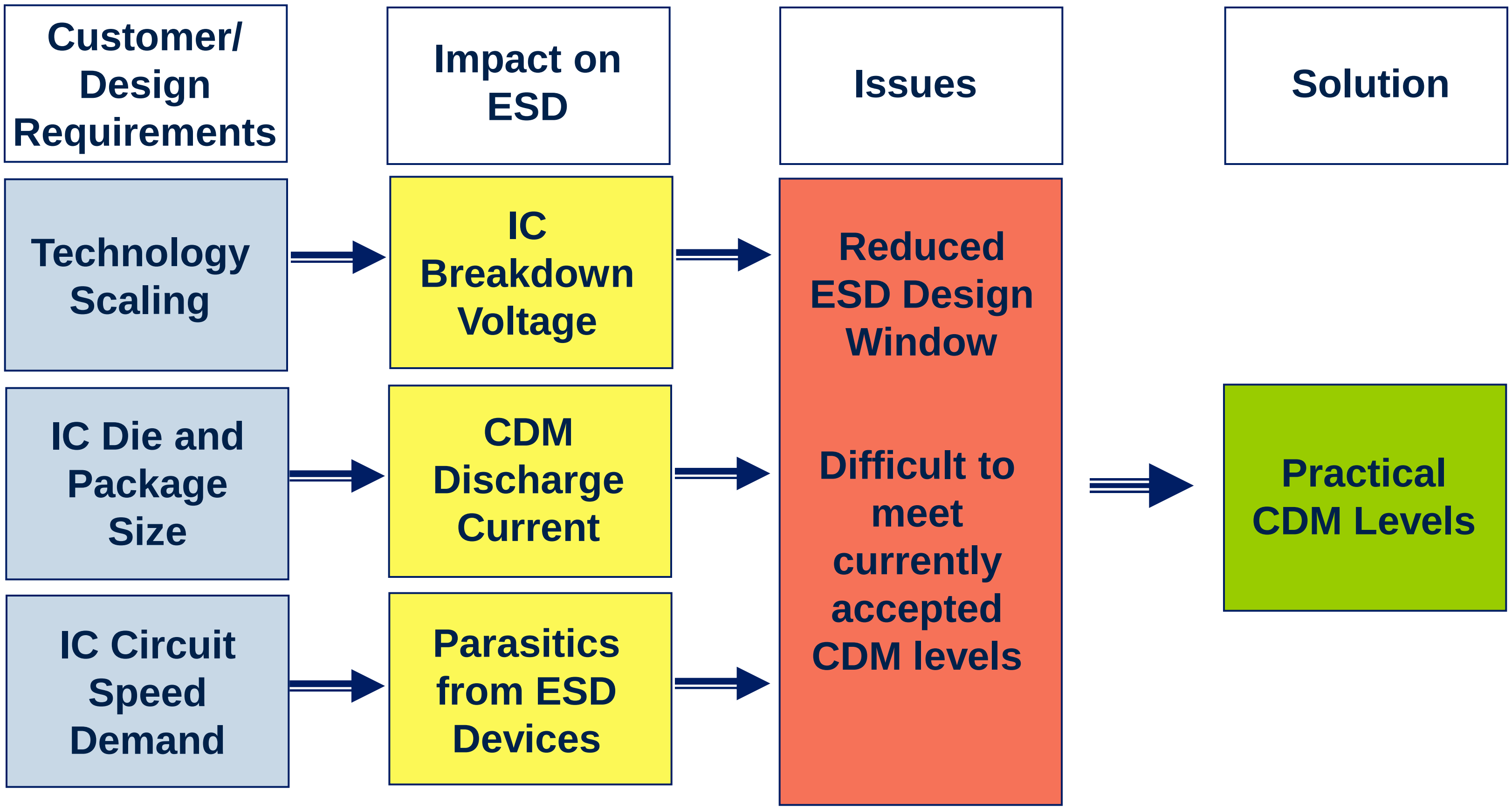
- CDM is a unique and important test method for IC component ESD testing
- There are proven damage signatures for field returns due to fast ESD discharges with high peak current that cannot be reproduced by HBM (or MM)
- CDM testing can effectively replicate these failure signatures
- Typical discharge scenarios have been simulated in IC testing and observed in manufacturing which cause CDM failure signatures

➔ **CDM is a necessary and important qualification test**

CDM Technology & Design Issues

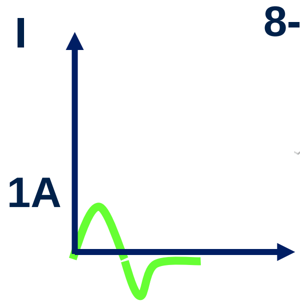
- CDM protection design is primarily driven by the peak current from the IC package discharge at the required (targeted) CDM voltage level.
- Increasing package size (and capacitance) lead to increasing peak CDM current for a given CDM stress voltage.
- Additionally, CDM protection design is increasingly limited by reduction in breakdown voltage of gate dielectrics and junctions.

CDM Technology & Design Issues

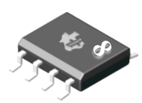


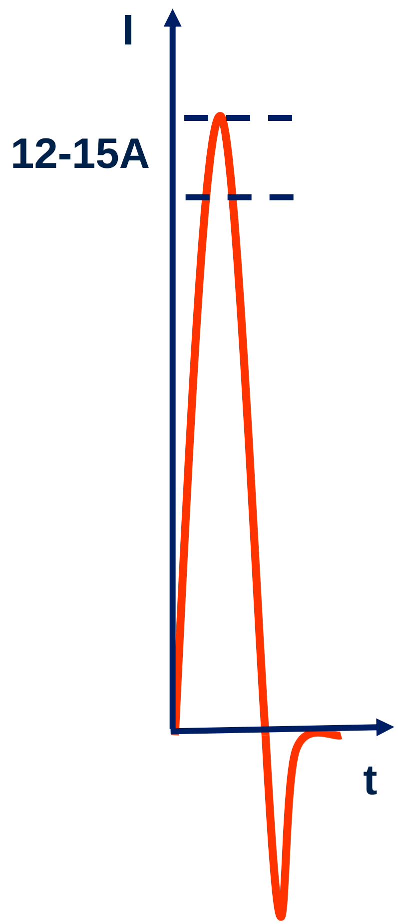
➔ IC design requirements create severe limitations for CDM protection

Impact of Package on CDM Discharge Current @500V

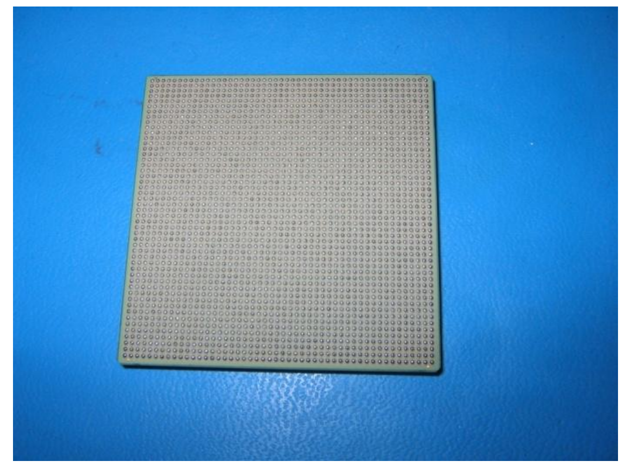


8-Pin DIP



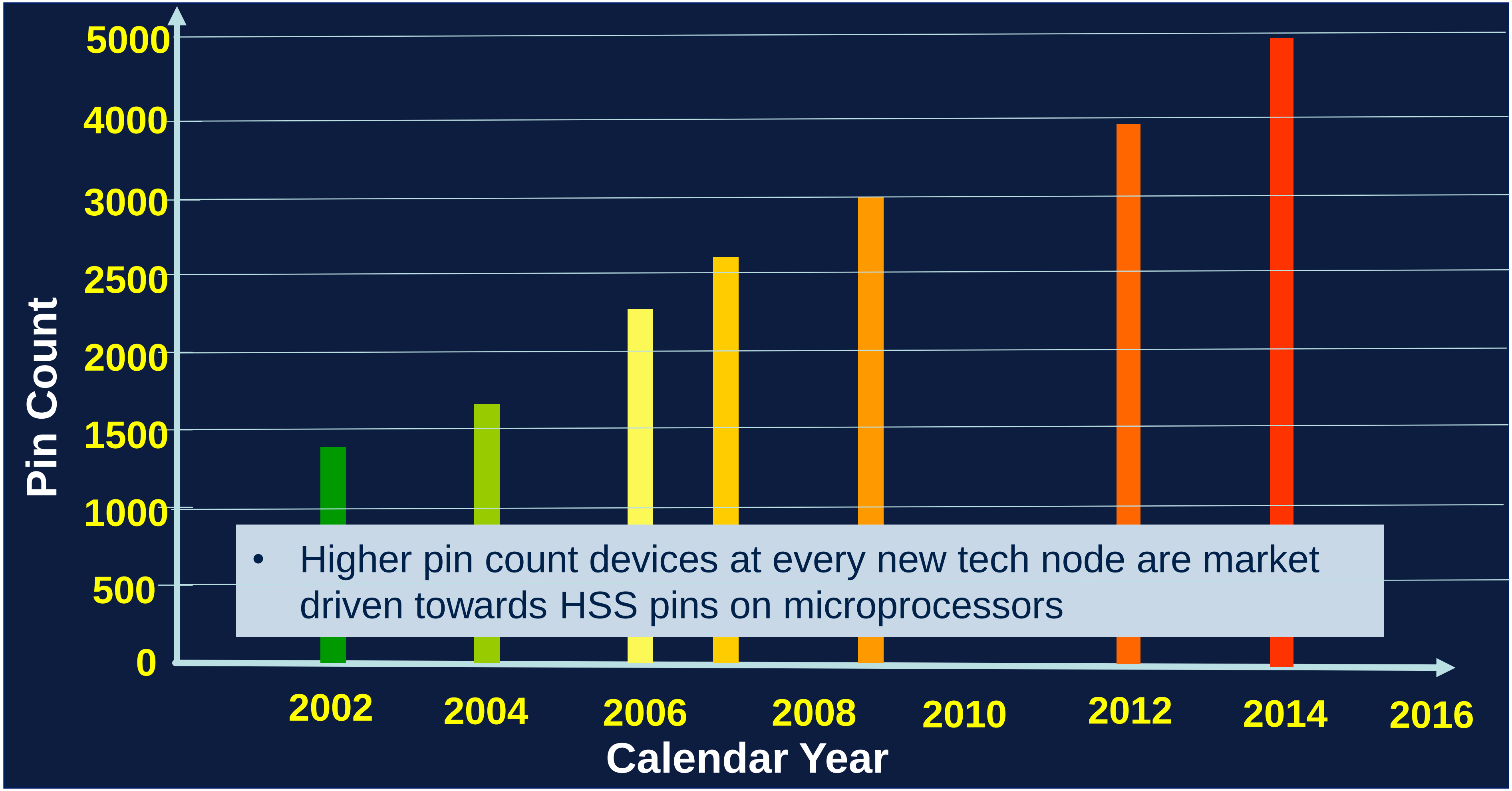


2400-Pin LGA



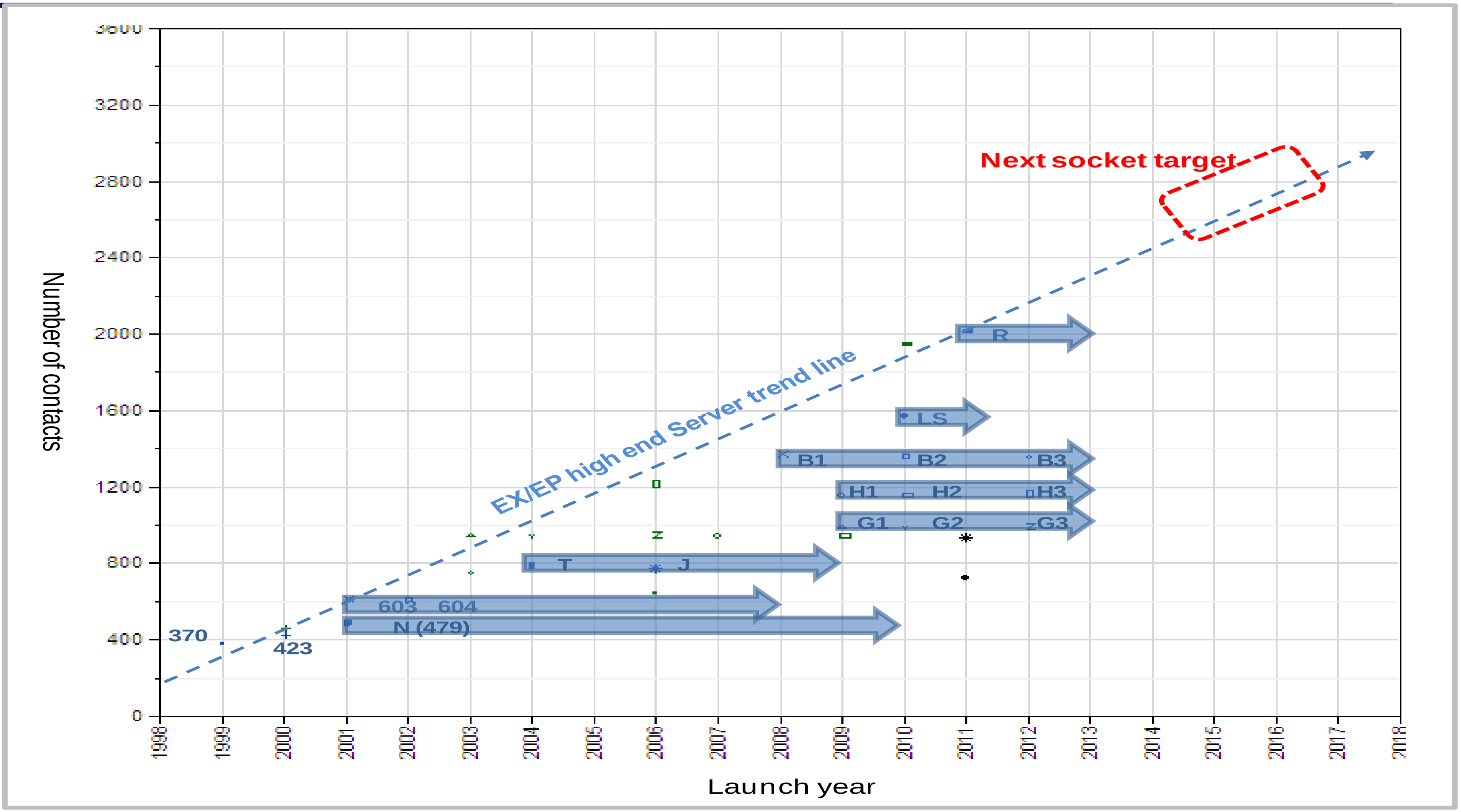
➔ Wide variations (>12X) in the peak discharge current from the smallest to the largest IC packages

Trends in IC Package Pin Counts: Microprocessors

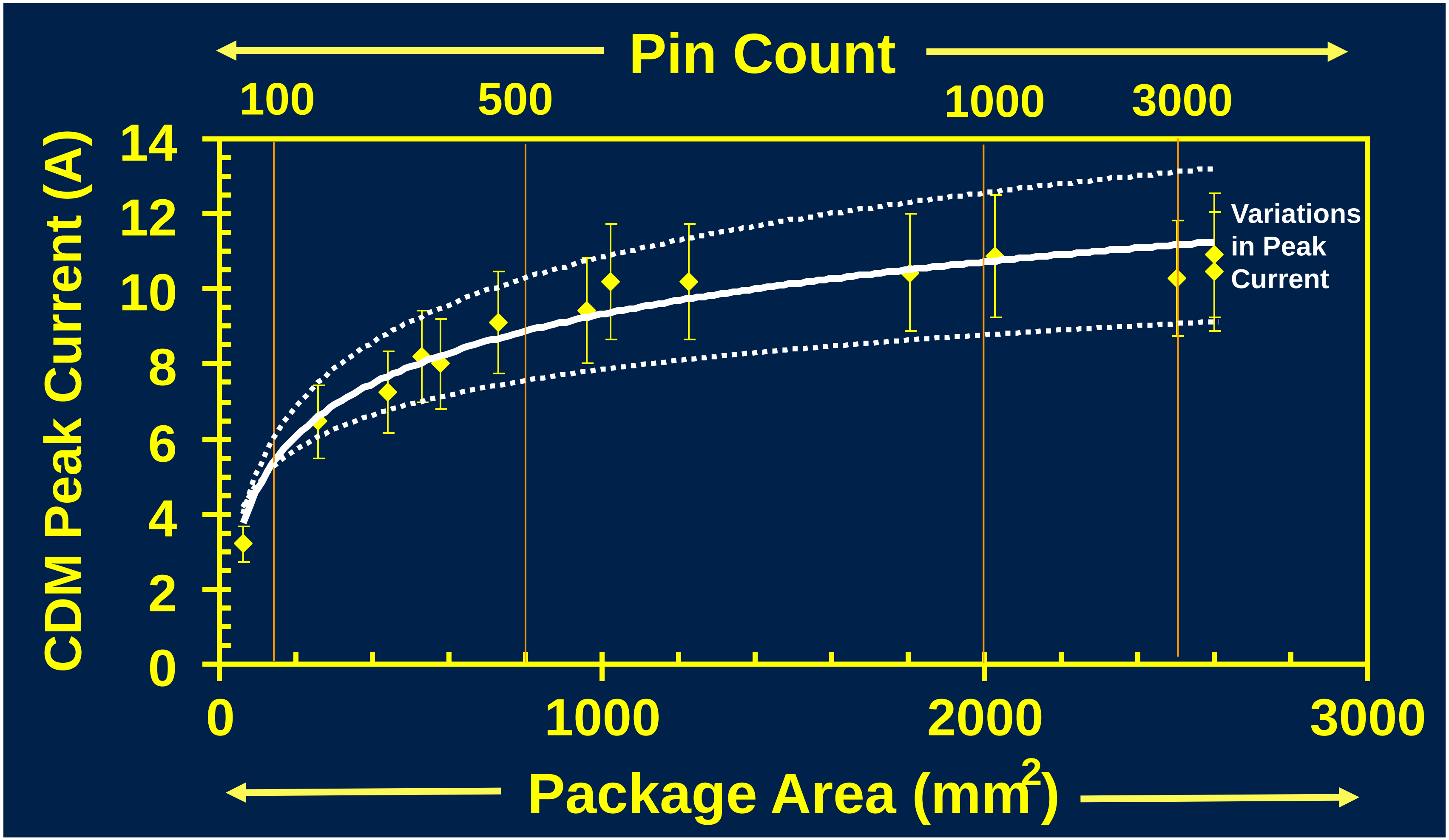


- Higher pin count devices at every new tech node are market driven towards HSS pins on microprocessors

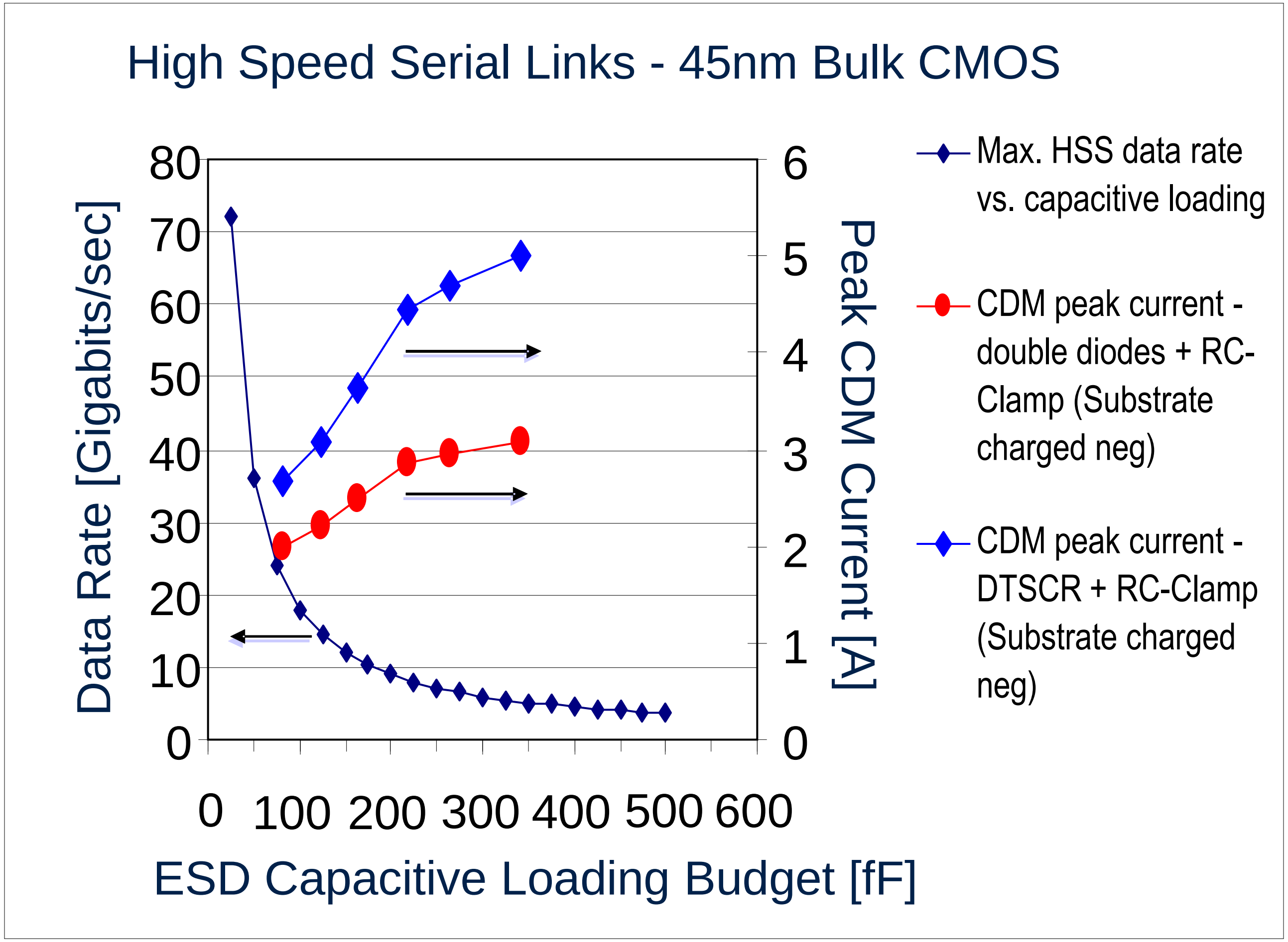
Trends in IC Package Pin Counts: Server Sockets



CDM peak Current @500V Vs. Pin Count (Package Area)



CDM Analysis - Example for High Speed Serial Link



- Capacitive loading of ESD protection for high speed serial (HSS) link design is limited to ~ 100 fF.
- **The limitation to 100 fF only allows a maximum peak current of 4 A in this example.**
- For BGA with more than 300 pins this limits the CDM level to 250 V at best.

Overview of CDM Design Capability for Advanced Nodes with 10-20 GB/s Speed Performance

Tech. Node	Design Type	Max Achievable CDM Peak Current		Corresponding CDM Level
65nm	High Speed Serial Link	5-6 Amps		300-400V
45nm	High Speed Serial Link	4-5 Amps		250-300V
45nm	Radio Frequency (RF)	2-3 Amps		200-250V

➔ 200-250V becomes the new practical level that is achievable

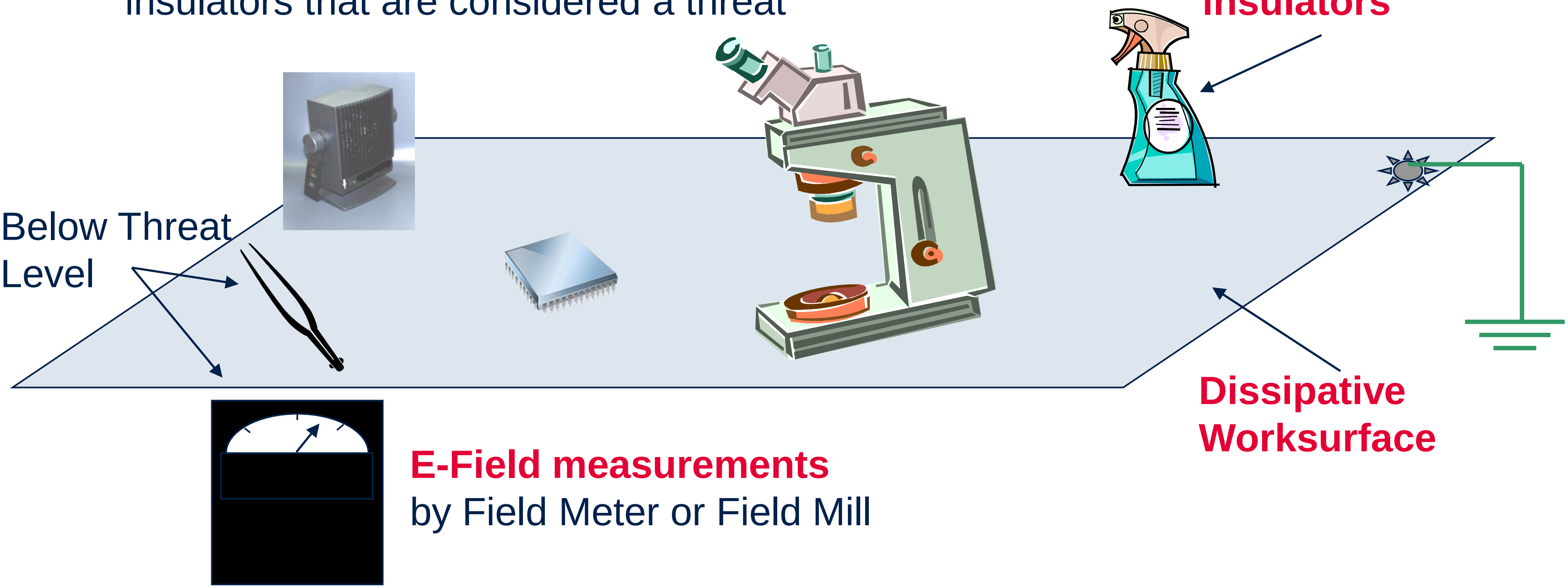
Relevance of ESD Control for Safe Manufacturing

- For CDM, as with HBM, ESD control in the production areas is an essential part of a safe manufacturing process
- Effective ESD control measures covering CDM events include the grounding of metallic machine parts, control of metal-to-metal contact with the device leads AND control of insulators
- Control of insulators requires assessment of the various handling steps

Basic ESD Control Program addressing CDM

Ionizer if there are process relevant insulators that are considered a threat

Remove all non-process relevant **insulators**



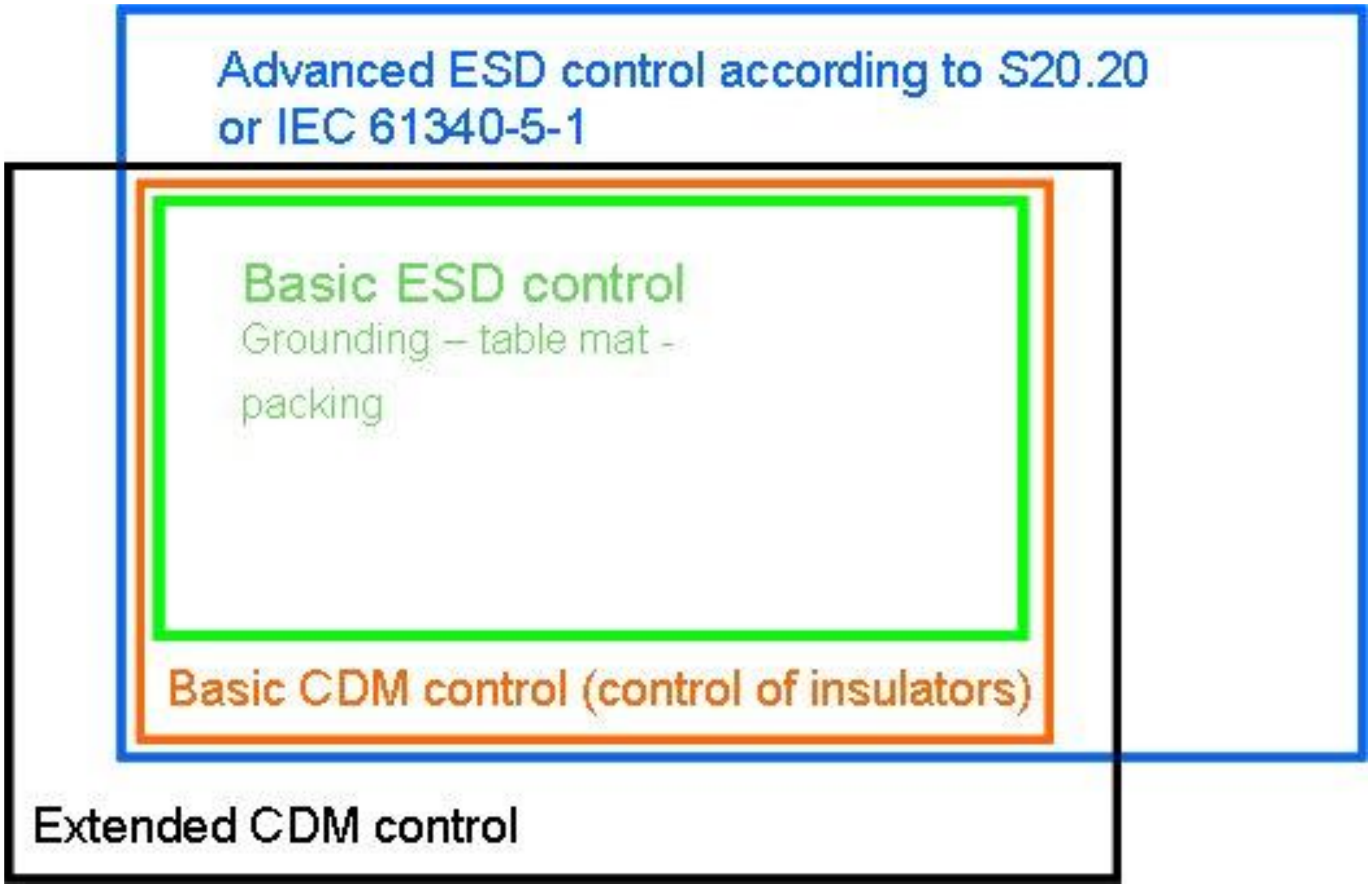
Below Threat Level

Dissipative Worksurface

E-Field measurements
by Field Meter or Field Mill

Threat level per ANSI/ESD S20.20 and IEC 61340-5-1

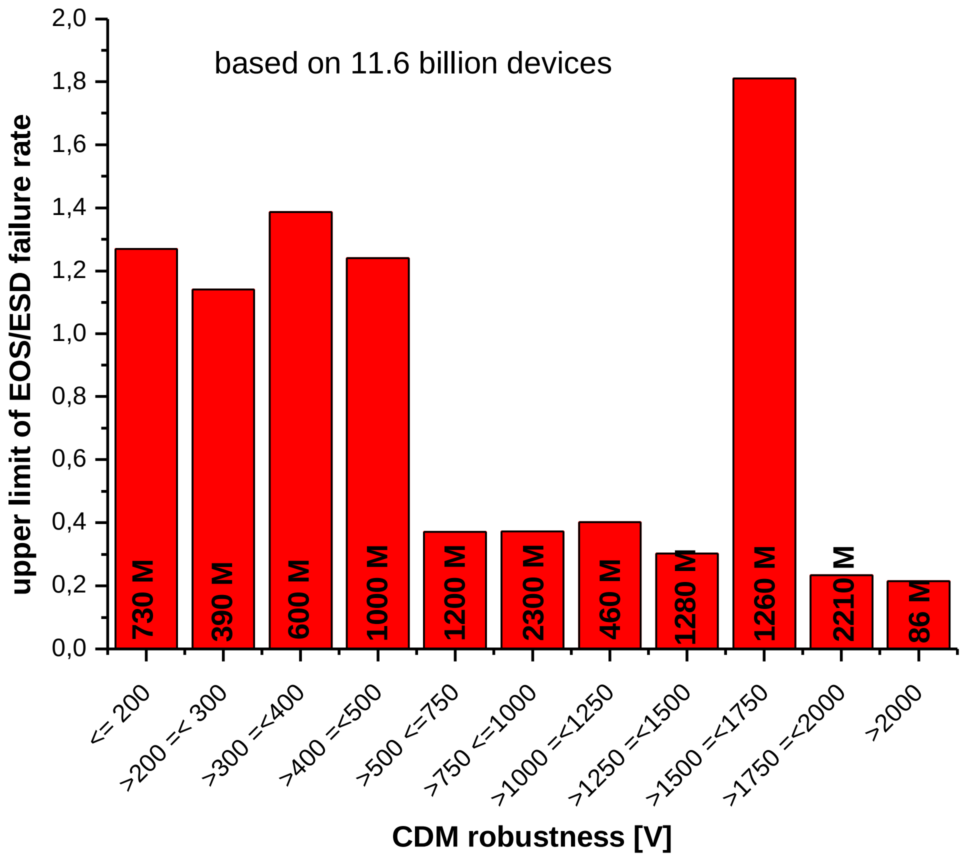
Relationship between General ESD Control and CDM Specific Control



Analysis of FAR Data

- FAR data was collected from various Council members for over 11 billion shipped IC's.
- Field returns include returns from handling and testing by IC suppliers, manufacturing of the PCBs and end-customer returns.
- 949 designs have been included covering automotive, consumer, memory and discrete products.
- The presented data were collected in the time frame from 2003 to 2007.

FAR Data versus CDM voltage



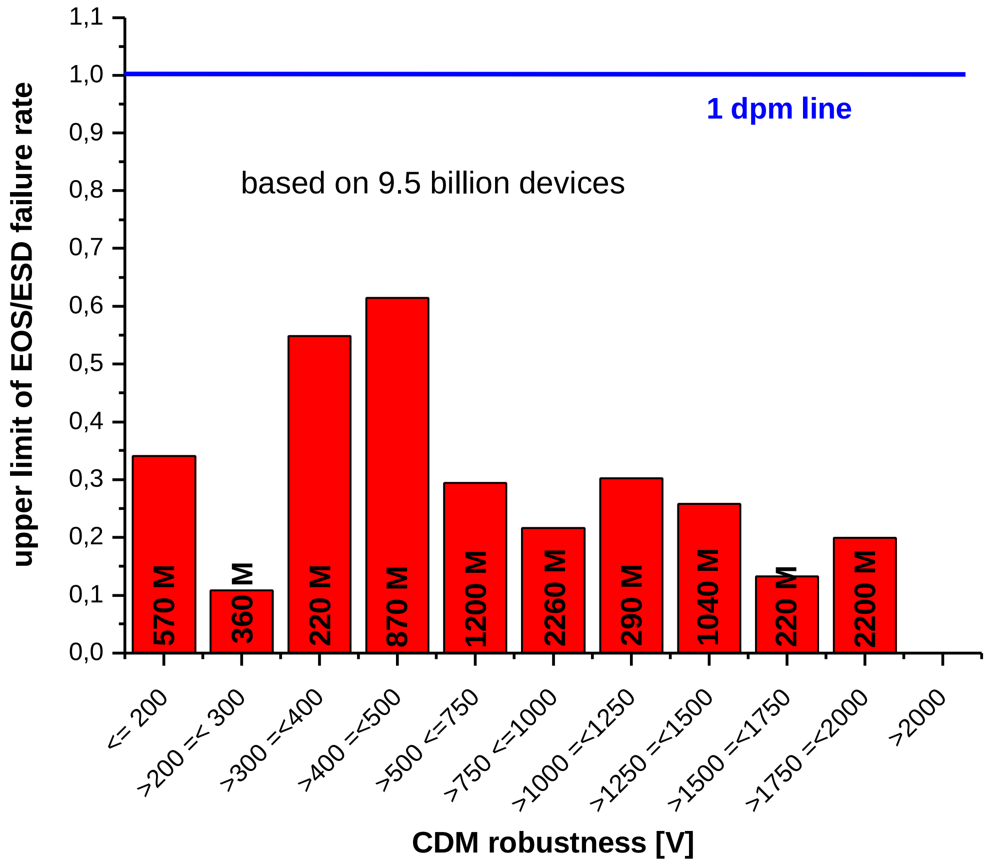
<u>Important Observations:</u>

- EOS/ESD failure rates do not show a clear trend with respect to dependence of the CDM voltage
- A few designs with high return rates (outliers) dominate the statistics

Further Limitations:

- Devices not always tested to failure voltage
- Discrepancy between JEDEC and ESDA testers
- Rel. Humidity during testing not controlled/recorded

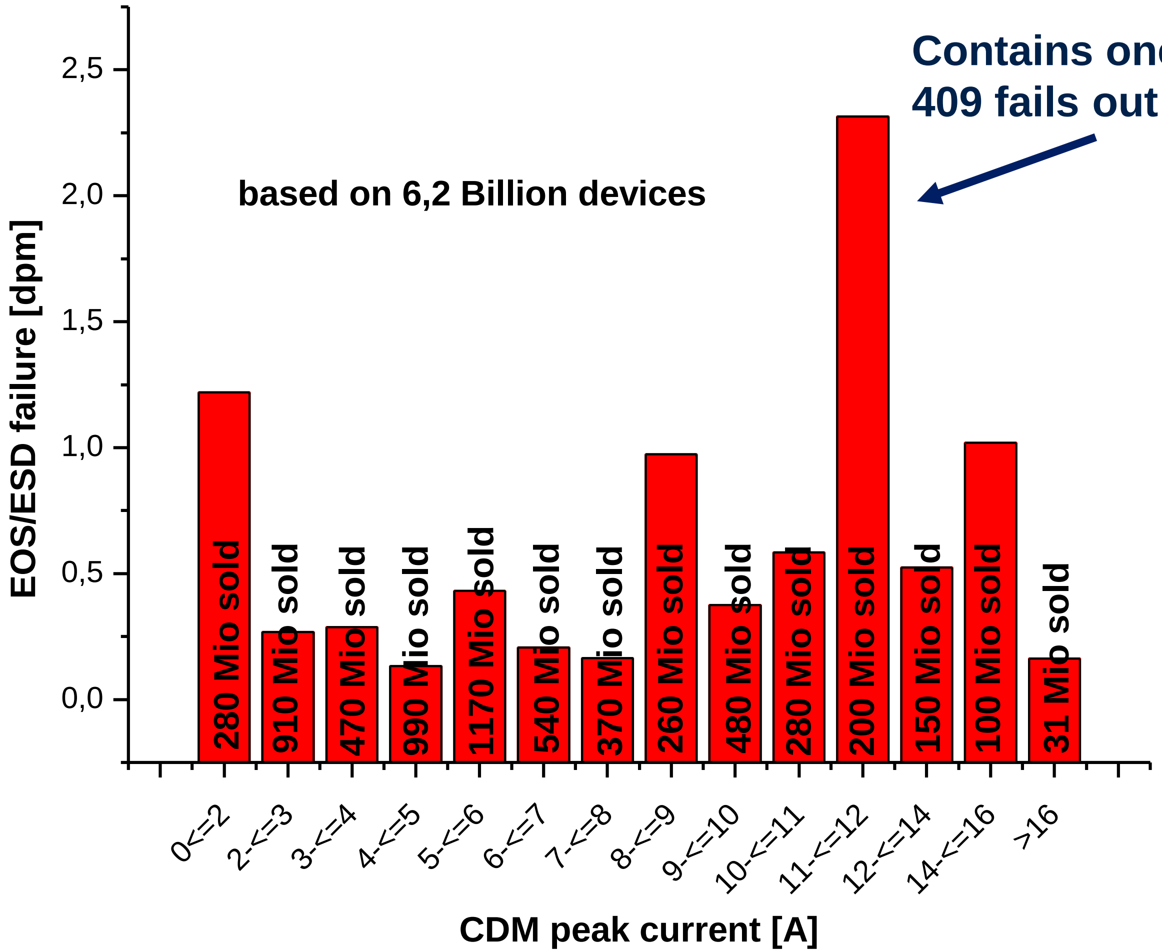
FAR Data versus CDM voltage w/o Outliers



Important Observations:

- Excludes 15 designs classified as FAR outliers (defined by > 100 field returns per type)
- Remaining designs (934 out of 949) show a FAR rate < 1 dpm
- No increase in the average return rate of parts with lower CDM levels

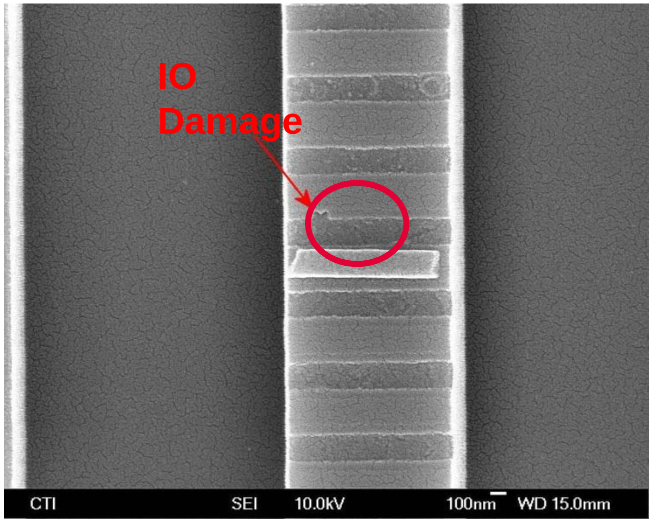
FAR Data versus CDM peak current



Contains one outlier in TQFP 100 with 409 fails out of 36 Mio (V_{CDM} = 1000V)

- **Limitations: Some peak currents were measured with a 1GHz scope, others with 4GHz scope (up to a factor of two difference in peak value)**
- **BUT: EOS/ESD failures occur at all CDM peak currents levels (even at very high values)**

Analysis of FAR of a CDM Weak Device



Design Issue & Failure Effect

- High speed IO performance required low capacitance ESD solution in 90nm
- Low capacitance solution = Low CDM
- Device pins were therefore clearly susceptible to field failures
- At the failure threshold current level for CDM discharge, IO damage is expected

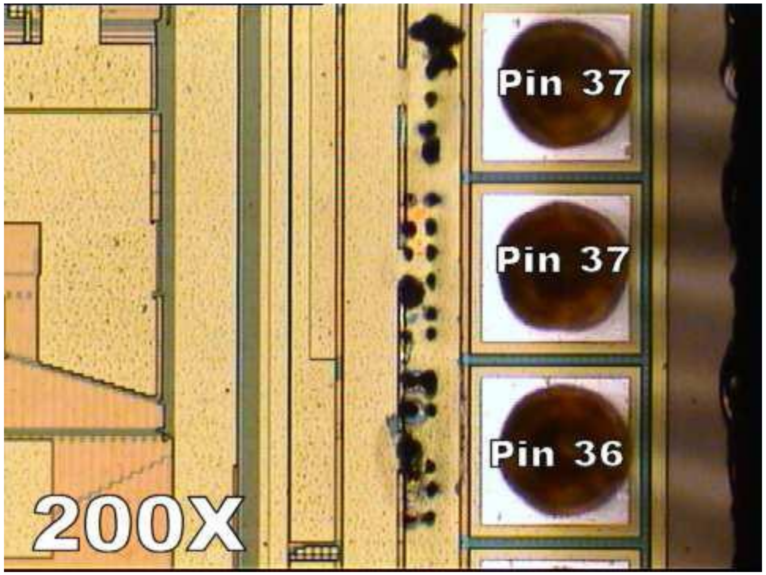
➔ FA indicated this expected damage

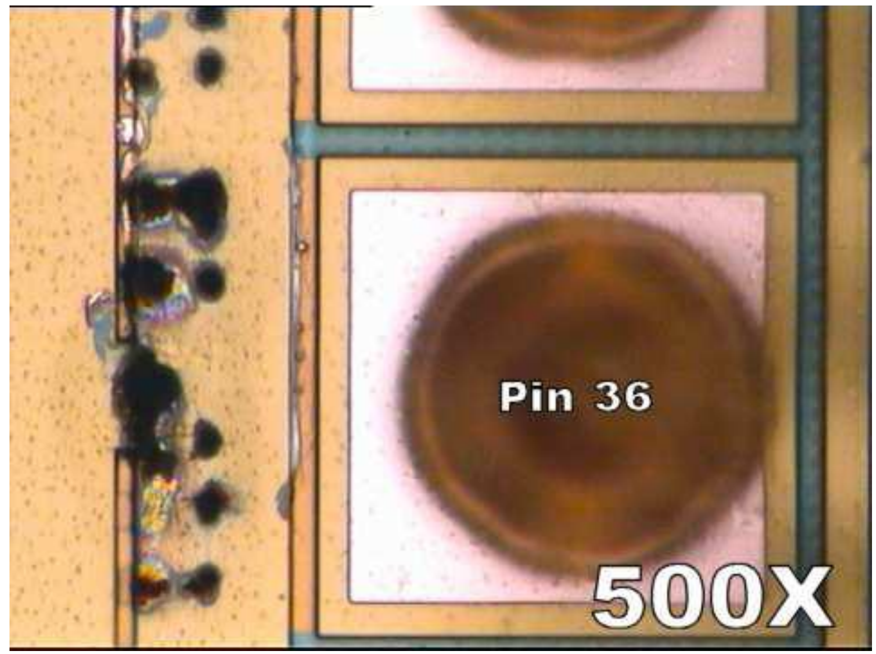
Low CDM Effect on FAR

- 140-Pin BGA shows 30 failures out of 67M units shipped
- CDM performance = <125V
- FA shows clear damage on IO gate due to marginal design
- Identical damage was detected on units stressed at 125V
- Implementing advanced CDM controls resulted in 0 FAR for 105M shipped

➔ Control measures can be effective, even for low CDM

Analysis of FAR Outlier (CDM Robust Device)



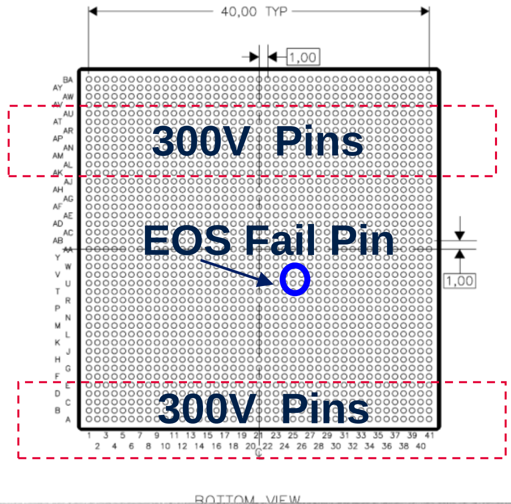


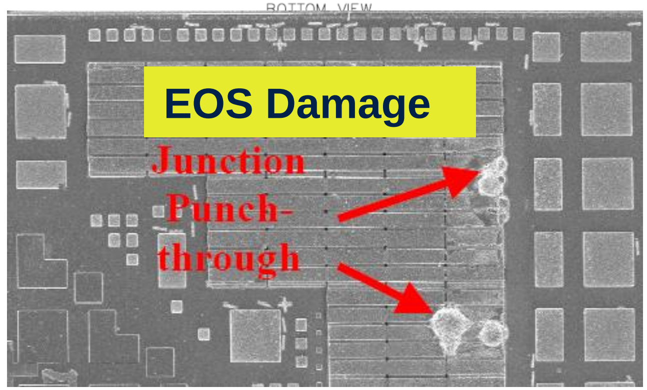
- **Outlier in TQFP 100 shows 409 fails out of 36 M devices sold**
- **CDM robustness voltage = 1000V**
- **Failure showed molten metallization**
- **Failure is due to EOS but not CDM**

Analysis of EOS related FARs

- **Example of 130nm product with medium CDM**
- **1681-LGA Product has 320 High Speed pins**
- **300V CDM performance on all 320 HS Pins**
- **All other pins >500V**
- **Some customer returns, but Failure Analysis shows only EOS damage**
- **No EOS damage on any of the 300V pins**
- **EOS on only Power Supply Pin with >500V CDM**

➔EOS on returns not correlated to CDM level





Conclusions from FAR Data Analysis

- EOS/ESD FARs can appear for any level of CDM from <100 V to >2000 V
- FARs with clear CDM damage can be seen for ICs with very low CDM passing level
- Proven CDM-type events occasionally occur during the ramp-up phase of a new handling/testing process at the IC supplier.
- FARs during ramp-up can also occur for devices with greater than 500 V CDM robustness.

Conclusions from FAR Data Analysis

- Addressing the failure mechanism with proper ESD control measures solves the problem. Usually only a minor effort combined with a low investment in cost is required.

➔ CDM field fails can occasionally occur with significant return rates during ramp-up. This has to be solved by ESD control measures.

Conclusions from FAR Data Analysis (II)

- Case studies show that a number of field failures in the FAR data are due to EOS or Charged Board Events (CBE).
- There was no observed correlation of CDM weak pins and EOS fails.
- Due to the high energies involved, it is not possible to address EOS and CBE hazards by on-chip CDM protection design.
- CBE is a factory protection issue and must be addressed by assembly protection measures.

➔ CDM qualification levels should not be based on protection requirements against EOS and/or CBE.

Summary – HBM vs CDM

- **For HBM** it is well known that with basic ESD control measures, safe handling of IC components can be guaranteed in an EPA
- **But for CDM** additional control measures may be necessary for specific handling processes in the EPA
- Additional measures for CDM should include a process specific assessment to control charging of insulators in the manufacturing environment as a requirement.

New Recommended CDM Classification Based on Factory CDM Control

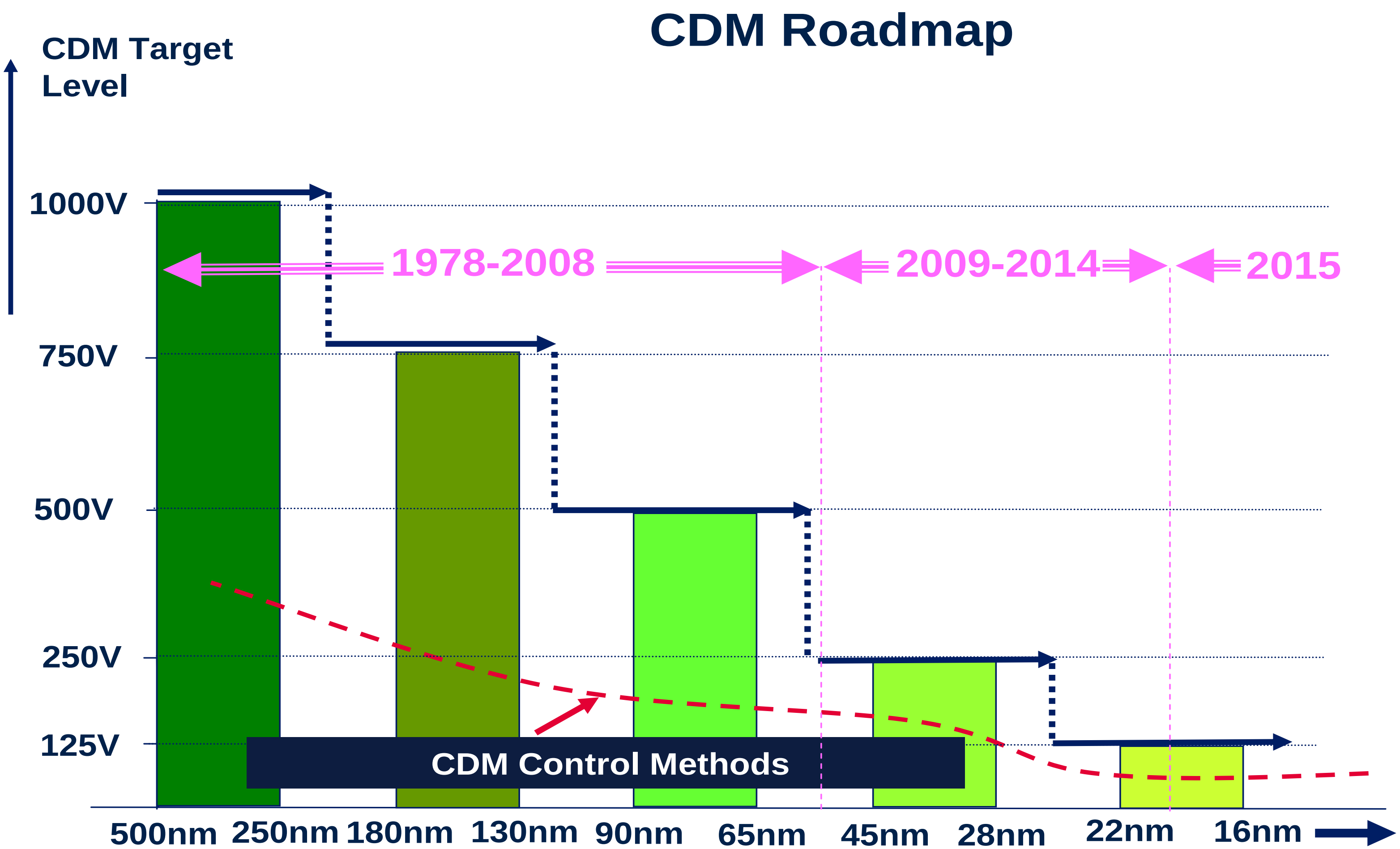
CDM classification level (tested acc. to JEDEC)	ESD control requirements
$V_{CDM} \geq 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators
$125V \leq V_{CDM} < 250V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **OR** to avoid a hard discharge (high resistive material in contact with the device leads).
$V_{CDM} < 125V$	• **Basic ESD control methods** with grounding of metallic machine parts and control of insulators + • **Process specific measures** to reduce the charging of the device **AND** to avoid a hard discharge (high resistive material in contact with the device leads) + • **Charging/discharging measurements at each process step.**

➔ Published as JEP157

Summary – Protection Design Constraints

- Technology downscaling combined with increased IC performance requirements and the trend towards larger package sizes have all placed severe constraints on CDM protection design.
- These constraints are even more limiting for high capacity packages with high speed interfaces.
- Because of these technology and performance constraints, the old standard of 500 V CDM cannot be maintained.

CDM Qualification Roadmap



Q & A

Q: If the production areas have basic control for ESD, would these methods also provide the necessary protection for CDM?

A: If the basic controls are in place and include control of insulators, then the chances for ESD events of any kind would be minimized

Q*: What are the main weak points for CDM ESD control in manufacturing?*

A: In contrast to controls for HBM, ESD controls for CDM rely on controlling the charge on insulators and controlling discharges to the conductors of the manufactured devices.

Q & A

Q: *How is it determined that lower than 500V CDM are really safe?*

A: It has been proven that even 100V CDM parts can be manufactured if appropriate CDM control measures are taken. The same assessment of ESD control measures and fail return data show that devices with 250V CDM are equally safe as 500V parts in typical modern manufacturing sites.

Q: *If the specifications are meant for all pins of a package, would it not make sense to require higher levels for the corner pins?*

A: With the automated pick and place tools today, any of the pins could make first contact. All of the pins need to be considered, the corner pins should not be treated differently.

Q & A

Q: *What if the customers are not confident that the subcons have the control measures to match the new requirements*

A: Simply staying at the old levels will not address the design challenges. It should be noted that:

- Customer demands for better IO performance will place more stress on achieving the old target levels.
- Efforts to improve CDM protection in the manufacturing facilities need to continue to be a focus area if we are to meet these challenges.
- In addition to the basic CDM protection measures, an analysis of the production lines should be completed. This is especially critical during introduction of new process steps or during product ramp-up

Q & A

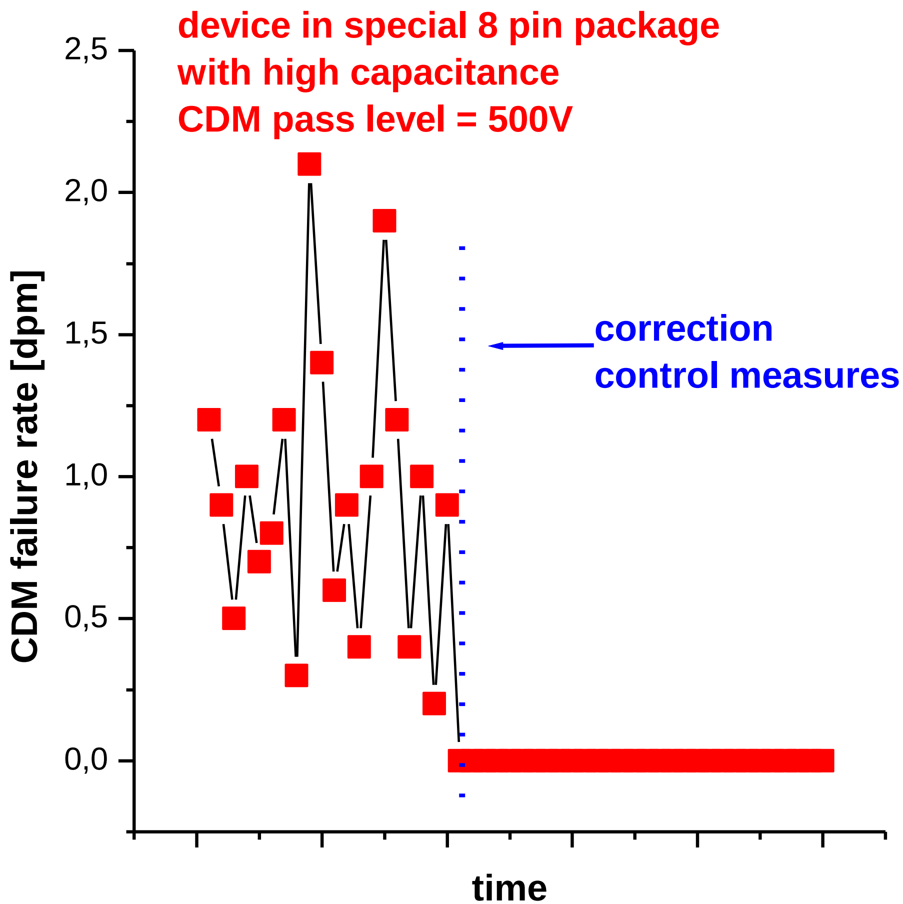
Q: *Will CDM change from die to package level? Will the die have greater risk in assembly onto a board*

A: In most cases, bare die or wafer level MLF show higher peak current levels than the same die in a package. If the die has the same connectivity to the board as the package, it could have a higher risk of charged board damage. Care must be taken to place the die away from insulators on the board that could charge up during assembly.

Q: *Are charge board events (CBE) related to CDM and shouldn't IC pins be designed to handle CBE?*

A: Board level aspects of CBE (much greater capacitance) results in failures that are much more severe, like EOS. Component IC protection cannot be designed to handle CBE events, which can be large and vary from application to application. Additional system level EOS protection must be provided.

Confirmed CDM failure @ Semiconductor Testing



- CDM fails during a ramp-up phase can also occur for parts with 500 V CDM and beyond.