System Level ESD – Expanded
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- EDA Vendor: 15%
- OEM - Mainframe: 20%
- OEM - Mobile: 20%
- OEM - Auto: 20%
- Consultants: 15%
- University: 10%

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PREFACE

The topic of System Level ESD was addressed by the Industry Council in two parts:

• Part I: “Common Misconceptions and Recommended Basic Approaches”
  – Published as JEDEC Document JEP161

• Part II: “System Level ESD: Implementation of Robust ESD Designs”
  – Published as JEDEC Document JEP162
Outline

• What is System Level ESD?
• Component vs. System Level ESD
• Misunderstanding about System Level ESD
• “System Efficient ESD Design” or SEED
  – Basic SEED
  – Advanced SEED
• Tools for System ESD Design
• Advanced Topics
• Future of System Level ESD
Outline

• What is System Level ESD?
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A system consists of embedded ICs and other electronic components to form a consumer/automotive/military/medical product that can be exposed to various random uncontrolled severe ESD events with unspecified waveforms.
System Level ESD

• **What is an ESD Event?**
  - Object becomes charged -> discharges to another
  - Charging levels range from 1 V to 35,000 V
    - Discharge currents range from 1 A to 60 A or more

• **What is a System Level ESD Event?**
  - An electrical system experiences an ESD Event

• **What can happen in a System Level ESD Event?**
  - The system continues to work without problem
  - The system experiences upset/lockup, but no physical failure.
    - Typically referred to as “Soft Failure”
    - May or may not require user intervention
  - The system experiences physical damage
    - Typically referred to as “Hard Failure”
System Level ESD

• **What are some sources of System ESD Events?**
  - Charged Humans
  - Charged Humans with a Metallic Tool
  - Charged Cables (Charger, Headset, USB, HDMI,..)
  - Charged Products themselves
  - Charged Metal Objects

• **How is the Event Transmitted to the System?**
  - An Direct contact to a system I/O pin
  - Direct contact to a system case
  - An arc through a vent hole or seam to a circuit board
  - Pickup of EM radiation from indirect ESD
  - A secondary discharge event within the system
System Level ESD Testing

- **System level ESD (qualification) testing** is intended to ensure that finished products can continue normal operation during and after a system level ESD strike.
  - The IEC 61000-4-2 ESD Test Method is used to represent one particular scenario of a charged human holding a metal object and discharging to a point on the system.
  - This is the most common test method used to assess the ESD robustness of the system.
  - Other test standards (e.g., ISO10605 for automotive, DO-160 for avionics) are used; depending on the application.

- **System Level ESD Test Results**
  - Pass: System continues to work without interruption
  - Soft error that corrects on itself
  - Soft error requiring intervention (reboot, power cycle, …)
  - Physical failure

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Categories of Failures (From Limited Case Studies)

- Common reported causes of system failure are:
  - Charged Board Events (CBE)
  - Cable Discharge Events (CDE)
  - Electrical Overstress (EOS)
  - IEC System Level ESD testing (for the “soft” failures, their relative percentage could be higher)

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• Physical damage was reported more frequently in the 58 case studies tallied by the Industry Council.
• However, system manufacturers report that physical damage occurred less frequently than soft failure.
• System manufacturers do not always report soft failures to suppliers. Because most of the case studies were provided by suppliers, data tends to be weighted towards physical damage.
Outline

• What is System Level ESD?
• **Component vs. System Level ESD**
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## System level ESD vs. Component level ESD

<table>
<thead>
<tr>
<th>Parameter</th>
<th>System level ESD - IEC</th>
<th>Component level ESD HBM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Event example</strong></td>
<td>Charged human discharging through a metallic tool to a system</td>
<td>Charged human discharging through the skin to a component (IC)</td>
</tr>
<tr>
<td><strong>Model</strong></td>
<td>IEC system level ESD</td>
<td>Human Body Model (HBM)</td>
</tr>
<tr>
<td><strong>Environment</strong></td>
<td>End customer’s normal operation</td>
<td>Factory assembly</td>
</tr>
<tr>
<td><strong>Standard example</strong></td>
<td>IEC 61000-4-2 (Powered)</td>
<td>JS-001-2013 (Unpowered only)</td>
</tr>
<tr>
<td><strong>Test</strong></td>
<td>ISO 10605 (Unpowered / Powered)</td>
<td></td>
</tr>
<tr>
<td><strong>R-C network</strong></td>
<td><img src="image.png" alt="R-C network diagram" /></td>
<td><img src="image.png" alt="R-C network diagram" /></td>
</tr>
</tbody>
</table>

✓ The two tests are distinctly different and serve different purposes

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<th>Component level ESD HBM</th>
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<tbody>
<tr>
<td><strong>Peak current</strong></td>
<td>3.75 A / kV</td>
<td>0.7 A / kV</td>
</tr>
<tr>
<td><strong>Typical requirement</strong></td>
<td>8 KV</td>
<td>1 KV (Formerly 2kV)</td>
</tr>
<tr>
<td><strong>Rise time</strong></td>
<td>0.6 ~ 1 ns</td>
<td>2 ~ 10 ns</td>
</tr>
<tr>
<td><strong>Pulse width</strong></td>
<td>~50 ns</td>
<td>150 ns</td>
</tr>
<tr>
<td><strong>Failures</strong></td>
<td>Soft and Hard</td>
<td>Hard</td>
</tr>
<tr>
<td><strong>Application</strong></td>
<td>PC, Cell phone, Modem, etc…</td>
<td>IC</td>
</tr>
<tr>
<td><strong>Tester examples</strong></td>
<td>KeyTek Minizap, Noiseken ESS2000</td>
<td>KeyTek Zapmaster MK2, Oryx</td>
</tr>
</tbody>
</table>

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Courtesy: Jae Park, TI
Waveforms of Component HBM and System Level

- System level ESD gun test has to be performed under powered conditions
- For powered systems there are two failure mechanisms
  - Destructive fail
  - Functional/Operational fail
- Improving the component ESD levels will not solve this issue
- There is no clear correlation of system level performance to the HBM robustness

4 kV HBM is not the same as 4 kV System Level IEC!
Component Vs. System ESD Comparison

- **HBM Test**: closed circuit test where the ESD pulse is applied between 2 or more pins of an unpowered part.
- **CDM Test**: static charge is built up on an unpowered part and then discharged from a single pin to a low resistance ground.
- **System Level Test**: a device is mounted on circuit board within a user ready and operating system.
  - Stress is applied between specific locations on the system and the power supply reference ground.
  - Peak currents, rise time and discharge duration differ from HBM/CDM.
Component Vs. System ESD Comparison

- **Pass/Fail Criteria**
  - **HBM/CDM**: based on physical damage
  - **System Level ESD**: based on temporary system upset and/or physical damage

→ The discharge paths and the associated currents will be different for these stress methods, therefore **NO correlation can be expected**
What is the interacting dependence between component protection and system level protection?

- Improving HBM and CDM often makes it harder to Protect the System
- HBM & CDM circuit design assumes no power to the circuits
- HBM and CDM do not address soft failures
- HBM & CDM circuit design assumes no external components
- On the other hand, system level ESD robustness is affected by all components and the board design
Case studies A through G represent data on products which had failure voltages characterized for both HBM and IEC based system level test.

Data indicates no correlation of HBM failure voltage to IEC failure voltage.

This disparity between the two test methods is due to the fundamental differences in the stress waveforms and in the way the stress is applied during the tests.
“Improving the component ESD levels would not improve the system level ESD performance.”

Following this, since ICs are now designed for lower component ESD levels, why would this not be reflected by a sudden change in the overall health of a system for its ESD capability?

• The overall health of a system is dependent on a comprehensive approach to the protection methodology that includes a number of factors including on board protection components, optimized board signal routing, component packaging and, as a last line of defense, the component level protection.
Understanding System Level ESD Protection

• Aren’t Integrated Circuits Tested for ESD?
  – Yes, they are tested for HBM & CDM

• Doesn’t that mean they will be fine in a system?
  – No, they are tested to **assure that** they can survive manufacturing in an controlled ESD environment

• But won’t that help?
  – No, this is a misconception. Good component ESD does not mean a system is comparably protected.
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Industry Wide Challenge

There is a prevailing misunderstanding between the IC Suppliers and System Level Designers regarding:

• ESD test specification requirements of system vs. component providers;

• Understanding of the ESD failure / upset mechanisms and contributions to those mechanisms, from system specific vs. component specific constraints;

• Lack of acknowledged responsibility between system designers and component providers regarding proper system level ESD protection for their respective end products.
Industry Wide Challenge

Why wouldn’t you expect to see correlation between device level and system level testing?

• Since the tests are done in different environments (unpowered versus powered or stand-alone versus on board) along with the different stress current wave shapes for the two tests, it is not surprising that they would lack correlation.

• However when external pins are involved, a higher component level ESD on these pins could mean less load for the on-board clamp to handle. But this type of approach, while being impractical and unpredictable, also detracts from the need for an efficient system ESD design compatible with the on-board clamp.
Is 2kV "HBM" testing the same as IEC Zap Gun testing?

- Unfortunately, there is sometimes confusion in the comparison of the two methods.

- Actual human contact to an IC component is simulated / tested with the Human Body Model Tester, which results in ESD stress between two or more component pins.

- This is completely different from the IEC Test method where the Zap Gun is used to test a system case, board or board connector and may or may not stress an IC.
Why would designing for higher HBM on chip not be advantageous for system protection design?

- Designing high IC HBM involves lowering the clamp triggering level and its on-resistance to reduce power dissipation on chip. But these design changes often make it harder for on board protection to be successful.
Industry Wide Challenge

What are the problems for an On-Chip System Protection Strategy?

• Misconception
  - Is necessarily a cheaper solution than off-chip design
  - A single IC can cover protection for the whole system

• Added IC level costs
  - ~30% increase in area
  - Need for a larger package
  - Increased design cycle time

• Uncertainty
  - No information on other components on the board
  - How the test would be done
  - To design for surviving the worst-case IEC stress
  - Additional system protection measures may be needed
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System Efficient ESD Design

• For efficient system ESD design, the “Internal Pins” versus the “External Pins” must first be defined.

• The interaction from the external pin stress to the internal pin must then be analyzed.

• Both Internal Pins and External Pins should meet minimum HBM and CDM levels as defined by component handling requirements; however, this is not a system requirement.

• For achieving system level ESD robustness, the External Pins must be designed with a proper system protection strategy; which is independent of their HBM/CDM protection levels.
Differentiation of Internal Vs. External Pins

Circuit Board

System

Internal
External

Stress Access to External Pins

- As identified here all the external pins are stressed with the IEC pulses
- What is the interaction to the corresponding interface pins?
Differentiation of Internal Vs. External Pins

Other types of pins, including Inter-chip, and the effects of Cross-Talk have to be considered.

Would this be a problem when reducing the HBM level from 2kV to 1kV or even 500V? Explained in slides 44 and 45.
OEM/IC Supplier Cooperation

*How can system/board designers get the required information about the IC IO behavior?*

- First, both the OEM and the IC supplier must define the ‘external pins’.
- Following this, the IC supplier provides the TLP curve of the pin of interest with either bias applied or without bias. This depends on the pin application in the overall system board.
- The measured TLP response at the pin will not only represent the pin’s internal ESD clamp behavior, but it will also include the IO design behavior to the transient pulse analysis.
Designing for the Overall System

- Internal Pins and External Pins should meet minimum HBM and CDM levels as defined by component handling requirements.
- System ESD protection design involves an understanding of the system, independent of component ESD levels.

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System-Efficient ESD Design (SEED) Concept

- Utilizes existing component level ESD protection as a starting point for design
- For an efficient system protection design, the IC pin’s breakdown characteristics play a critical role
- Effective IEC protection design can be achieved for any IC pin that interfaces with the external world

External Component Response Characterization linked to the IC Pin’s Transient Characteristics
Do all pins on a device need to be tested using system level events?

- Only the external pins (e.g. USB data lines, Vbus line, ID and other control lines; codec, and battery pins, etc) need to be tested if the IC is not protected with on-board components. However, if the pin is protected by on-board components, TLP characterization of the pin is more useful.

- Other internal ESD sensitive pins (e.g. control pins, reset pins, and high speed data lines, etc.) can be inductively coupled during a discharge to the case and/or to an adjacent trace of an exposed pin undergoing system testing.

- These sensitive internal pins need to be identified and may need to be monitored during system level events.
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Basic SEED Approach

- The residual pulse after external clamp is matched with the TLP information of the interface IC pin for different time domains
- The board components are tuned for robust IEC protection

- This method can be effective for the case of hard failures

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USB2 Interface  Example with SEED

- 4 Pins to be protected (D+, D-, ID, VBUS)
- High Speed Data Rate (480Mbit/s)
- EMI/ IEC ESD and Signal Integrity requirements
Evaluation Board (Reference Platform)

Form Factor representative of a Smart Phone Application Board
Simulation Methodology Overview

1. CDM Info : Ip
   TLP Info : It2

2. TLP Info
   100-ns Pulse IV
   V(f)

3. TVS Response to IEC Pulse

4. Residual Pulse from Board Design

Diagram:
- Power IC
- OMAP IC
- CFB
- CMF
- TVS
- USB Interface Diagram
- Receptacle
- VCC pin
Simulated Current Waveform at IC pins

- Transient simulation
- +8kV at D- Connector pin
- Additive contribution of each elements
- Suppression of the First IEC Peak by the PCB
- EM simulation $\rightarrow$ [S] model
- Post CMF interconnect
  - $\text{Leq} \approx 30 \, \text{nH} / \text{Req} \approx 0.9 \, \Omega$
  - Raise isolation impedance between TVS and IC
  - More effective to mitigate the first IEC peak (inductance)
• Under an IEC event
  • Insertion impedance defined by Load Mode
  • Load formed by On-Chip/Off-Chip On Resistance (positive or negative to ground) and PCB interconnect
But How Is Cross-Talk Addressed?

Automotive Application Example

- **Concern:** Crosstalk between long PCB traces leads to overstress at internal pins during system level ESD stress
- **Reality:**
  - Analysis of CANH and µP pins show low energy coupling between PCB traces when system level ESD pulses are applied [zur Nieden et al., German ESD Forum, December 2011]
  - Minimum ESD robustness of internal pins is more than sufficient to handle typical induced energies of system level ESD pulses
  - This is true even at 8kV IEC stress (see simulation reference on the next slide)
Crosstalk to Internal Pins

Friedrich zur Nieden, Stanislav Scheier, Stephan Frei; „System level ESD on-PCB coupling”, report 2011.

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Summary of Basic SEED (I)

- It is often misunderstood that a high level of HBM ESD protection will adequately protect a component from IEC testing.
- Even pins with >10kV HBM may not survive 3kV IEC.
- Thus the external TVS plays a major role; however, the TVS alone would not still guarantee that the 8kV IEC requirement will be met.
- A detailed simulation approach with understanding of the role of the various elements on the board becomes essential for achieving effective protection.

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Summary of Basic SEED (II)

- Simulation approach with System Efficient ESD Design (SEED) can be very valuable to achieve good IEC performance with minimum impact on the signal integrity (USB or HDMI, etc.)
- The SEED approach is useful for preventing hard failures
- Full understanding of the frequency response of all the elements on the PCB must be included for a successful design
- But for addressing soft failures “Advanced SEED” is necessary
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Advanced SEED

• System ESD can impact an entire system and can create both “hard” and “soft” failures.
• So called soft failures may involve complex EMC/EMI effects and also some Transient Latchup (TLU) phenomena.
• These issues require recommendations for component and system level manufacturers regarding proper protection / controls and best practice ESD design for EMC/EMI
Objectives for Advanced SEED

• Provide details on effective system ESD protection issues and designs
  - Address the more complex EMC/EMI issues and the techniques and tools for understanding the associated system soft failures
  - Demonstrate that system ESD protection can only be solved by combined efforts of the IC Suppliers and System Application Designers
Assumptions and Requirements

- Efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level.
- An appropriate characterization of the components is required.
- Need of a methodology to assess the whole system using characterization data, such as by simulation.
- Application to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)).
- Need of improved communication between the IC supplier, the OEM and the system builder.
SEED Categories-1

SEED Category 1:
External pin experiences hard failure due to a direct ESD zap (failure root cause: high pulse energy at exposed line)

OR

Non-external pin experiences a hard failure due to an indirect ESD zap (failure root cause: high transferred pulse energy to non-exposed lines)
SEED Categories-2,3

**SEED Category 2:**
Pin experiences a transient latch-up event which can lead to either a hard or soft failure (failure root cause: current injection into the substrate which is too high)

**SEED Category 3:**
Describes protection of an IC experiencing soft failure due to low amplitude transient bursts in the system during an ESD zap (for example, this may be caused by degraded signal integrity of an exposed line, cross-talk to a neighboring line or supply noise).
## Summary of SEED Options

<table>
<thead>
<tr>
<th>Categories</th>
<th>Strategy</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEED 1</td>
<td>System ESD simulation using TLP characterization</td>
<td>Also requires analysis of the PCB trace elements</td>
</tr>
<tr>
<td>SEED 2 and SEED 3</td>
<td>Use EMC best design methods</td>
<td>Also requires detailed analysis of PCB behavior and EM scanning tools</td>
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Tools

- Troubleshooting to Determine the Cause of Failures
  - Hard Failures
  - Soft Failures
- New Technologies for Determining Root Cause of Failures
  - Susceptibility Scanning
  - New Software Methods
  - System Specific Test Boards
Basic Vs Extended SEED

**Basic SEED**
- Conducted discharge leads to damage
- Simulations must include analysis of the PCB trace elements

**Extended SEED**
- Covers also soft fails due to low injected currents and EM radiation
- Needs additional EM scanning tools
Discharge via wired network connected to PCB port

(A) ESD and EMI energy spread deep into the system, potentially creating secondary problems.

(B) ESD and EMI energy guided out of the system as soon as possible, keeping "noisy" and "quiet" areas isolated. Best practice.

(C) ESD and EMI energy primarily filtered at the system periphery. Some residual noise/energy continues on inside, but the level is reduced and does not create additional secondary issues. Best cost/performance tradeoff.

Off-Chip Protection is the ideal approach!
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Advanced Topics (in JEP162)

- Coupling of ESD into Systems and Circuits
  - How Does ESD Couple into a System and Affect a Specific Device During System Level Testing?
  - What Happens When the Charge Gets into the System?
  - Recoverable or “Soft” System Failure Modes
  - System Degradation
  - Hard System Level Failure Modes
Advanced Topics (in JEP162)

- State-of-the-Art ESD/EMI Co-design
- Robustness/Performance/Cost vs. Basic/Advanced/Comprehensive
- Shielding (Prevent Entry)
- Beyond Shielding (Accelerate Exit)
- Component Selection (Interaction, Lack of Info)
Advanced Topics (in JEP162)

- ESD/EMI Budget Strategy (Tradeoff Gamut examples)
- Equipment Ground (Exit for the Pulse)
- Quick Fixes (Copper tape, upgrading components)
- Information Available to the Designer (Conflicting datasheets)
Advanced Topics (in JEP162)

- Primary Goals of ESD/EMI Co-design Today
- Sufficient Signal Integrity and Functionality
- Adequate ESD/EMI Robustness and Compliance
- Cost and Time to Market
Advanced Topics (in JEP162)

• Desired Results vs. Actual Process Reality
• Design Reuse  (Use what worked)
• Revision Decisions (Don't change what worked)
Advanced Topics (in JEP162)

- Post-Design Iterative Improvement (Lab Optimization)
- Robustness Margin Fine Tuning
- Head to Head Component Comparisons
- Software Recovery Methods
- Comprehensive Co-Design Methodologies
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Future Trends

System level will continue to become complex with many other future trends

- Requirements for higher speed USB and HDMI interfaces
- Higher integration in automotive applications
- Higher board integration with increased EMC sensitivity
- Stacked 3D ICs embedded in PCB and SiP
- Demands for cost-efficient solutions
Technology Trends

• New technology directions for both IC designs and applications will start to have impact on how well system level ESD designs can be done

• The impact is from
  - ICs and Microprocessors
  - Automotive Applications
  - IC Packages and Applications
  - Advances in Board Assembly/Technologies
  - Optical Interconnects
  - New Polymer Materials
  - Compatibility to IEC Protection Requirements
DSP and Microprocessors

- SerDes: 20 GB/sec at 20nm - Internal
- DDR:2.3G at 28nm - Internal
- USB and HDMI - External
- RF Antenna low tolerance to capacitance - External

The external pins require special attention for all future system level ESD designs

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Package Trends

• System-in-Package (SiP) needs to carefully match all IC and product interfaces - includes EMC/ESD compatibility issues

• The same IC may contain digital, analog and RF blocks.

• May not be possible to separate noisy RF interfaces on a board from other sensitive interfaces

• For higher board integration more detailed information is needed from Systems on Chip blocks and most likely early EMC/ESD simulations are needed to optimize design
PCB Trends

• Board technologies evolve along with new material and joint technologies.

• SMT with FR-4 printed circuit boards will most likely continue to be the dominating board technology due to low price, etc.

• High volume chips made with the latest efficient silicon processes will provide the best operations and cost efficiency - traditional board technologies and novel IC and Systems on Chip technologies may bring challenges for the system design.
PCB Trends

• Board 3D design with stacked components, embedded components in PCB, System-in-Packages, System-on-Packages and other 3D constructions

• Special 3D designs like the Molded Interconnection Device (MID)

• Nanoscale features will be Flexography printing and Nano-imprint lithography.

• Advances with printable electronics rely mainly on material technology development
System Trends

- Technology advances will bring more functions to electronic devices in all product ranges. Advanced sensors, high speed display technologies (3D displays), >3 GHz data transmission and optoelectronics will most likely add system complexity.
Summaries and Status:
JEP161 and JEP162
Highlights of JEP161

Summary

• ESD test specification requirements of system providers must be clearly understood

• Using component level ESD specifications as a basis to address robust system designs must be discouraged

• Understanding of system ESD failures and upset mechanisms is important

→ Shared responsibility between system designers and component providers is critical
Main Message of JEP161

- A novel design concept called System Efficient ESD Design (SEED) can address hard failures.
- IC suppliers (and discrete protection diode suppliers) are requested to characterize their components in the high current regime (by TLP) and provide system ESD relevant models to system designers.
- System designers are responsible for assessing (e.g. simulating) the system protection (PCB & components) based on the models and data delivered by component supplier.
Main Message of JEP162

- Efficient ESD design can only be achieved when the interaction of the various components under ESD conditions are analyzed at the system level.
- An appropriate characterization of the components is required.
- This requires a methodology to assess the whole system using characterization data, such as by simulation.
- Can be applied to system failures of different categories (such as hard, soft, and electromagnetic interference (EMI)).
- The above require improved communication between the IC supplier, the OEM and the system builder.
JEP161 Status

• Published by JEDEC in October 2011
• Also available at the ESD Assoc. web site
• And at the Industry Council web site
• //www.esdindustrycouncil.org/ic/en/news
JEP162 Status

- Published by JEDEC in February 2013
- Also available at the ESD Assoc. web site
- And at the Industry Council web site

- Cross-reference:
  - JEITA Technical report EDR-4709
  - This is a parallel Japanese Document
What is the Difference Between JEP162 Versus EDR4709?

• Both white papers emphasize that component level ESD should not be coupled with system level ESD

• Industry Council documents JEP161 and JEP162 recommend using TLP (powered and unpowered) analysis to understand System Level ESD design

• EDR-4709 currently is experimenting with Powered MMM (Modified MM) but plans to harmonize with the TLP method in future
Backup Slides
Will there be a need for a device ESD target level, to confirm system level performance?

• No. System level performance is a combination of on-chip ESD protection, on-board protection components and system mechanics design.

• The detailed properties of the IC’s ESD protection (such as turn on voltage, resistance, and maximum withstand current) are much more important than the IC’s HBM and CDM withstand level measured in voltage.
If system level ESD testing does not meet the required system level performance, isn’t having the highest component level HBM ESD target the best approach?

• This would only give a false sense of security and could result in extensive cost of analysis, customer delays and a circuit performance impact. (Remember, higher HBM ICs may be harder to protect!)

• System ESD protection depends on the pin application and therefore requires a different strategy.

• System level ESD is clearly important, but targeting and relying on excessive component level requirements could pull resources away from addressing and designing better system level ESD.
It is often heard that the IEC 61000-4-2 pulse is a superposition of a CDM and a HBM pulse. Can IEC 61000-4-2 ESD testing replace CDM and HBM testing?

• Looking at the two peaks in an IEC 61000-4-2 pulse, the time duration is indeed comparable to a CDM and HBM pulse.

• However the required levels and discharge nature are completely different.

• This is because CDM is intended for component level testing while IEC61000-4-2 is intended for system level testing.
If a component with the new lower ESD levels starts showing high levels of system failures how will the industry address this?

• First, an investigation comparing ICs from provider A and provider B should look at the details of the component level ESD designs, not just the component failure levels in volts.

• Second, the OEM should share the system level ESD test results with the IC providers. For example, if IC provider A fails and IC provider B (2nd source) passes. IC provider A needs to investigate why their IC fails.

• Next, the OEM should review their ESD protection design for further improvement for both IC suppliers. This type of dialogue is important in the future.
Is there a correlation between device failure thresholds and real world system level failures?

• There is rarely correlation between device (IC level) failure thresholds and real world system level failure in the field.

• Device failure thresholds are based on a simulated ESD voltage and current directly injected into (or extracted from) the device (IC) with the device in a powered down condition.

• Real world system level failures in the field occur in many different conditions, most of which are powered.
Does SEED reproduce real, physical behavior of a board and IC?

- SEED is a design concept whose goal is to attenuate damaging current pulses before reaching the internal IC pin.

- So in this sense, it must first model what the physical effect would be on an IC pin resulting from an IEC stress at the external port of the PCB.

- What it represents for the board depends on how well the scenario is represented during the SEED analysis.