

Flash Storage Trends & Ecosystem

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Agenda

- Introduction
- Trends
 - Wireless Industry Trends
 - Memory & Storage Trends
- Opportunities
- Summary

QCT Product Groups

Cellular
Products
Group

(CPG)

Wireless
Handsets



CDMA, EVDO, GSM/GPRS,
EDGE, WCDMA, HSPA

Computing
&
Consumer
Products

(CCP)

Connected
Consumer Devices



POWERED BY
snapdragon™

Connectivity
&
Wireless
Modules

(CWM)

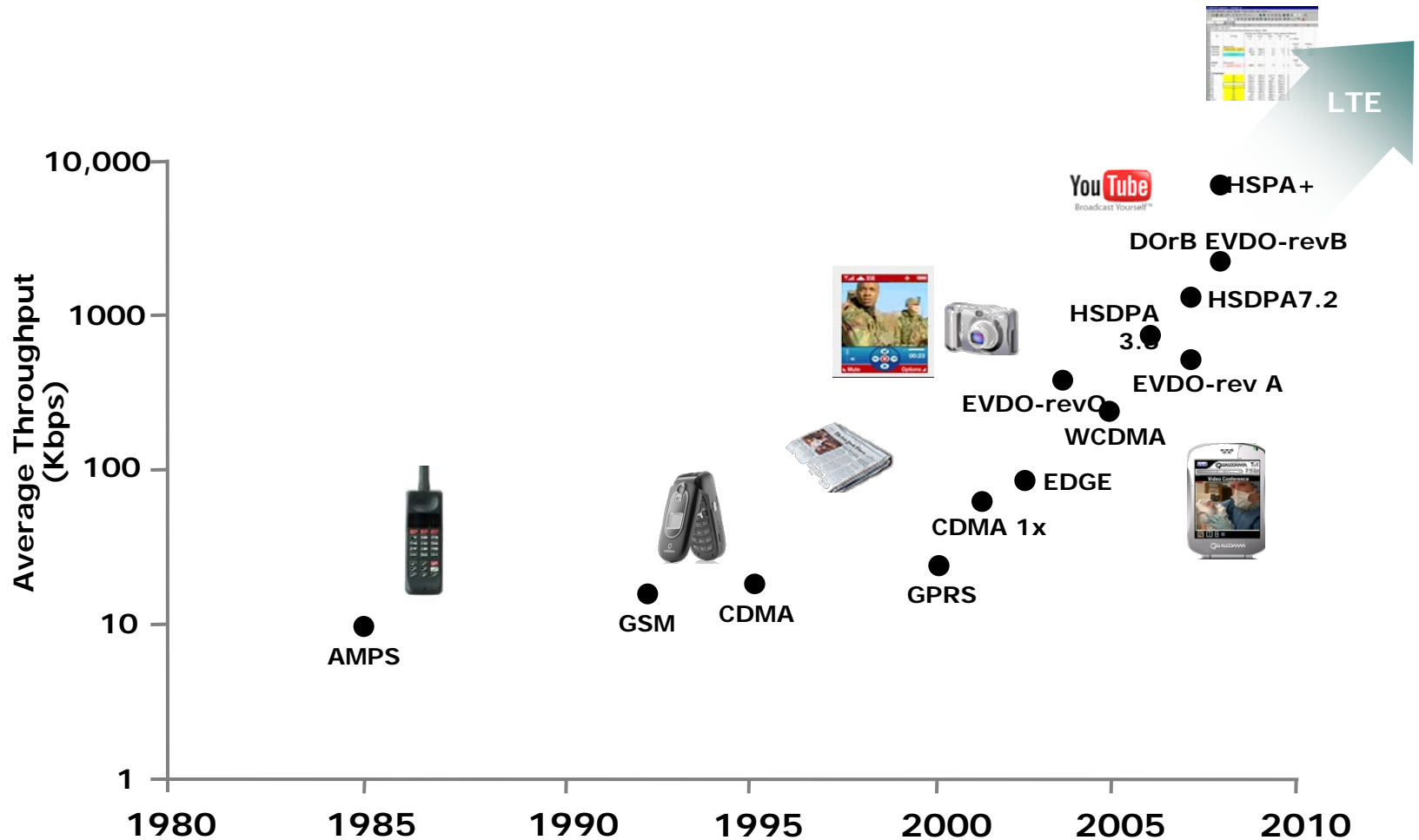
Connected Mobile
Computing



Connectivity



Integration with CPG and CCP Platforms



Wireless Industry Moving Beyond Voice

More Bandwidth → Increased Data use → Advanced Mobile Devices

User trends shift from non-connected to connected, wired to wireless

Simple Communication

Download

Download & Upload

Real-Time Delay Sensitivity

Seamless Fixed Mobile Convergence

Voice & Text

- Voice
- SMS/Email



Streaming

- Music/Ringtones
- Video
- Web Browsing



User Generated Content

- Mobile 2.0
- Social Networking
- Media Sharing
- Collaboration
- Mobile Advertising



Rich Communication

- VoIP
- PTT/PTM
- Video Communication
- Multiplayer Gaming



Seamless Connectivity

- Ubiquitous Broadband
- Apps store
- Consumer Electronics



Mobile services becoming the center of life



Handset
< 2"



Feature
Phone
2.5"



Smartphone
< 3.5"



SmartPhone →
Tablet/SmartBook

~4" → 7" – 12"



Wireless
Notebook
> 12"

Feature phone/smartphone:

- Communication (voice, text, email)
- Full internet
- Entertainment
- Navigation

New Device Categories



Mobile
Professionals

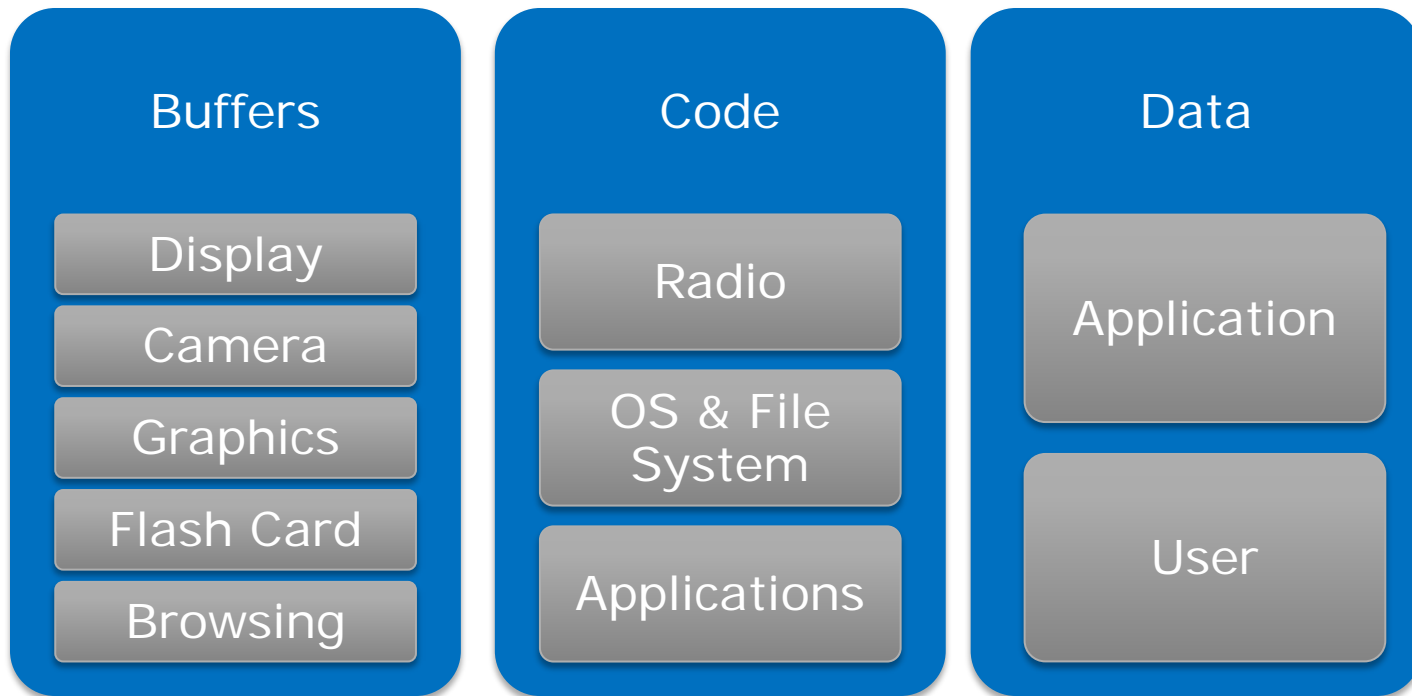


Families

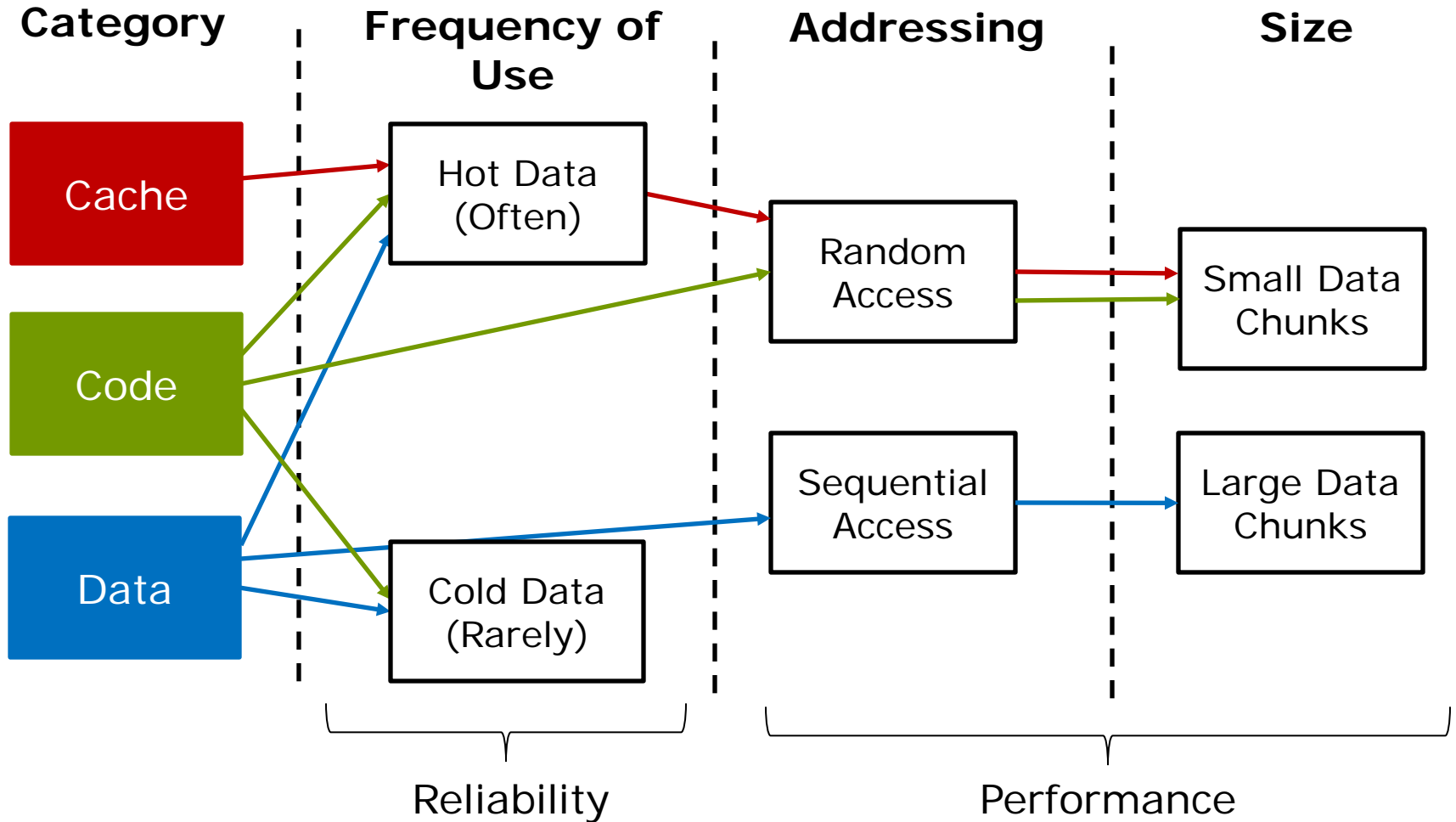
Traditional laptop:

- Productivity
- Internet/E-mail
- Entertainment
- Navigation

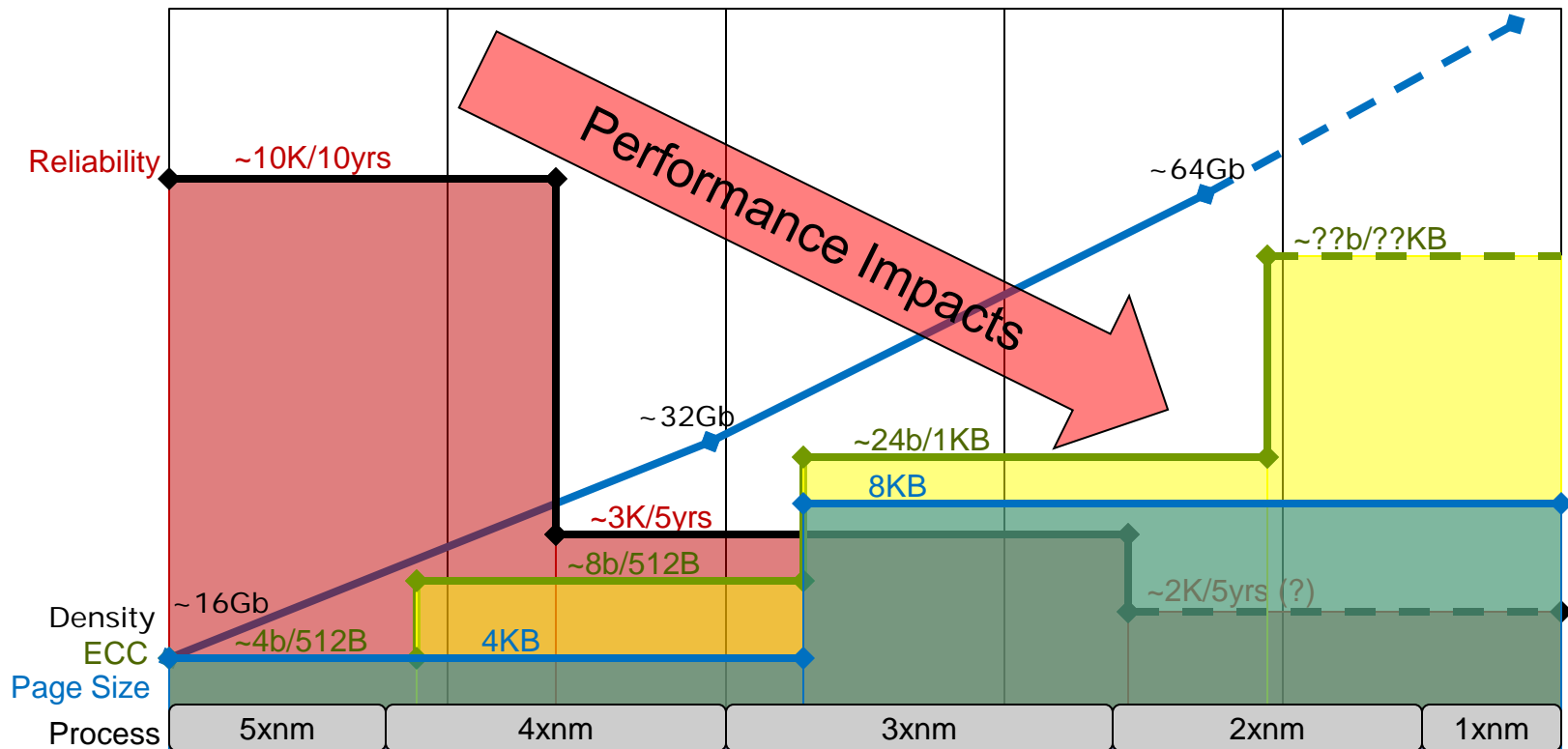
Application Data Types



Flash Data Type Characteristics



NAND FLASH Technology Trend



Problem Statement: Applications vs. Storage

- Mobile Applications & its Computing Model
 - “All about Multimedia” & more storage!
 - Phone: Change from Simple talk/listen to smartphone with increase data usage
 - OS: Change from Single-thread to multi-threaded environment
 - **Result: Demand for higher random IOPs performance**
- FLASH Technology
 - FLASH: NOR – NAND – MLC NAND – manage NAND
 - Migration from Single-Level Cell (SLC) to Multi-Level Cell (MLC)
 - Reliability Degradation
 - lower than endurance (3K or lower) & retention (5K or lower) for MLC FLASH
 - Higher ECC, 24bits or higher per 1KB block
 - Larger page size, 8KB block & possibly higher
 - **Result: Performance degradation in raw NAND**

Opportunities Within JEDEC

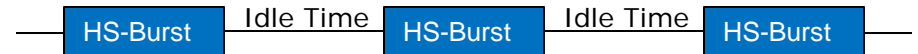
- Size & pincount reduction on SoC
 - Pincount will limit SoC size reduction
 - Stacked memory (SIP, POP) continue to mature
 - TSV (Through Silicon Via)... are still “emerging”
- Serial Interface
 - Minimize pin count. Today SoC pincount is ~600 & growing
 - SoC Process shrink continue to migrate to 2xnm
- Proven programming model
 - SCSI architecture & commands (SW re-use)
 - Standard Host Controller Interface (HCI) definition
- Optimization for performance & power
 - Optimization of device architecture with Increase parallelism (Multi-plane & Multi-LUN support)
 - eMMC Standardization for today managed NAND
 - JEDEC UFS is the next Generation NVM memory

Serial Technologies

- There are limitation on current CMOS IO, ~250MHz; ~533MHz for PoP
- To improve performance CMOS IO, pincount must increase or look at other aspects for improvement
 - Clock architecture & methodology
 - I.e. Multi-phase & DLL
 - Complex IO design
 - Drive Strength
 - Lower signaling Voltage
 - Lower bus loading
 - Termination
- There are multiple Serial technologies in the industry
 - SATA, PCIe, MDDI, MIPI, SPMT, RAMbus, etc.
 - But how to do Serial Interface while optimize for power...

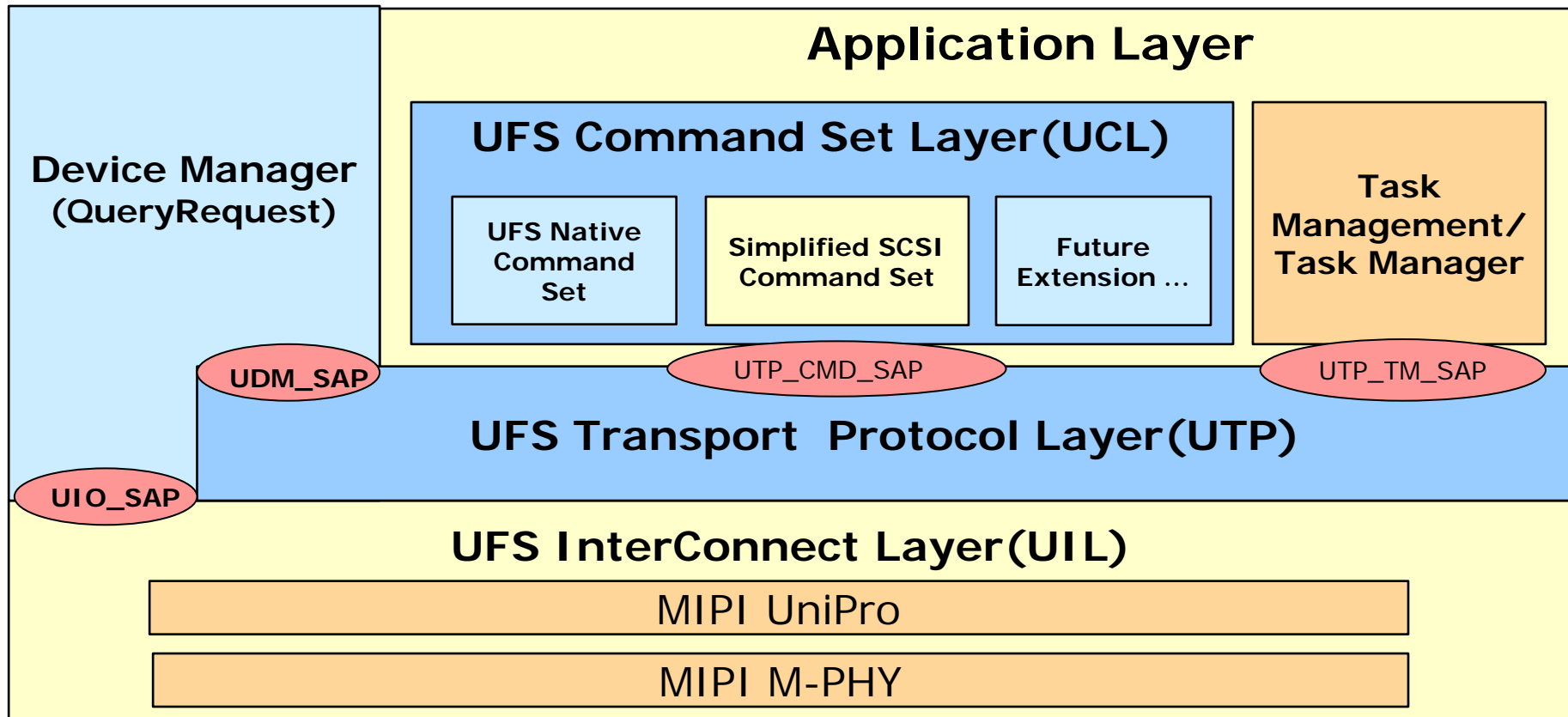
Serial Interface Power Estimate: USB Sideload

- Assumptions
 - Transaction size: 64KBytes
 - Transaction Rate: 30MB/s
 - Flash Write Speed: 30MB/s



Transaction size (Kbytes)	65.5E+3			
Transaction Rate (MB/s)	30.0E+6			
Flash Read/Write Speed (MB/s)	30.0E+6			
	e.MMC4.41	M-PHY (150MB/s)	M-PHY (250MB/s)	M-PHY (500MB/s)
Link Rate(MB/S)	100.0E+6	150.0E+6	250.0E+6	500.0E+6
Peak Utilization	30.0%	20.0%	12.0%	6.0%
Idle Utilization	70.0%	80.0%	88.0%	94.0%
Energy (mW/Gbps)	8.640	6.400	3.789	1.779

UFS Architectural Diagram



SCSI Architectural Model

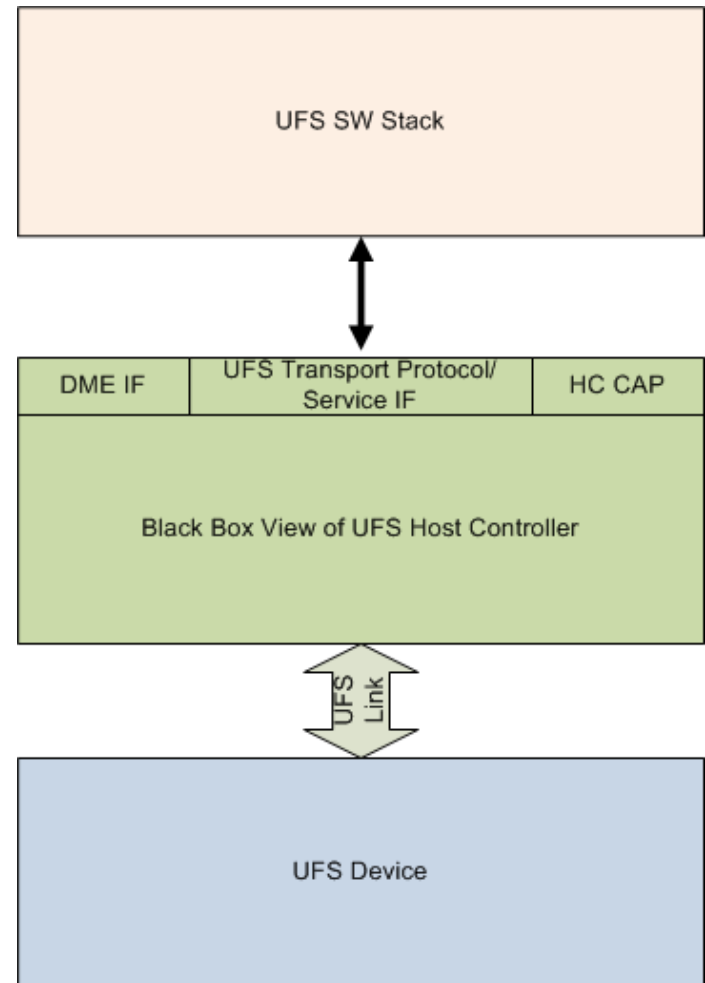
- eMMC today command-response based architecture is limiting
 - Designed for Single-thread computing model
 - Increasing bus frequency will not further improve BW
- Based on SCSI architecture model Multi-threaded computing operation model
 - Command queuing
 - Out-of-order execution
- Well-known architecture model for Host & Device, same as SSD/SAS & USB3 storage
 - Flexible to support small & simple storage device such as USB drive
 - And still support high-performance model such as enterprise computing
- Goal: Re-Use Standard SCSI commands to enable UFS features

UFS Host Controller Interface (HCI)

- Objectives - Provide standard programming interface for UFS
 - Enable the use of common Host/OS Driver
 - Common Register set, for OS driver as well as Low-Level driver
 - Low-level driver can be customized per HW host controller
 - Management of DMA & queues
 - Provide bus/link management capabilities
 - Provide power management capabilities, including device power management
- Optimized interface for different UFS usage models with regards to embedded mass storage, memory card, and UFS bus topology
- Minimize changes to UFS Host SW as the technology matures

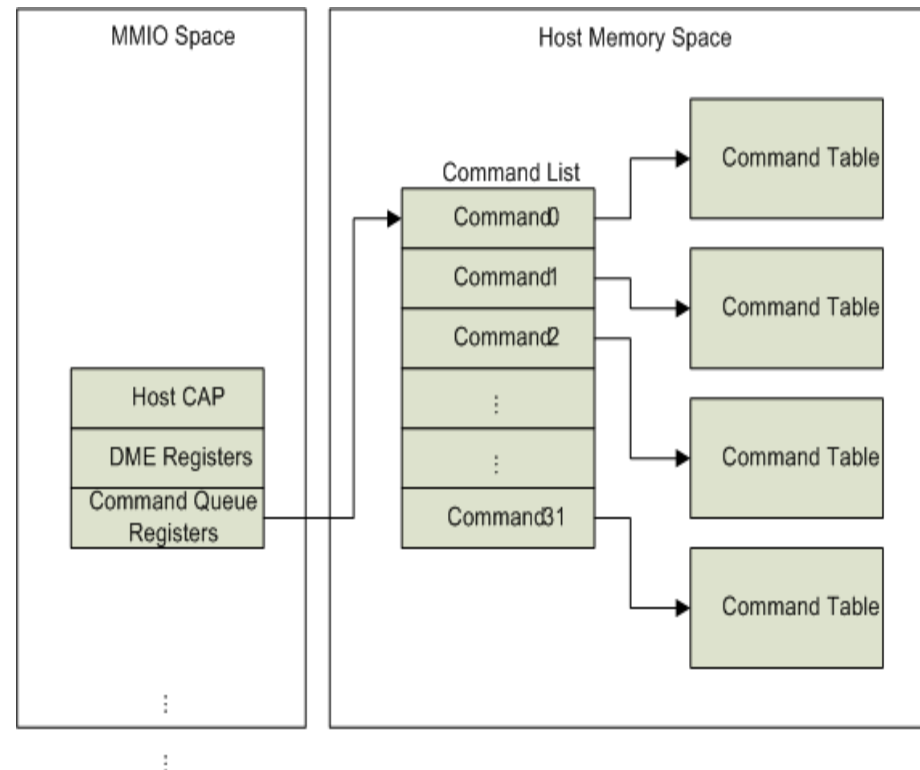
Host Architecture Interface (HCI) Overview

- Device Management Entity (DME) Interface
 - Support Native UniPro DME calls
- UFS Transport Protocol/Service Interface
 - UFS Transport Protocol (UTP)
 - UFS Transport Service IF
 - UFS Native Command IF
- Host Controller Capability (HC CAP)
 - Host version
 - Host Controller Capability
 - Host Controller Configuration



Host Controller Interface (HCI) Architecture

- Command Queuing
 - Up to 32 Commands/Service Calls can be queued
 - Command/Service call reordering by SW
- DMA Operation
 - For command/data fetching
 - For data delivery
- Native UniPro support
 - Direct access to UniPro DME Service Access Point Interface at host register
 - Local control/configuration
 - UniPro layer (L4-L1.5) control/configuration
 - M-PHY control/configuration
 - Remote device control/configuration
 - Device reset
 - Device control/configuration
- Doorbell register to start command execution



Optimization: Command Queuing

- Need to migrate to multi-threaded operations
 - Single thread operation of e.MMC will limit device peak BW
- Command Queuing & Native Command Queuing existed today with SATA/SCSI, supporting up to 32 commands for SSD
- Goal - improve random read and write performance while minimize Host SW interaction
- Impact - Device Firmware complexity increase, added management functions
- Out-of-Order Execution. Device can service commands strategically out of order to achieve greatest performance

Other UFS Optimizations

- Background operations
 - Define time for device operations to occur
 - Define the power-mode for these operations
- Power Management
 - Power modes
 - Notification. Indicate power mode transition
- Secure operations, including write & erase operations
- Dynamic Capacity
- Data reliability
 - Reliable write
- Enhance area
- Partitioning based on performance/reliability requirements

Conclusion

- Changes in mobile computing model dictates changes to storage device & its interface
- Serial interface
 - Serial technology: Power, performance, and pin count optimization
 - JEDEC-MIPI agreement allows the use of M-PHY & Unipro, for Jedec NVM & DRAM solutions
 - JEDEC UFS is the 1st specification resulting from this agreement
- SW Architecture advantages
 - SCSI Architecture & Command set
 - UFS HCI definition
 - Implications: added complexity to the storage device
- **Result – Quicker adoption of UFS**
 - Qualcomm committed to JEDEC Standard interface developments