Migrating to LPDDR3:

An overview of LPDDR3 commands, operations, and functions.

LPDDR3 Symposium 2012
Contents

• LPDDR2 to LPDDR3 migration
• LPDDR3 Commands: highlights
• LPDDR3 Operations: highlights
• LPDDR3 AC Timing and Signaling
LPDDR3 Objective

- **Increase bandwidth 50% LPDDR2-1066**
  - From 8.5 GB/s\(^1\) to 12.8 GB/sec\(^1\)

- **Fast time-to-market**
  - Re-use existing LPDDR2 infrastructure
    - No change or limited changes to interface, command protocol, state machine, etc.
    - Only changes which enable the higher speed operation should be considered.
    - SOC vendors and DRAM vendors should re-use as much as possible from LPDDR2 in order to meet very aggressive time-to-market.

1. 2-channels
# LPDDR3: Key Features Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>LPDDR2-S4</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface/Bond Pads</td>
<td>LPDDR2</td>
<td>Same w/additional ODT pin</td>
</tr>
<tr>
<td>Command Protocol</td>
<td>LPDDR2</td>
<td>Same</td>
</tr>
<tr>
<td>Array Pre-Fetch</td>
<td>4n</td>
<td>8n</td>
</tr>
<tr>
<td>Speed Bins</td>
<td>533,400,333,266,200</td>
<td>800,667</td>
</tr>
<tr>
<td>Read/Write Latencies</td>
<td>8/4,6/3,5/2,4/2,3/1</td>
<td>12/6,10/6 or optional WL=9</td>
</tr>
<tr>
<td>Memory Densities</td>
<td>64Mb – 8Gb</td>
<td>4Gb/6Gb/8Gb (16/32Gb TBD)</td>
</tr>
<tr>
<td>Burst Lengths</td>
<td>4,8,16</td>
<td>8 only!</td>
</tr>
<tr>
<td>Burst Sequence</td>
<td>Sequential, Interleaved</td>
<td>Sequential only!</td>
</tr>
<tr>
<td>Drive Strength</td>
<td>34,40,48,60,80,120</td>
<td>34,40,48 + asym options</td>
</tr>
<tr>
<td>ODT</td>
<td>Not supported</td>
<td>Added!</td>
</tr>
<tr>
<td>Low Power Features (PASR, TCSR, DPD, etc.)</td>
<td>Supported</td>
<td>Supported</td>
</tr>
</tbody>
</table>
LPDDR3: Addressing

- Overlap between LPDDR2/3 at 4-8Gb.
  - Same addressing for maximum IP re-use from LPDDR2
- Additional 16Gb & 32Gb definitions
  - 32Gb TBD – feasibility still to be determined.
  - 16Gb addressing defined, but refresh requirements still TBD.

### Table 3 — LPDDR3 SDRAM Addressing

<table>
<thead>
<tr>
<th>Items</th>
<th>4Gb</th>
<th>6Gb</th>
<th>8Gb</th>
<th>16Gb</th>
<th>32Gb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Banks</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>TBD</td>
</tr>
<tr>
<td>Bank Addresses</td>
<td>BA0-BA2</td>
<td>BA0-BA2</td>
<td>BA0-BA2</td>
<td>BA0-BA2</td>
<td>TBD</td>
</tr>
<tr>
<td>( t_{REFI}(\text{us})^2 )</td>
<td>3.9</td>
<td>3.9</td>
<td>3.9</td>
<td>3.9</td>
<td>TBD</td>
</tr>
<tr>
<td>x16 Row Addresses</td>
<td>R0-R13</td>
<td>R0-R14(^4)</td>
<td>R0-R14</td>
<td>R0-R14</td>
<td>TBD</td>
</tr>
<tr>
<td>Column Addresses(^1)</td>
<td>C0-C10</td>
<td>C0-C10</td>
<td>C0-C10</td>
<td>C0-C11</td>
<td>TBD</td>
</tr>
<tr>
<td>x32 Row Addresses</td>
<td>R0-R13</td>
<td>R0-R14(^4)</td>
<td>R0-R14</td>
<td>R0-R14</td>
<td>TBD</td>
</tr>
<tr>
<td>Column Addresses(^1)</td>
<td>C0-C9</td>
<td>C0-C9</td>
<td>C0-C9</td>
<td>C0-C10</td>
<td>TBD</td>
</tr>
</tbody>
</table>

\(^{1}\) Only relevant for x32 address.
LPDDR3: Performance

Peak Throughput for Mobile Platforms
(GB/s)

2010 2011 2012 2013 2014 2015

LPDDR2
LPDDR3
WideIO
WideIO-2
LPDDR4

2X 4X

Global Standards for the Microelectronics Industry
LPDDR3: Performance

• 1333/1600 speed bins
  – $8n$ array pre-fetch to support higher $t_{CK}$
  – Min Burst Length 8 supported
  – RL/WL/$n$WR support for each new speed bin
    • Note WL “set B” support
    • Additional RL/WL settings allow for frequency scaling to intermediate speeds with optimized latency settings. Use next higher speed bin timing specs.

• Future support for higher speeds (266MHz DRAM core)
  – LPDDR3e speed extensions under discussion, to support 1866/2133 Mbps (target).
LPDDR3: Power

- LPDDR2 -> LPDDR3: no change in $V_{DD}$
- Larger pre-fetch, higher R/W power
- Faster tCK: higher IO power

Low-Power DRAM?

- Power efficiency (pJ/bit) improvement with higher performance – performance increase out-gains power increase...
  - 2-ch LPDDR2 delivers 8.3GB/sec at 533MHz, approx 11.9pJ/bit
  - 2-ch LPDDR3 delivers 12.8GB/sec at 800MHz, approx 9.2pJ/bit

- Higher performance also allows for faster data transfer of fixed quantity resulting in longer idle time for additional power savings.
**LPDDR3: Low Power Features**

- TCSR – same feature as LPDDR2
- PASR – same as LPDDR2 (identical bank & segment masking as S4)
- DPD – supported
- Power-down mode
- Self-refresh mode
- New requirements:
  - $t_{CPDED}$ required for PD/SREF/DPD entry
  - $t_{MRRI}$ required upon PD exit
    - Ensures output buffers do not have worst-case scenario after power-down exit.

Controller backward compatibility to new specs ensured.
LPDDR3: Low Power Mode

Changes

- $t_{CPDED}$

- $t_{MRRI}$
LPDDR3: Power Management

- Higher clock speed means higher power, potential thermal concern (esp. PoP).
- Power management features and methods may be employed
  - Expect that LPDDR3 may operate in elevated temperature range (+85°C to +105°C).
  - MR4 die temp sensor polling enables operation in elevated temp region with refresh de-rating.
  - Per-bank refresh enables user to run in extended temp range without performance degradation.
    - 17% performance hit when running all-bank refresh at 4x $t_{REFI}$ elevated temperature refresh requirement.
    - Concurrent bank R/W operations with per-bank refresh allows data bus to remain active. (Watch command bus activity though!)
LPDDR3: Power Management (continued)

- Clock frequency scaling
  - Utilize alternate RL/WL settings for optimization at a given scaled frequency.
  - Optional RL3 setting (see MR0) for <166MHz enables efficient low-frequency operation.

- High speed operation allows for shorter time to transfer a fixed amount of data – utilize power-down between data transfer for average power reduction.

- Termination will consume power. Optimize ODT and OBT based on SI analysis
  - Multi-rank power control must consider ODT pin connections. Rank0 cannot provide termination for Rank1 if in SREF mode.
Contents

- LPDDR2 to LPDDR3 migration
- **LPDDR3 Commands: highlights**
- **LPDDR3 Operations: highlights**
- LPDDR3 AC Timing and Signaling
LPDDR3: Command TT

- With need to support only BL8, no longer support truncated bursts.
  - No BST command
  - WIW/RIR forbidden

5.5.1 Writes interrupted by a write (cont’d)

Figure 49 — LPDDR2-SX: Write burst interrupt timing: WL = 1, BL = 8, t_{CCD} = 2
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• LPDDR2 to LPDDR3 migration
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LPDDR3 Operations: Initialization

• Power Ramp / Initialization Updates
  – Changes to enable boot at-speed prior to CA Training (when required).
    • Boot at-speed may not be possible if CA bus requires training.
    • Insertion of CA training period.
    • Boot at reduced $t_{\text{CKb}}$ still supported.
LPDDR3 Operations: Initialization

CA training should be performed prior to ZQ Cal; not required if low-speed boot

MRR not used when booting at-speed
(DQ calibration, CA training not yet performed)
LPDDR3 Operations: MR0

- MR0
  - support for WL setB
    - Similar to additive latency concept in DDR3/DDR4.
    - Optional settings with alternate RL/WL ratios for scheduling optimization in different controllers.
  - RL3 support option
    - Low speed operation
LPDDR3 Operations: MR1

- MR1 nWR/BL
  - Sequential burst support only – subset of LPDDR2 read burst sequence options.

- nWR support expanded using additional nWRE bit from MR2[4] to allow higher speed operation and support asynchronous $t_{WR}$ timing requirement.

<table>
<thead>
<tr>
<th>C2</th>
<th>C1</th>
<th>C0</th>
<th>BL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0B</td>
<td>0B</td>
<td>0B</td>
<td>0B</td>
</tr>
<tr>
<td>0B</td>
<td>1B</td>
<td>0B</td>
<td>0B</td>
</tr>
<tr>
<td>1B</td>
<td>0B</td>
<td>0B</td>
<td>0B</td>
</tr>
<tr>
<td>1B</td>
<td>1B</td>
<td>0B</td>
<td>0B</td>
</tr>
</tbody>
</table>

Table 9 — Burst Sequence

<table>
<thead>
<tr>
<th>Burst Cycle Number and Burst Address Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>6</td>
</tr>
</tbody>
</table>
LPDDR3 Operations: MR2

- **MR2**
  - Write Lev
  - WL set B
  - RL/WL
    - Support for various clock settings, but not all speed bins defined in AC timing.
    - Use of intermediate RL/WL settings require next higher speed bin timing requirements.
    - RL3 support is optional.
LPDDR3: Operations – MR3

- Asymmetric drive strength settings for data-eye optimization.
  - Asymmetric rise/fall slew rates will cut into data-eye width.
  - Margin can be regained using independent control of output drive and resulting slew rates.
  - May improve aperture width, common mode power noise, DQS jitter.

MR3 I/O Configuration 1 (MA<7:0> = 03h):

<table>
<thead>
<tr>
<th>OP7</th>
<th>OP6</th>
<th>OP5</th>
<th>OP4</th>
<th>OP3</th>
<th>OP2</th>
<th>OP1</th>
<th>OP0</th>
</tr>
</thead>
<tbody>
<tr>
<td>(RFU)</td>
<td>DS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- DS: Write-only, OP<3:0>
  - 0001B: 34.3Ω typical pull-down/pull-up
  - 0010B: 40Ω typical pull-down/pull-up (default)
  - 0011B: 48Ω typical pull-down/pull-up
  - 0100B: reserved for 60Ω typical pull-down/pull-up
  - 0110B: reserved for 80Ω typical pull-down/pull-up
  - 1001B: 34.3Ω typical pull-down, 40Ω typical pull-up
  - 1010B: 40Ω typical pull-down, 48Ω typical pull-up
  - 1011B: 34.3Ω typical pull-down, 48Ω typical pull-up
  - All others: reserved
LPDDR3 Operations: MR4

- MR4 temp sensor output additional output setting

<table>
<thead>
<tr>
<th>MR4 Device Temperature (MA&lt;7:0&gt; = 04H)</th>
<th>OP7</th>
<th>OP6</th>
<th>OP5</th>
<th>OP4</th>
<th>OP3</th>
<th>OP2</th>
<th>OP1</th>
<th>OP0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TUF</td>
<td>(RFU)</td>
<td>SDRAM Refresh Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----</td>
<td>-------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDRAM Refresh Rate</td>
<td>Read-only</td>
<td>OP&lt;2:0&gt;</td>
<td>00H: SDRAM Low temperature operating limit exceeded</td>
<td>001H: 4x tREFL, 4x tREFLb, 4x tREFW</td>
<td>010H: 2x tREFL, 2x tREFLb, 2x tREFW</td>
<td>011H: 1x tREFL, 1x tREFLb, 1x tREFW (&lt;=55°C)</td>
<td>100H: 0.5x tREFL, 0.5x tREFLb, 0.5x tREFW, do not de-rate SDRAM AC timing</td>
<td>101H: 0.25x tREFL, 0.25x tREFLb, 0.25x tREFW, do not de-rate SDRAM AC timing</td>
</tr>
<tr>
<td>Temperature Update Flag</td>
<td>Read-only</td>
<td>OP&lt;7&gt;</td>
<td>00: OP&lt;2:0&gt; value has not changed since last read of MR4.</td>
<td>10: OP&lt;2:0&gt; value has changed since last read of MR4.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
LPDDR3 Operations: WRITE

- Write Preamble changed from low-only to toggle (DDR3-like)
  - With DQ termination DQS_t/DQS_c are pulled high prior to a data input operation, making it difficult to detect a DQS transition.
  - Toggle preamble allows better detection of DQS crossover.

[Diagram showing data input (write) timing]

Figure 41 — Data input (write) timing

Figure 15 — Data input (write) timing
LPDDR3 Operations: READ

- LPDDR3 Data Valid Window (DVW) definition has changed from LPDDR2 definition
  - Alignment with DDR3 definition
  - DVW = tQH - tDQSQ
    - For LPDDR2: \( t_{QSH_{\text{min}}} / t_{QSL_{\text{min}}} - t_{QHS_{\text{max}}} - t_{DQSQ} \)
    - DVW Calculation
      \[
      \begin{align*}
      t_{\text{CKavg}} &= 1250\text{ps} \\
      t_{\text{CH(abs)min}} &= 0.43 \times t_{\text{CKavg}} = 537.5\text{ps} \\
      t_{\text{QSH}_{\text{min}}} &= t_{\text{CH(abs)min}} - 0.05 \times t_{\text{CKavg}} = 475\text{ps} \\
      t_{\text{DQSQ}} &= 135\text{ps} \\
      \text{DVW} &= 340\text{ps} \\
      \text{UI} &= 0.5 \times t_{\text{CKavg}} = 625\text{ps} \\
      \%\text{UI} &= 54.4\%
      \end{align*}
      \]

Duty cycle distortion already accounted for in tQSH/tQSL;
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LPDDR3: AC Timing

• Key spec changes
  – 1600/1333 speed bins
    • tCK = 1.25ns/1.5ns
    • Other tCK require use of next highest speed bins
  – Input setup/hold
    • 150ps/175ps
  – Potential for LPDDR3E?
    • 1866/2133 speed bins
    • Setup/hold timing budget very challenging.
LPDDR3: System Design, Pin Cap

- Pin cap reduction from LPDDR2 to LPDDR3 to allow higher speed operation
  - CCK: 2.0 -> 1.4pF
  - CI: 2.0 -> 1.3pF
  - CIO 2.5 -> 1.8pF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min/Max</th>
<th>Value</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input capacitance, CK_t and CK_c</td>
<td>C_{CK}</td>
<td>Min</td>
<td>0.7</td>
<td>pF</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>1.4</td>
<td>pF</td>
<td>1.2</td>
</tr>
<tr>
<td>Input capacitance delta, CK_t and CK_c</td>
<td>C_{DCK}</td>
<td>Min</td>
<td>0</td>
<td>pF</td>
<td>1.2,3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>0.15</td>
<td>pF</td>
<td>1.2,3</td>
</tr>
<tr>
<td>Input capacitance, all other input-only pins</td>
<td>C_I</td>
<td>Min</td>
<td>0.7</td>
<td>pF</td>
<td>1.2,4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>1.3</td>
<td>pF</td>
<td>1.2,4</td>
</tr>
<tr>
<td>Input capacitance delta, all other input-only pins</td>
<td>C_{DI}</td>
<td>Min</td>
<td>-0.20</td>
<td>pF</td>
<td>1.2,5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>0.20</td>
<td>pF</td>
<td>1.2,5</td>
</tr>
<tr>
<td>Input/output capacitance, DQ, DM, DQS_t, DQS_c</td>
<td>C_{IO}</td>
<td>Min</td>
<td>1.0</td>
<td>pF</td>
<td>1.2,6,7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>1.8</td>
<td>pF</td>
<td>1.2,6,7</td>
</tr>
<tr>
<td>Input/output capacitance delta, DQS_t, DQS_c</td>
<td>C_{DDQS}</td>
<td>Min</td>
<td>0</td>
<td>pF</td>
<td>1.2,7,8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>0.2</td>
<td>pF</td>
<td>1.2,7,8</td>
</tr>
<tr>
<td>Input/output capacitance delta, DQ, DM</td>
<td>C_{DIO}</td>
<td>Min</td>
<td>-0.25</td>
<td>pF</td>
<td>1.2,7,9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>0.25</td>
<td>pF</td>
<td>1.2,7,9</td>
</tr>
<tr>
<td>Input/output capacitance ZQ Pin</td>
<td>C_{ZQ}</td>
<td>Min</td>
<td>0</td>
<td>pF</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Max</td>
<td>2.0</td>
<td>pF</td>
<td>1.2</td>
</tr>
</tbody>
</table>
LPDDR3: System Design Considerations

- Signal integrity is significantly affected by these parameters:
  - CIO (capacitance)
  - Driver slew rate
  - Package design
  - Power delivery (key in PoP implementation)

- Great care must be taken to design a system that has good signal integrity at 1600 MT/s with this PHY.

- It is highly recommended to work with memory vendors to model your system using extracted driver and package parameters.

- Additional features can be employed to improve signal margin:
  - DQ On Die Termination (ODT)
  - Asym drive strength