



*Global Standards for the Microelectronics Industry*

# LPDDR4 Moves Mobile

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*Mobile Forum 2013*

# LPDDR4 Architectural Approach

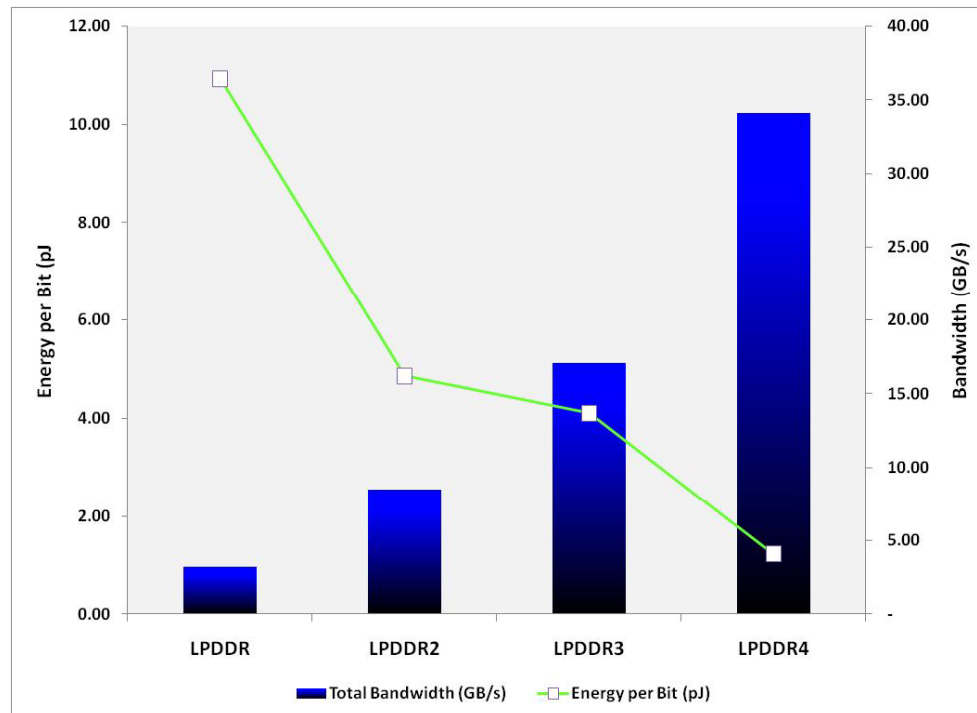
- ▶ LPDDR4 Priorities
  - Power neutrality
  - 2x BW performance
  - Low pin-count
  - Low cost
  - Backward compatibility

# Power Neutrality

- ▶ The Power Neutrality requirement is based on mobile platform constraints
  - Battery capacity is (roughly) static
    - Days (standby) and hours (active) of battery life are required for an acceptable user experience
    - Batter form-factor is (roughly) fixed
  - TDP for the platform is (roughly) static
    - No “oven mitt” platforms allowed!
- ▶ Therefore, power from one generation to the next must be (roughly) static
  - But, advancements in hardware require 2x the BW, generation to generation
- ▶ Achieving power neutrality would be easy if voltage scaling of the transistors could keep pace, but they can't
  - Architectural solutions are required to close the gap

# Mobile DRAM Power Requirements

- ▶ A great user experience requires great power efficiency
  - Tablets – 10 hours active with a 11.5 Ah battery
  - Phones – 8 hours active with a 1.4 Ah battery
- ▶ Active and Stand-by power are critical for mobile platforms



- Phones are targeting 10+ days of standby
- Tablets in “connected standby” targeting 2+ weeks
- Ultrabooks require “always on, always connected” power state, <5% battery drain within 16 hours
- Memory consumes up to 30% of the system power in standby modes

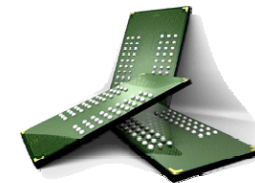
# Mobile System Thermal Envelope

- ▶ Mobile handset platforms are limited to 4-5W total power
  - Heat spreaders are being used to move heat to the case, away from the memory/processor, but the final heat sink is the user
- ▶ Handset performance is “throttled” when thermal limits are reached
  - Reduce video fps
  - Reduce processor core clock speeds
  - Reduce screen backlight
  - All throttling solutions have a negative impact on user experience
- ▶ Heavily utilized memory bandwidth is a significant contributor to thermal response
  - Power consumption > 1W is possible in today’s mobile memory solutions (LPDDR3 & WIO)
- ▶ Mobile DRAM is spec’d for operation up to 105°C with 4x refresh
  - WIO and LP-PoP systems are pushing those limits during “normal” operation, exposing the memory to refresh failures
- ▶ Thermal management is both a system design and DRAM reliability issue

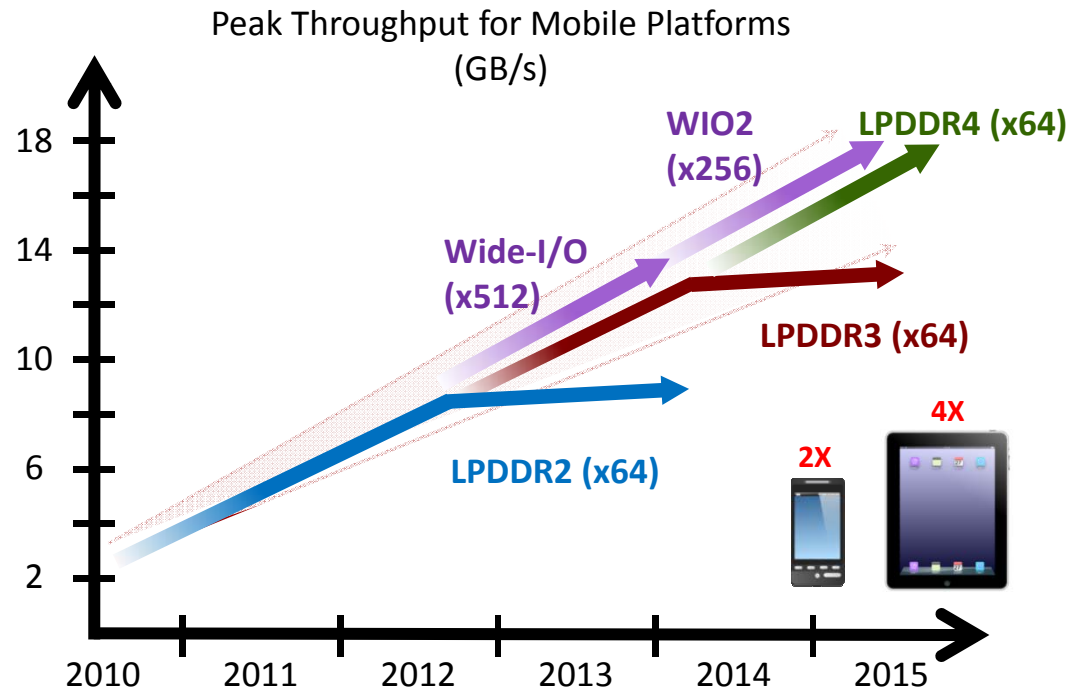
# LPDDR4 Target: Power Neutrality

- ▶ LPDDR4 Key Features for Power Neutrality:
  - Refined architecture lowers the energy/bit:
    - 2ch x16 Architecture for lower  $IDD4R/W$
    - 2KB page for lower  $IDD0$
    - Low-swing rail-terminated driver for lower I/O energy/bit and better signal integrity
    - Low-frequency un-terminated operation supported
    - DBI(dc) for reduced I/O termination power
  - Retain existing low-power features from LPDDRn:
    - Low-latency clock stop/start and frequency change
    - Power-down and self-refresh modes

# Low Power DRAM Bandwidth Roadmap



- ▶ **LPDDR2** (x64) BW target is 8.5 GB/s
  - Data rate up to 1066 Mbps DDR
- ▶ **LPDDR3** (x64) BW target is 17 GB/s
  - Evolutionary successor to LPDDR2
  - Data rate up to 2133 Mbps DDR
- ▶ **Wide I/O** (x512) BW target is 17 GB/s
  - Limited performance scalability (frequency-only)
  - Data rate up to 266 Mbps SDR
- ▶ **LPDDR4** (x64) BW target is 34 GB/s
  - Scalable performance
  - Data rate up to 4.126 Gbps DDR
- ▶ **WIO2** (x256) BW target is 34 GB/s
  - Scalable performance
  - Stacked-die configuration (x512) BW target is 68 GB/s
  - Data rate up to 1066 Mbps



Graphic Source: JEDEC, 2011



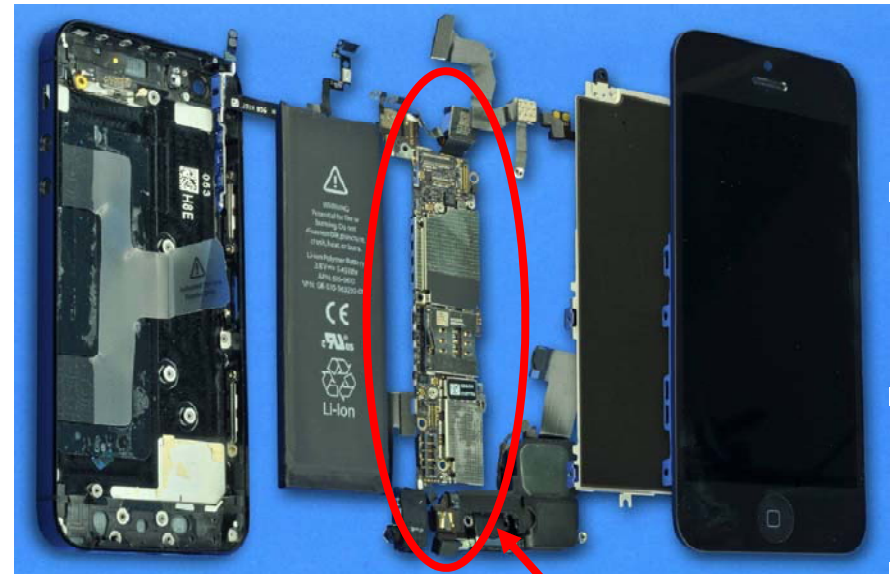
# LPDDR4 Target: BW Performance

- ▶ Key features for BW Performance
  - 2-Channel x 8-bank architecture
    - More responders for higher scheduling efficiency
    - Lower average latency
  - 32B pre-fetch per channel
    - Optimized MAL for fragmented data traffic
  - High speed I/O, up to 4.267 Mbps
    - Targeting support for up to 2DQ or 4CA loads (system dependent)
- ▶ 6.4 GB/s to 8.5 GB/s bandwidth from each channel  
→ Up to 17GB/s per die, 34GB/s for x64 system

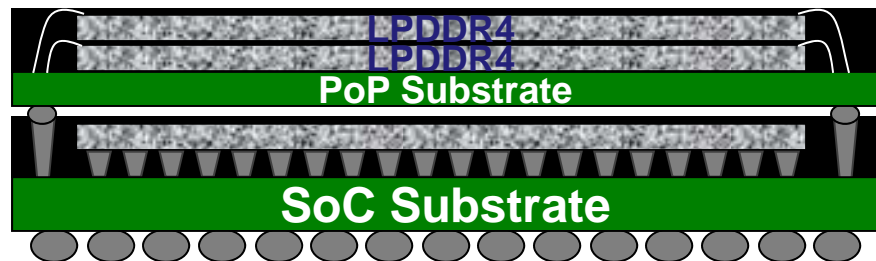


# Mobile DRAM Footprint Requirements

- ▶ The electronics in a handset are assembled on a double sided PWB and sandwiched between the battery and the screen, or sit beside the battery
- ▶ DDP or QDP packages are required to meet the density requirements (1GB – 2GB today, 4GB – 8GB by 2016)
- ▶ <0.8mm total package height for memory is the technology target
- ▶ PoP package used extensively for footprint reduction
- ▶ “Custom” or “Semi-Custom” packages increase inventory risk and limit flexibility
- ▶ BGA and PoP packages provide the most flexible low-cost solution
  - LPDDR4 goal: Retain BGA and PoP package capability



iPhone-5 Electronics  
– 16.4 cm<sup>2</sup>  
Source: Techinsights, 2012



# LPDDR4 Target: Low Pin-Count

- ▶ Key features for Low Pin-Count:
  - Reduce CA bus to 6 pins
    - SDR-CA, 2-beat commands
    - 1066 Mbps max CA rate – same as LPDDR3e
  - Retain LPDDR3 clocking
    - Differential CK
    - Bi-directional differential DQS

# LPDDR4 Target: Low Cost

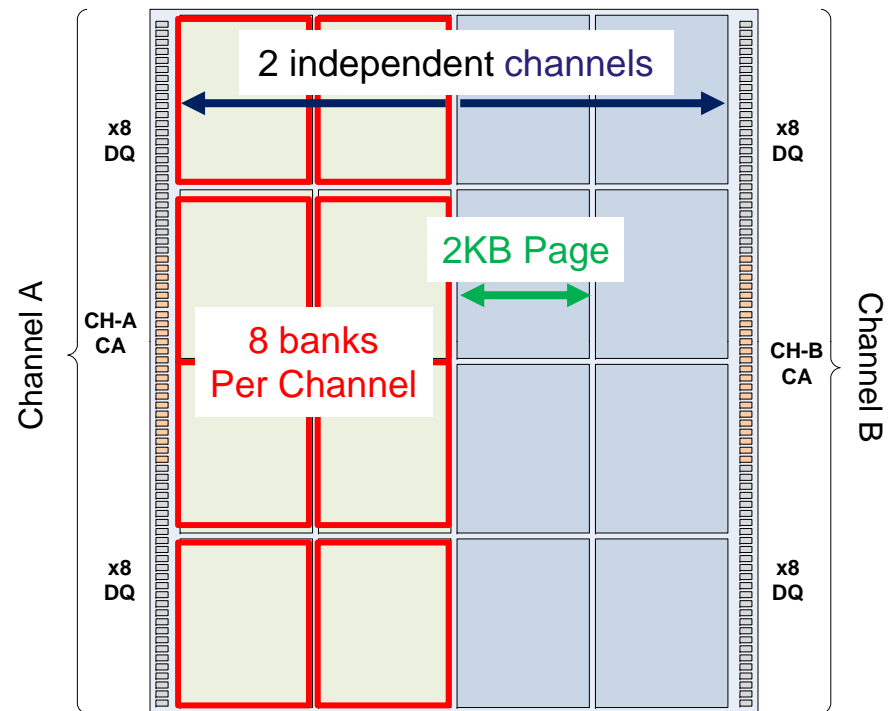
- ▶ Key features for Low Cost:
  - Design re-use of LPDDRn architecture
    - LP-3 and LP-4 both use a 32B pre-fetch architecture
  - Masked Write command provides flexibility for Mfg yield improvement
  - Same back-end manufacturing flow as LPDDR3
    - ATE test and burn-in capability
  - Re-use existing assembly/packaging technology
    - FGBA, PoP, MCP and eMCP packages
  - System-level features for quality and reliability
    - Post-package repair to lower the quality (yield) costs
    - Targeted Row Refresh to lower the reliability (field failure) costs

# LPDDR4 Target: Compatibility

- ▶ Many features and operations will remain compatible with LPDDR3, however...
  - VDD will be changed to lower power consumption
    - 1.1V nominal VDD2/VDDQ
  - CA encoding is new to lower pin-count
    - 6p SDR vs. 10p DDR (LPDDR3)
  - VSSQ-termination is new to enable high-BW with good signal integrity
    - Good data valid window with low-swing I/O
    - Better signal integrity (SSO, ISI, cross-talk)
  - Fully trained Data (WR) bus
    - Enables high data-rates on DQs, better energy/bit for terminated I/O
- ▶ Compromises to compatibility are being carefully weighed against the benefits

# LPDDR4 Architecture

- ▶ 2-Channel x16 architecture
  - Lower power, lower latency
- ▶ 8 Banks per channel (16 per die)
- ▶ 2KB page size
- ▶ 16n (32B) data per column command
- ▶ BW target: 17GB/s per die
- ▶ Clocks centered in local clock-trees
  - DQS centered in byte lanes
  - CK centered in CA lanes



**Conclusion:** LPDDR4 is architected to meet the power, bandwidth, packaging, cost, and compatibility requirements of the world's most advanced mobile systems

**Smartphones ° Tablets ° Ultrabooks**

***THANK YOU***

***JEDEC***

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