UFS v2.0 PHY and Protocol Testing for Compliance

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Agenda

• Introduction to MIPI® Architecture & Linkage to UFS
  – Compliance Testing “Ecosystem”

• UFS Testing Challenges

• Preparing for UFS Compliance Testing
  – Electrical, Interconnect & Protocol
    • Recommended Test Equipment

• Looking Ahead
M-PHY®
Flexible Architecture for High Data Rates/Minimal Power

- M-PHY is a high-speed serial PHY interface to
  - MIPI Alliance
  - JEDEC
  - USB-IF®
  - PCI-SIG®
## Testing in the MIPI Alliance Ecosystem

<table>
<thead>
<tr>
<th>Conformance Testing</th>
<th>Compliance Testing</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MIPI Alliance</strong></td>
<td><strong>UFSA</strong></td>
</tr>
<tr>
<td>- DigRF™</td>
<td>- UFS v2.0</td>
</tr>
<tr>
<td>- CSI</td>
<td><strong>USB-IF</strong></td>
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<tr>
<td>- DSI</td>
<td>- USB3.0</td>
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<tr>
<td>- LLI</td>
<td><strong>PCI-SIG</strong></td>
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<td>- Mobile Express</td>
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</table>
Serial Connections in UFS over M-PHY
UFS Testing Specification

<table>
<thead>
<tr>
<th>UFS</th>
<th>UniPro</th>
<th>MPHY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Version 1.1</td>
<td>1.41.00</td>
<td>2.0 (CTS 1.0)</td>
</tr>
<tr>
<td>Version 2.0</td>
<td>1.6.00</td>
<td>3.0</td>
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</tbody>
</table>

*Note: UniPro & MPHY documents are available only for MIPI Alliance Members for implementation/licensing*
## UFS Testing Challenges

- Higher data rate will increase importance of Signal Integrity of links
  - More emphasis on timing/jitter and noise (signal integrity)
  - Receiver testing will be needed to stress-test BER
- Changeable Gears, Terminations, Amplitudes
  - UFS default is PWM-G1
  - Sublinks can be PWM-G1 through PWM-G7 **OR** HS Gears

### M-PHY Signal Characteristics

<table>
<thead>
<tr>
<th>Signaling mode</th>
<th>Data rates</th>
<th>Amplitudes</th>
<th>Impedance</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Gears</td>
<td>A (Gbps)</td>
<td>B (Gbps)</td>
</tr>
<tr>
<td>High Speed (HS)</td>
<td>G1</td>
<td>1.25</td>
<td>1.45</td>
</tr>
<tr>
<td></td>
<td>G2</td>
<td>2.5</td>
<td>2.91</td>
</tr>
<tr>
<td></td>
<td>G3</td>
<td>5</td>
<td>5.83</td>
</tr>
<tr>
<td>PWM (ie. TYPE-I)</td>
<td>G0</td>
<td>0.01</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>G1</td>
<td>3</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>G2</td>
<td>6</td>
<td>18</td>
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<tr>
<td></td>
<td>G3</td>
<td>12</td>
<td>36</td>
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<tr>
<td></td>
<td>G4</td>
<td>24</td>
<td>72</td>
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<td></td>
<td>G5</td>
<td>48</td>
<td>144</td>
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<tr>
<td></td>
<td>G6</td>
<td>96</td>
<td>288</td>
</tr>
<tr>
<td></td>
<td>G7</td>
<td>192</td>
<td>576</td>
</tr>
<tr>
<td>SYS (ie. TYPE-II)</td>
<td></td>
<td>576 (Mb/s)</td>
<td></td>
</tr>
</tbody>
</table>
UFS Testing Challenges

- Interchangeable PWM and HS Gear Signaling Modes
  - Pulse width modulation for power-efficient low speed communications mode
    - “1” is 30/70 Pulse width
    - “0” is 70/30 Pulse width
  - Use of Ref Clock becomes optional
    - Good for HS gears, but not needed for PWM (self-clocked)
  - Test Challenge
    - Capture of PWM signaling dynamically with HS Gear Signaling
UFS Testing Challenges

Dynamic Signaling & Operation

- Multiple power modes
  - STALL/SLEEP: power saving states; mandatory
  - HIBERN8: enables ultra low power consumption
  - DISABLED: a Powered state where module operation is disabled by RESET
  - UNPOWERED: Power supply is withdrawn
- Dynamic nature makes protocol “capture” difficult
  - MPHYS PWM & HS Gears challenging for FPGA-based signal decoding
  - Dependent on oscilloscopes for protocol decoding
Preparing for UFS Compliance Testing

- Recommended Test Equipment
- PHY test approaches for Compliance & Debug
  - Tx/Rx & Interconnect
- Protocol analysis approaches
  - UniPro
Preparing For UFS Electrical Compliance

- Transmitter Testing
  - Oscilloscope for capture & verification of PWM and HS Gear Signaling
    - Dynamic acquisition state
    - Multiple channels (control/decoded protocol, HS gears, PWM gears)

- Signal Access
  - Probing
    - Differential SMA-based

<table>
<thead>
<tr>
<th>High Speed (HS)</th>
<th>Gears</th>
<th>A (Gbps)</th>
<th>B (Gbps)</th>
<th>Oscilloscope Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>G1</td>
<td>1.25</td>
<td>1.45</td>
<td>6 GHz</td>
<td></td>
</tr>
<tr>
<td>G2</td>
<td>2.5</td>
<td>2.91</td>
<td>8 GHz</td>
<td></td>
</tr>
<tr>
<td>G3</td>
<td>5</td>
<td>5.83</td>
<td>20 GHz</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>PWM (ie. TYPE-I)</th>
<th>Gears</th>
<th>Min (Mb/s)</th>
<th>Max (Mb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G0</td>
<td>0.01</td>
<td>3</td>
<td>50 MHz</td>
</tr>
<tr>
<td>G1</td>
<td>3</td>
<td>9</td>
<td>50 MHz</td>
</tr>
<tr>
<td>G2</td>
<td>6</td>
<td>18</td>
<td>100 MHz</td>
</tr>
<tr>
<td>G3</td>
<td>12</td>
<td>36</td>
<td>150 MHz</td>
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<tr>
<td>G4</td>
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<td>G5</td>
<td>48</td>
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<td>500 MHz</td>
</tr>
<tr>
<td>G6</td>
<td>96</td>
<td>288</td>
<td>1 GHz</td>
</tr>
<tr>
<td>G7</td>
<td>192</td>
<td>576</td>
<td>4 GHz</td>
</tr>
</tbody>
</table>

SYS (ie. TYPE-II)

576 (Mb/s) 4 GHz

Global Standards for the Microelectronics Industry
Preparing For UFS Electrical Compliance

M-PHY Triggering

- Capturing HS Gear and PWM Gear Signaling
  - Aids in identification of timing/amplitude errors

- Serial Trigger System Approaches

[Images of HS Gear – 8b/10b Trigger and PWM Gears – NRZ Trigger]
Preparing For UFS Electrical Compliance

M-PHY HS Gear Decode, Trigger & Search

- Aids debugging by verifying consistency of bus performance over time
- Decode function can look Symbols or 10-bit Characters
- Decode HS Gear 1 - 3 Data Rates
- Trigger & Search on
  - Any Control Character
  - Character/ Symbol
  - Pattern
  - Error (Character Error & Disparity Error)
Preparing For UFS Electrical Compliance

M-PHY Tx Test Automation

- Tests today are tied to M-PHY CTS Specification 1.0
  - CTS1.0 just released by MIPI
Preparing for UFS Interconnect Compliance

- Board and PHY impedance tests that address tolerance for PHY insertion loss on M-PHY devices
- Requires time and frequency domain analysis
  - Time domain tests
    - Impedance
    - Delay
  - Frequency domain tests
    - Differential insertion loss

- Sampling Oscilloscope w/S Parameter Capability
UFS Interconnect Testing

**Time-Domain Reflectometry (TDR)**

- Common TDR Measurements:
  - Impedance
  - Delay

![Sampling Scope display of two TDR waveforms](image)
UFS Interconnect Testing

Frequency Domain S-Parameters

- Frequency-domain characterization of reflections and loss on UFS Interconnects

- Common S-parameter Measurements:
  - Differential return loss
  - Differential insertion loss
  - Frequency domain crosstalk
De-embedding interconnect loss

- SDLA Visualizer de-embeds reflections from UFS interconnect
Preparing for UFS Electrical Compliance

- M-PHY Receiver Testing (needed for HS Gears)
  - Stimulus
    - Arbitrary Waveform Generator
  - Bit Error Detector
    - Oscilloscope
M-PHY Rx Testing
Generating Test Impairments using Arbitrary Waveform Generator

- Support needed for flexible signal impairments for characterization.
- Support needed for Jitter insertion and Pulse Width Modulation as per the M-PHY CTS v1.0.
- Support for DUT in both loopback and non-loopback mode.
M-PHY Rx Test Automation

Oscilloscope-based M-PHY BER with AWG as Pattern Source

- HS Gear 8b/10b Error Detect & Pattern Generation:
  - Hardware Serial trigger: 1.25 Gb/s - 6.25 Gb/s
  - BER for PRBS @ 312Mbs+ data rates.
- Testing Guidance in published Tek Methods of Implementation
Preparing For UFS Protocol Testing

• Protocol Analysis of UFS
  – Oscilloscope for capture & decoding of UniPro and UFS protocol
    • Consistent with MPHY Bandwidth recommendations
      – Ensure link traffic edge captures
    – UniPro defines a universal chip-to-chip data transport protocol, providing a common tunnel for higher-level protocols
UFS Protocol Testing

Seamless PHY & Protocol Views

- Protocol Decode placed right below oscilloscope waveforms
- Packet level info collapses to view packet content
- Link the UniPro/UFS packet to oscilloscope waveform
UFS Protocol Testing

Speed up verification & compliance checks

- Enable faster system level protocol debugging
  - Trigger – target specific events/messages
  - Protocol and physical layer data correlation
- Speed up verification for UFS Compliance
  - Automated CRC computation to monitor CRC errors in protocol packet
- Conforms to UniPro Protocol Specification version 1.41.00
Looking Ahead

• UFS Compliance Testing
  – An open test house / certification process
  – A multi-vendor CTS specification
  – Vendor-based “Methods of Implementation”

• MIPI Alliance
  – UFS2.0 support is well-defined with UniPro v.1.6 & MPHY 3.0 but future requirements for UFS3.0 have just begun
    • UniPro WG seeking more formal requirements discussions for future of UFS3.0
Tektronix M-PHY & Memory Testing Resources

www.tek.com/technology/ddr
www.tek.com/technology/mipi

- Videos/Webinars
- Application Notes
- Product Manuals
- Product Data Sheets
- Recommended Test Equipment
- M-PHY CTS Test Spec