Present and Future Packaging Solutions for the Mobile & IoT Industry

JEDEC Mobile & IOT Forum
Major Growth Drivers in Electronics Industry

For the next phase of growth, the key driver will be the Internet of Things
What is IoT / IoE

- IoT will connect everything with everyone to form a global integrated network
- IoT is driven by integration of multiple technologies in combination with lower costs
- IoT will enhance “things”, “objects” or “machines” with embedded computing and ubiquitous communication technologies
- IoT device typically consists of Sensors/actuators, embedded microcontrollers and connectivity hardware
Hardware IC makers are always squeezed by the market for lower cost Chip-designers -> Wafer Foundries -> OSATs

Who has the lowest margin?
Basic Building Blocks for IoT

Key technologies:
• Sensing
• Processing
• Connectivity

Supported by:
• Sensor/machine infrastructure
• Communication backbone
• M2M service layer
• Application platform
All devices—limited only by our imagination—will form a “close loop control” via sensors, and MCUs with the world through a wireless network.
The Next Golden Age for Semiconductor

- Cisco predicts – the IoT market will be $19 trillion in the coming years
- IDC predicts - IoT market from $1.9 trillion in 2013 to $7.1 trillion in 2020
- World Economic Forum (WEF) - Industrial IoT will have a big impact on world economy that could be nearly two-thirds of the global gross domestic product (GDP) in the next 10 years
- Semiconductor era - a tremendous focus on cost, connectivity, and ultra-low power consumption
- More than just the “things” - also in the networks and data centers which are piece of the IoT stack
- Greater use of MEMS sensors and actuators, RF power devices and MCU chips

![Total MEMS Shipments by Type](source: Semico)

![MCU market in IoT applications compared to markets outside of IoT](source: IHS)

Global Standards for the Microelectronics Industry
Challenges

- Heavy investment to develop high performance IC for IoT systems
- Ultra low power consumption and management is needed
- Connectivity load and data security
- Small form factor to be embedded in today’s and future products
- Increased integration – 16/14nm processes and 10nm processes to satisfy demand

Moore's Law starts slowing the pace of advancement
IC makers have crossed into the packaging industry to continue to meet demand

$ COST
Packages Choices

Integrated-circuit packaging has evolved since the 1970s

1970s
- DIP: Dual in-line package
- SOP: Small outline package
- PGA: Pin-grid array
- EGA: Ball-grid array

1980s
- QFP: Quad flat package
- LCC: Leadless chip carrier
- QFN: Quad flat, no-leads package
- SIP: System in package

1990s
- CSP: Chip-scale package
- POP: Package on package
- 2.5 D: 2.5-D integrated circuits

2000s
- WLP: Wafer-level package
- 3 D: 3-D integrated circuits

2010s
- 2.5 D: 2.5-D integrated circuits

Advanced packaging growth driven by mobile products

Source: IC Insights; Yole Développement; McKinsey analysis

2014
- Total ICs = 223.7 billion units
- Wire Bond is Majority

2019
- Total ICs = 308.2 billion units
- Wire Bond is Majority

Includes only integrated circuits as defined by IC Insights. Excluded are devices such as image sensors, MOSFETs, IPDs, and filters.
Source: TechSearch International, Inc. and IC Insights

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# NFME Quad Packages Choices

<table>
<thead>
<tr>
<th>Sawn QFN</th>
<th>Punch QFN</th>
<th>QFP/LQFP</th>
<th>BGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>QFN 10×10</td>
<td>PDFN 5×6</td>
<td>LQFP 28×28</td>
<td>SLP</td>
</tr>
<tr>
<td>QFN 9×9</td>
<td>PDFN 1.8×5.5</td>
<td>LQFP 24×24</td>
<td>BGA306 11.6×12.1</td>
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<tr>
<td>QFN 7×7</td>
<td>PDFN 3×3</td>
<td>LQFP 20×20</td>
<td>eMMC</td>
</tr>
<tr>
<td>QFN 6×6</td>
<td>PDFN 3×2</td>
<td>LQFP 16×16</td>
<td>BGA169 14×18</td>
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<tr>
<td>QFN 5×5</td>
<td>PDFN 3.3×3.3</td>
<td>PQFP 14×20</td>
<td>BGA443 10.6×11</td>
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<tr>
<td>QFN 3×3</td>
<td>PDFN 8×8</td>
<td>LQFP 14×14</td>
<td>BGA325 19×19</td>
</tr>
<tr>
<td>DFN 1.6×1.2</td>
<td>MOS Modules</td>
<td>LQFP 12×12</td>
<td>BGA241 17×17</td>
</tr>
<tr>
<td>QFN 1.5×1.5</td>
<td></td>
<td>LQFP 10×10</td>
<td>BGA180 12×12</td>
</tr>
<tr>
<td>DFN 1×1</td>
<td></td>
<td>LQFP 7×7</td>
<td>BGA100 7×7</td>
</tr>
</tbody>
</table>

- Pin counts: 4~120 ld
- Pin counts: 6~12 ld
- Pin counts: 32~256 ld
- Pin counts: 10~448 ld
- Body size: 2.05×2~23×2

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NFME FC and WLC Packages Choices

**FLIP CHIP**

- CSP309 7.6*7.6mm
- CSP208 6.2*6.2mm
- CSP64
- CSP48
- CSP16
- CSP9
- CSP6
- CSP4 0.8*0.8mm

**WLCSP**

- CSP309 7.6*7.6mm
- CSP208 6.2*6.2mm
- CSP64
- CSP48
- CSP16
- CSP9
- CSP6
- CSP4 0.8*0.8mm

**Cu Pillar**

- Cu Pillar 10*10mm
- Cu Pillar 7.5*7.6mm
- Cu Pillar 6.4*6.4mm
- Cu Pillar 5.4*5.4mm
- Cu Pillar 3.4*3.4mm
- Cu Pillar 1.5*1.6mm
- Cu Pillar 1.3*1.5mm
- Cu Pillar 1*1.5mm

**Casio WLP**

- Casio WLP 112 6*6mm
- Casio WLP 100
- Casio WLP 36
- Casio WLP 20
- Casio WLP 16
- Casio WLP 12 1.8*1.4mm

**Solder Bump**

- Solder Bump CSP39 3.23*3.23mm
- Solder Bump CSP6
- Solder Bump CSP5 0.8*1.1mm

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Drivers for Flip Chip and WLP

Flip Chip used for
- Microprocessors (all CPUs, GPUs, APUs and Chipsets)
- ASICs, FPGAs and DSPs
- Digital TV and other media products
- Wireless products
- High performance DRAMs and graphics memories

FC is the thinner package

Major applications for WLP
- Smartphones (the highest volume)
- Digital cameras and camcorders
- Laptops and tablets
- Medical devices
- Automotive
- Wearable devices (watch, glasses ……)

WLP meets system packaging needs
- Small form factor / Need for low profile packages
- Lower cost (less materials)

Form Factor is key
- Low profile
- Limited space on PCB
Copper Pillar – Bumping Trends

Demand on 12” Wafers

![Graph showing demand on 12” wafers from 2014 to 2019 with a CAGR of 29%/yr.]

- Industry is transitioning to Cu Pillar
- Mobile IC makers (Spreadtrum, MTK…) are pioneers to use Cu pillar for mobile devices
- Intel’s CPUs/GPUs, chipset, FPGAs etc. migrated to use Cu pillar
- Most ASICs and FPGAs migrating to Cu pillar at < 100um pitch
NFME 12” Fully Auto Bumping Line

First Chinese OSAT to provide 12” 28nm Cu pillar full turnkey services
## NFME Cu Pillar Process Capability

![Diagram showing dimensions of NFME Cu Pillar Process Capability](image)

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
<th>Current limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>Bump Pitch</td>
<td>( \geq 80\text{um} )</td>
</tr>
<tr>
<td>S</td>
<td>Bump Space</td>
<td>( \geq 30\text{um} )</td>
</tr>
<tr>
<td>D</td>
<td>UBM Diameter</td>
<td>( \geq 40\text{um} )</td>
</tr>
<tr>
<td>BH</td>
<td>Bump Height</td>
<td>( \text{BH} \leq 70\text{um} )</td>
</tr>
<tr>
<td></td>
<td>Aspect Ratio</td>
<td>( \text{BH} / S \leq 2 )</td>
</tr>
<tr>
<td>h</td>
<td>Solder Cap Height</td>
<td>( h \leq 70% \text{D} )</td>
</tr>
</tbody>
</table>
NFME Wafer Level CSP Structure

Ball size : 150~300um
Pitch : >250 um
Max size (engr mode) : 7.6 x 7.6mm
Max size (production) : 3.4 x 3.4mm
RDL thickness : 3.0 ~10 um
Fan-Out WLCSP

- Embedding known good die (KGD) into mold compound or substrate
- Building up interconnect layers from die to BGA balls on mold compound or substrate
- Major processes: Reconstitution, Redistribution, Ball Attach and Package Singulation

Advantages:
- Eliminates die interconnect (bump and wire bonds) and substrate
  - Excellent Electrical Performance with Shorter interconnects
  - Eliminate interconnect stress and ELK (extreme low dielectric constant) crack delamination issues
- Fine Line/Space (L/S) for better routability and miniaturization
- Finer pad pitch on die than flip chip
- Thin package, Smaller Form Factor
- Potential SiP, Multi-die, 3D Solution
  - High integration – chips + passives
Drivers for Fan-Out WLCSP

- Advanced WLP will further drive miniaturization of next generation electronic products
- The use of Redistribution Layers (RDL) is an integral part of WLP, in which processes are being performed at the wafer level instead of the traditional wire bonding process
  - Smaller form factor, lower profile package (less than 0.35mm)
  - Increased I/O density
  - Multi-die package/SiP
  - Excellent electrical and thermal performance
  - High reliability is given
  - Package cost only spent on Known Good Die
  - No pad limitation
  - SiP compatible (2D & 3D)

Potential for >5.6 billion units shipments in 2020 by TechSearch
Advanced Packaging Technology for MEMS

Multiple layer RDL on top of TSV

UBM Processing

Cu-pillars

Fan-out Wafer Level Packaging with TSV
System in Package (SiP)

- A complete system packaged in one housing
- Several IC chips are connected on a single substrate or interposer
- A multichip module (MCM) that contains all the parts of a complete system

Markets for System in Package

- RF and wireless devices
  - Power amplifiers, front end module, antenna switch, GPS/GNSS modules, cellular handset and cellular infrastructure, Bluetooth® solutions
- Solid-state drives (SSDs)
  - Storage for tablets, net books and computing applications where typical SSDs include controller ASIC, NAND, DDR, logic and power circuits
- Automotive applications
  - Under-hood electronic control unit (ECU), sensory modules and infotainment
- IoT for wearable and machine to machine (M2M) products
  - Connectivity, MEMS, sensors, microcontroller, power management and other mixed-signal devices
- Power modules
  - IPM, DC/DC converter, LDO, battery management and others
Power Module Packages Introduction

*Intelligent Power Module* typically includes 6 IGBTs, 6 Diodes and 3 Driver ICs.

- **1.8mm IC**
- **3.1mm**

Customized DIP modules  QFN + MCM = µpower module

Power SiP

- **600V IPM (1-5A)**
- **600V IPM (6-15A)**
- **600V IPM (15-30A)**
- **600V IPM (20-40A)**
- **1200V IPM (30-50A)**

Standard Power Module  IGBT Module  Open Tool IPM

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2.5D and 3.0D Technologies Growing

- Need to integrate more die content per package
- Driven by processor makers toward memory integration
- Driven by mobile makers to use advanced lithography and leading-edge silicon with bringing memory into package
- Challenge: A lot of different things all in the same package at the right cost

Source: McKinsey
Will 2016 be the year for 2.5D/3D?

- 3D stacking always make sense to shrink features and dimensions
- How to remove the heat from a stacked die package with logic-on-logic on multiple layers
- Industry concerns about who’s responsible if a known good die doesn’t function in a 3D stack
- 3D packaging has been used for high-performance DRAM for shorter interconnects with TSV

**AMD High-Bandwidth Memory (HBM)**

- GDDR5 can’t keep up with GPU performance growth by power consumption
- GDDR5 limits form factors
- On-chip integration not ideal for everything
Consolidation Impacts on OSAT Business

- Industry is always developing new and advanced package types – WLP, 2.5D/3D
- Advanced packaging requires a significant high investment on R&D and CapEx
- OSAT-IDM strategic engagement (JV/M&A) can leverage their advantages to yield very positive and key inflections points for growth, market share gains
- The JV of NFME-AMD creates a strong engineering and operation talents to develop advanced packages, such as FC-CSP, WLCSP, 2.5D and 3D
- NFME will be positioned in a key market segment to drive next generation platforms crossing several key end markets:
  - High performance (Server, Graphics, Computing …)
  - Mobile (Miniaturization, SiP …)
  - IoT (Integrating MCU/Sensors/Memory …)
NFME-AMD JV – Market Share Expansion

Bar chart showing market share expansion for various companies, with ASE leading at 4,769, followed by SPIL at 3,700, PowerTech at 2,520, and TFME at 730. The top 6 companies are highlighted in a red box.
NFME-AMD JV – Package Expansion
Nantong Fujitsu Microelectronics (NFME)

1st OSAT in China to provide:
- Automotive packaging
- LQFP packaging
- BGA packaging
- MCM packaging
- 28nm Cu Pillar full turnkey

NFME + AMD

Technology expansion:
- Increase FC I/O up to 3000
- ≥ 14/16nm ELK qualified
- Coreless substrate
- Substrate up to 18 layers
- Increase package size (75mm)
- Increase density, speed & bandwidth
- Adv. SoC hardware development
Same Package Choice from Suppliers

Success of McDonald’s Business

- **Consistency**
  To have a similar experience wherever you are (geographic region)
  - Look the same; - Taste the same; - Service the same

- **Innovation**
  Innovation stemming from responsiveness to customers

Packages assembled need to be

- **Consistency**
  To have a same look, same quality, same reliability, same service and same value produced in wherever companies and country locations

- **Innovation**
  To provide the advanced technologies to satisfy market and customers

JEDEC is the solution

- **Consistency**
  For over 50 years, JEDEC has been the global leader in developing open standards and publications for the microelectronics industry

- **Innovation**
  JEDEC committees provide industry leadership in developing standards for a broad range of technologies. e.g. released first DDR spec in June 2000
Conclusions

IoT experiencing tremendous growth – Sensing, Processing and Connectivity
- Billions of devices in few more years to increase the connectivity
- Many short-range to long-range wireless transmissions to transport IoT data
- The margin of ICs will continually be squeezed for lower cost
- Mobile products require low profile packages: FC-CSP, Fan-in WLP, FO-WLP

Demand for lower cost solutions drives adoption of new package designs
- Many different products, many different package types

Moore’s Law slows the pace of advanced silicon technology
- Need more packaging, co-package-co-design, closer Silicon to package integration for electrical, thermal and performance
- Miniaturization drivers Fan-Out WLP, SiP, 2.5D, 3D advanced packages
- 2016 will be the year of 2.5D

Consolidation
- Value of OSATs working closely with IDMs who knows the advanced design and systems
- With partner with AMD, NFME can be able to build an ecosystem from supply-chain to manufacturing to design and produce the advanced future packages

OSATs should produce the packages: same look, same spec, same reliability
- Industry 4.0/IoT should be applied by OSATs operations
- OSATs should joint and partner with JEDEC to set up more industry rules
Thank You!