

JEDEC DESIGN STANDARD

**DESIGN REQUIREMENTS FOR OUTLINES OF SOLID
STATE AND RELATED PRODUCTS**

JEDEC PUBLICATION 95

SECTION 4

DESIGN GUIDES



**JEDEC
SOLID STATE TECHNOLOGY ASSOCIATION**

SECTION 4: DESIGN REQUIREMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS

Contents

		<u>Page</u>
4	Design Guides, Introduction	4.1-1
4.1	Unused	
4.2	General Requirements	4.2-1B
4.3	Unused	
4.4	English Bumpered Gullwing Quad Flat Package (PQFP)	4.4-1
4.5	Fine Pitch (Square) Ball Grid Array Package (FBGA)	4.5-1G
4.6	Fine Pitch (Rectangular) Ball Grid Array Package (FRBGA)	4.6-1D
4.7	Die-Size Ball Grid Array Package (DSBGA)	4.7-1E.01
4.8	Plastic Quad and Dual Inline Square and Rectangular No Lead Packages (With Optional Thermal Enhancements) (QFN/SON)	4.8-1C
4.9	Generic Matrix Tray for Handling and Shipping (Low Stacking Profile for BGA Packages)	4.9.1A
4.10	Generic Matrix Tray for Handling and Shipping	4.10.1D
4.11	Dual In Line Plastic Family	4.11-1A
4.12	To Be Determined	4.12-1
4.13	Metric Small Outline J-Leaded Package (SOJ)	4.13-1A
4.14	Ball Grid Array Package (BGA)	4.14-1G.01
4.15	Metric Thin Small Outline Package Type II (TSOPII)	4.15-1B
4.16	Ultra-Thin Plastic No Lead Small Outline Package (UR-PDSO-N)	4.16-1A
4.17	Ball Grid Array (BGA) Package Measurement and Methodology	4.17-1C
4.18	Wafer Level Ball Grid Arrays (WLBGA)	4.18-1A
4.19	Quad No-Lead Staggered and Inline Multi-Row Packages (With Optional Thermal Enhancements) (QFN)	4.19-1D
4.20	Small Scale Plastic Quad and Dual Inline Square and Rectangular No-Lead Packages (With Optional Thermal Enhancements) (QFN/SON)	4.20-1E

**SECTION 4: DESIGN REQUIREMENTS FOR OUTLINES OF SOLID STATE AND
RELATED PRODUCTS**

Contents (cont'd)

		<u>Page</u>
4.21	Internal Stacking Module, Land Grid Array Packages with External Interconnect Terminals (ISM)	4.21-1A
4.22	Fine Pitch Square Ball Grid Array Package (FBGA) Package on Package (PoP)	4.22-1C.02
4.23	Punch-Singulated Fine Pitch Square Very Thin and Very-Very Thin Profile Leadframe-Based Quad No-Lead Staggered Dual-Row Packages (With Optional Thermal Enhancements) (QFN)	4.23-1A

SECTION 4: DESIGN REQUIREMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS (formerly JESD 95-1)

(From JEDEC Board Ballot JCB-89-38, formulated under the cognizance of JC-11 Committee on Mechanical Standardization)

Introduction

JEDEC REGISTERED AND STANDARD OUTLINES FOR SEMICONDUCTOR DEVICES, JEDEC PUBLICATION 95, is the official JEDEC Publication that contains the registered or standard mechanical outlines of solid state products and related items. The introduction of this document states:

"The primary purpose of solid state products outline registration is to assure complete mechanical interchangeability of all products conforming to a particular outline regardless of when or from whom it was obtained."

The reality of the situation is that the Publication 95 outlines have become "umbrellas" or "catch-alls" in order to accommodate the various nominal dimensions of different manufacturers. The effect has been to increase tolerances to the point that they reflect large size variations rather than small variations around a common nominal or mean dimension. Another factor has been the attempt on the part of the manufacturers to use the largest possible tolerances in order to allow production to proceed at high speed and high volume.

From a component production point of view, the use of wide tolerances is an economically desirable goal. From a system point of view, such use results in the transfer of costs to the user who has to accommodate the large tolerances. The user is also limited in the selection of vendors because of a lack of complete interchangeability of the products of different manufacturers.

Recognizing these problems, the JEDEC Board of Directors authorized the formation of the Design Handbook (DHB) Committee to operate under the cognizance of the JC-11 Committee on Mechanical Standardization. The Committee was charged to establish criteria that will:

- Reduce the PROLIFERATION of outlines
- Provide FUNCTIONAL semiconductor package and related part outlines that will be the basis for PROCUREMENT documents specifying nominal dimensions, realistic tolerances and quality requirements for all outlines.

JEDEC Standard 95-1, once referred to as the Design Handbook, established guideline methods for obtaining the desired dimensions and tolerancing for various classes of packages and related items. In September 2000, JEDEC Standard 95-1 was combined with JEP95 as section 4. This section will be updated on a regular basis as new packages are developed.

During its Fall 1987 meeting the JC-11 Chairman authorized the formation of a Task Group, which subsequently became the JC-11.2 Design Requirements Committee, with the goal of producing this section.