

2 TERMS AND DEFINITIONS

This section contains listings and definitions of a number of terms that are needed for a clear understanding of the standards as presented. Most of these terms have been developed within the semiconductor memory industry and are not covered by JEDEC Standard 100. They are, however, not in conflict with this standard which contains all JEDEC approved definitions.

The following pin names and functional descriptions apply uniformly to all devices covered by this standard. Where a pin has a dual-function, and those functions are invoked at substantially different times, the names and symbols for the functions are separated by a slash (/) (e.g., VPP/G\). Where a pin has multiple functions which are used interspersed at essentially the same time, the slash is omitted (e.g., DQ). Where multiple pins have a similar function, a number symbolized as (n) is appended to the symbol. Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the overbar or trailing reverse slash (\) is appended to the symbol. Where alternative functions are allowed by the standard, the allowed functions are listed separated by commas. Where common usage has resulted in two terms being used interchangeably, both are listed but the order of listing indicates the order of preferred usage. For example, $\overline{\text{CAS}}$ is preferred to $\overline{\text{CE}}$.

Following the list of PIN definitions, there are a series of other terms and definitions that are required for a clear understanding of the individual device standards.

In addition to the standard terms that are commonly used in a broad range of devices, there are names that are specialized and used only with a single class of device. These terms are included in separate sections of the standard as their usage becomes commonplace. In the current release, names for MPDRAM, Memory Cards, and SRAM are included.

The terms in this section are organized by technology and usage and presented in 11 different sub-sections as follows:

- 2.1 CONVENTIONAL DEVICE PIN NAMES
- 2.2 MULTIPOINT DRAM PIN NAMES
- 2.3 POWER PIN NAMES
- 2.4 DEVICE TYPE NAMES
- 2.5 MISCELLANEOUS DEVICE RELATED TERMS
- 2.6 SPECIAL OPERATIONAL CYCLES FOR MPDRAM
- 2.7 Package-Related Terms
- 2.8 Memory Card Pin Names
- 2.9 SRAM & SSRAM SPECIAL PIN NAMES
- 2.10 SLDRAM SPECIAL PIN NAMES
- 2.11 MCP Signal Names

2.1 CONVENTIONAL DEVICE PIN NAMES

The following signal names are those that are used over a broad range of devices described in this standard. Specialized pin names that are used for a specific class of device are given in separate sections of Chapter 2 of this standard. All pin names may be either positive or negative logic as defined in the individual device standards. Logic polarity is not given here unless it is inherent in the definition.

2.1.1 - A, PORT A

In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.2 - A(n), ADDRESS INPUTS

Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another. When the address numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.3 - ADQ(n), ADDRESS DATA INPUT/OUTPUT

The pins that are multiplexed three ways to serve as address input, data input, and data output pins. When the address data input/output numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.4 - AL, ADDRESS LATCH ENABLE

An input that when true, allows the input address to be entered into a register, and when false, causes the address state previously entered to be latched.

2.1.5 - B, PORT B

In dual port memory devices, the two ports are designated port A & port B. The letter A or B is appended as a suffix to any pin that is specific to one or the other of the ports.

2.1.6 - BA, BANK ADDRESS

In a RAM that has multiple banks in its architecture, the BANK ADDRESS is used, to select any one of the available banks.

2.1.7 - BG, BYTE MODE ENABLE

An input that when true, causes a word wide device to operate in the byte mode and to present the high or low byte on a pre-defined data pin set. Truth tables will be provided to define the details of the operation.

2.1.8 - BS, BLOCK SELECT

A group of input signals that enable individual bit blocks of the data interface.

2.1.9 - BY, BUSY

The output that, on some devices, signifies that some internal asynchronous operation is still in process, and that the device is not available for normal functions. This signal is normally implemented so that multiple devices can be OR-tied.

2.1.10 - C, OUTPUT CLOCK

The input, on some devices that contain an output data register, that causes the data to be set into the register.

2.1.11 - CA, COLUMN ADDRESS

In an address multiplexed DRAM, the address field that is captured by the COLUMN ENABLE clock CAS\ . When the column address numbering is significant for device operation, the addresses are numbered, beginning with 0.

2.1.12 - CAS, (CE), COLUMN ENABLE

An enable signal that on some dynamic RAMs actuates only the column oriented internal circuits and the data input/output circuits. Most devices normally require the RAS\ signal to be present for the CAS\ signal to be effective. In some newer designs, however, special sequences of the RAS\ and CAS\ signals are used to actuate certain special device control functions. In devices that have a CAS\ per output, the CAS\s are numbered beginning with 0. In devices that have a CAS\ per byte, the CAS\s are designated LCAS\ & UCAS\ for 2 byte devices. LCAS\ affects DQ0⇒DQ7, and UCAS\ affects DQ8⇒DQ15. For devices with a CAS\ per byte, and have more than 2 bytes, the CAS\s are numbered beginning with 0. In modules that have a CAS\ per byte, the CAS\s are numbered beginning with 0. CAS0\ affects DQ0⇒DQ7, CAS1\ affects DQ8⇒DQ15, CAS2 affects DQ16⇒DQ23, and CAS4\ affects DQ24⇒DQ31.

2.1.13 - CK, INPUT AND OUTPUT CLOCK

An input that controls the activation of both input and output circuitry, normally storage registers or latches.

2.1.14 - CKE, CLOCK ENABLE

In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.

2.1.15 - CL, Clear

An input that, when true, causes all cells in the memory array to be cleared to their zero state.

2.1.16 - D(n)(x), DATA INPUT

Those inputs whose state represents the value of data that is to be written into the selected address on a write cycle of an alterable memory device. When the numbering of the data inputs is significant for device operation, the data inputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc.

2.1.17 - DC, DIAGNOSTIC CLOCK

The input that, on some devices, invokes and controls any built-in diagnostic test features.

2.1.18 - DQ(n)(x), DATA INPUT/OUTPUT

The pins that serve as data output(s) when in the read mode and as data input(s) when in the write mode. When the device is not selected or enabled, the output(s) are in a floating state. On a devices having both serial and parallel access ports, these pins provide access to the parallel RAM port data channels. The suffix (n) is a numeric value indicating the number assignment of a particular pin with numbering starting at 0. In some situations the letters U or L are used to indicate that the pins are assigned to the upper or lower byte of a 2 byte data interface. In devices where the standard supports an optional 9th bit that may be used as a parity bit, the suffix P may be used in lieu of a numeric value. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc.

2.1.19 - DQM, INPUT/OUTPUT DATA MASK

A control signal used primarily on SDRAMs that acts as a mask for reading and writing functions. In some instances, the DQM term will include a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, a "x" is applied where "x" takes the values of a, b, c, etc.

2.1.20 - E, CHIP ENABLE

The input that, when true, permits active operation including the input and/or output of data, and when false, prevents active operation and causes the memory to be in a reduced power standby mode with the outputs floating.

2.1.21 - F, REFRESH

An input that, when true, causes the device to enter a data refresh mode.

2.1.22 - G(n), OE(n), OUTPUT ENABLE

The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.23 - GS, SYNCHRONOUS OUTPUT ENABLE

An output enable input that must be set in by a synchronizing clock signal, K (q.v.).

2.1.24 - I, INITIALIZE INPUT

A control input that provides a preassigned Manufacturer or User defined code to be set into the data register. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.25 - ID(n), IDENTIFICATION

A group of output terminals, nominally used to convey information about the configuration or other attributes of the device when plugged into a system. The function of these outputs are similar to those of the PD(n) terminals but they often have different electrical interface characteristics.

2.1.26 - I/O, INPUT/OUTPUT

A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicator of the nature of the function of the pin.

2.1.27 - IS, INITIALIZE INPUT (SYNCHRONOUS)

A control input that provides a preassigned Manufacturer or User defined code to be presented to the data register for subsequent setting by a clock input. If the input is all "0", it can be called "clear", and if all "1", then "preset".

2.1.28 - K, INPUT CLOCK

The input that, on devices that contain input buffer registers, causes the address on the A(n), the data on the D(n) pins and/or certain control inputs to be set into the register.

2.1.29 - L, LATCH ENABLE or LOWER BYTE

An input that, on devices containing a latch register, causes the data to be latched into the register. When L is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. LW).

2.1.30 - LB, LOWER BYTE ENABLE

An input, on worldwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.

2.1.31 - LW, LOWER BYTE WRITE ENABLE

An input, on worldwide devices, that when true causes the data present on the lower byte input/output, terminals DQ0 through DQ7, to be written into the addressed cells of the device.

2.1.32 - M(n), M, MODE SELECT, MASK

Input signals that when true select an alternative mode of operation for the device. The alternative modes available must be defined in the applicable device standard. When M is used in conjunction with other symbols to create a new pin name, it signifies that the pin function is either MASK or MODE related.

2.1.33 - MA, MATCH

An output signal that when true indicates that there has been a match (logic compare equal) between data stored in the memory and data presented on a set of input pins as defined in the individual device standard.

2.1.34 - MCH, MUST CONNECT HIGH

A pin which must be connected to a voltage that is interpreted as logic high or "true" signal.

2.1.35 - MCL, MUST CONNECT LOW

A pin which must be connected to a voltage that is interpreted as logic low or "false" signal.

2.1.36 - NC, NO CONNECTION

A pin to which no internal electrical connection is present or allowed.

2.1.37 - NE, NON-VOLATILE ENABLE

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The input, on a NVRAM, that enables the non-volatile functions ST & RC as determined by the states of S,E,G, and W.

2.1.38 - NF, NO FUNCTION

An input that is electrically connected to the device but for which the signal has no function in the device operation.

2.1.39 - NP, NO PIN

A pin position on a package where the pin has been purposely been left blank or removed after assembly. No physical pin is allowed in this position.

2.1.40 - NU, NOT USABLE

A device pin to which there may or may not be an internal connection but to which no external connections are allowed.

2.1.41 - OE,(n), G(n) OUTPUT ENABLE

The input that, when false, disables the outputs and causes them to go to an inactive state, but that does not effect the writing function. When disabled, the inactive state is floating (Z), for MOS and TTL devices and low (L), for ECL devices. In modules that have multiple OEs, the OEs are numbered beginning with 0.

2.1.42 - OP, OPTIONAL

The designation for pins on which the manufacturer has the freedom to supply a specialized function not previously defined in the standard, and still have his part meet the requirements of the standard.

2.1.43 - P, PROGRAM or PROGRAM ENABLE, PARITY

The input on a non-volatile memory device that, when true, causes the data present on the D or DQ pins to be written into the addressed cell(s) of the device. The letter P may also be used as a suffix for data pins where an optional 9th bit, that may be used for parity, is allowed by the standard (e.g. DQP)

2.1.44 - PD(n), PRESENCE DETECT

A group of output pins, normally used on modules or cards, whose state is used to convey information about the capacity, speed, configuration, or other attributes of the device when plugged into a system.

2.1.45 - PR, PAGE RESET

The input on a page select memory that, when true, unconditionally causes the page select address register to be reset to zero and the corresponding page to be selected.

2.1.46 - PS, PAGE SELECT

The input on a page select memory that, when true, causes one of the pages of memory to be selected as identified by the inputs on the DQ pins (as defined in the appropriate function table) and for this page address to be stored in an internal register.

2.1.47 - Q(n)(x), DATA OUTPUT

The outputs whose state represents the data read from the selected cells. When the device is not selected or enabled, the outputs are usually in a floating (Z, high impedance) state. When the numbering of the data outputs is significant for device operation, the data outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc.

2.1.48 - QFC, FET CONTROL

An internally generated output signal from a memory device that goes true during every Read and Write access cycle. It can be used to control isolation switches on modules.

2.1.49 - RA, ROW ADDRESS INPUT

In an address multiplexed DRAM, the address field that is captured by the ROW ENABLE signal, RAS_. When the numbering of the row address numbering is significant for device operation, the RA are numbered beginning with 0

2.1.50 - RAS, (RE) ROW ENABLE INPUT

A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry. In modules that have multiple RAS's, the RAS's are numbered beginning with 0.

2.1.51 - RC, RECALL

The input on a NVRAM, that transfers the non-volatile data into the RAM array.

2.1.52 - RFU, RESERVED FOR FUTURE USE

A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined.

2.1.53 - RSVD, RESERVED

In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.

2.1.54 - RY, READY

The output that, on some devices, signifies that no internal asynchronous operations are still in process, and that the device is available for normal functions. This signal is normally implemented so that multiple devices can be OR-tied. This signal is the inverse of BY (RY= $\overline{\text{BY}}$)

2.1.55 - S(n)(x), CHIP SELECT

The input(s) that, when any one is false, causes the device to be disabled without any significant change in the power consumption. When deselected, the outputs go to the inactive state (floating (Z) for MOS and TTL devices and low (L) for ECL devices), and the device becomes insensitive to a write command. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc.

2.1.56 - ST, STORE

The input, on a NVRAM, that initiates the non-volatile data storage of the entire RAM array.

2.1.57 - Sxx, SYNCHRONOUS FUNCTION

On a synchronous memory device, any input terms that are synchronous with a clock should start with the letter S. For example: $\overline{\text{SG}}$ = Synchronous Output Enable, $\overline{\text{SW}}$ = Synchronous Write Enable.

2.1.58 - TF, TEST FUNCTION

The input, on a MEMORY that, when true, causes built in on-chip test logic to be actuated and for the part to go into its test mode of operation.

2.1.59 - U, UPPER BYTE

When U is used in conjunction with a data or control term it signifies that the combined term applies to the lower byte of a two byte data interface device (e.g. UW).

2.1.60 - UB, UPPER BYTE ENABLE

An input that, on worldwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.

2.1.61 - UW, UPPER BYTE WRITE ENABLE

An input, on worldwide devices, that, when true, causes the data present on the upper byte input/output, terminals DQ8 through DQ15, to be written into the addressed cells of the device.

2.1.62 - WE, W, WRITE ENABLE

The input that, when true, causes the data present on the D or the DQ pin(s) to be written into the address cell(s) of the device. In devices that have a WE per byte, the WEs are designated LWE & UWE for 2 byte devices. In devices that have a WE per byte and more than two bytes, the WE are numbered beginning with 0. In modules that have multiple WEs, the WEs are numbered beginning with 0.

2.1.63 - WP, Write Protect

When this signal is applied to a memory module or an EEPROM, it is an input signal that when true, protects the EEPROM memory array from being written into or erased. When false, the write functions inherent in the device are activated. When applied to a memory card, it is an output signal defined in Par. 2.8.5 of this Standard.

2.2 MULTIPORT DRAM PIN NAMES

The following pin names apply primarily to specialized function pins for MPDRAM. In some situations, the names may also be applicable to other types of memories such as Graphics DRAMs.

2.2.1 - DSF, SPECIAL FUNCTION ENABLE INPUT

The input on a device, that when true, actuates certain special operational functions. In devices and modules that have multiple DSFs, the DSFs are numbered beginning with 0.

2.2.2 - DT/OE(n), TRG(n), DATA TRANSFER/OUTPUT ENABLE INPUT

The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.2.3 - QSF, QSY, TRANSFER ACKNOWLEDGE OUTPUT

The output on a device having both serial and parallel access ports which signifies that a transfer of data from the parallel to the serial port, in certain special transfer cycles, has been completed. In devices and modules that have multiple QSFs, the QSFs are numbered beginning with 0.

2.2.4 - SC, SERIAL CLOCK

An input, on devices having a serial data access port, that actuates the serial transfer of data, either in or out.

2.2.5 - SDQ(n)(x), SERIAL DATA INPUT/OUTPUT

The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode and as serial data inputs(s) when in the write mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data input/outputs is significant for device operation, the serial data input/outputs are numbered beginning with 0. In devices where data bit groupings have independent control, an additional suffix "x" is applied. "x" takes the values of a, b, c, etc.

2.2.6 - SE, SERIAL PORT ENABLE

The input that, when true, actuates the device's serial access circuitry.

2.2.7 - SG, SERIAL PORT OUTPUT ENABLE

The input that, when true, actuates the device's serial data output circuitry.

2.2.8 - SQ(n), SERIAL DATA OUTPUT

The pins, on a device having a serial data access port, that serve as serial data output(s) when in the read mode. When the device or the serial port is not selected or enabled, the output(s) are in a floating (Z) state. When the numbering of the serial data outputs is significant for device operation, the serial data outputs are numbered beginning with 0.

2.2.9 - TRG(n), DT/OE(n) DATA TRANSFER/OUTPUT ENABLE INPUT

The input on a device having both serial and parallel access ports that, depending on the state of one or more of the other control lines of the device, either enables an internal data transfer between the serial and parallel port circuitry, or enables the data outputs of the parallel port.

2.3 POWER PIN NAMES

The following symbols are used to designate the power pins in a memory device. When only a single pin is provided for a given supply, the pin name is used without suffix. When multiple pins are used, a suffix may be used to designate specific pins. A numeric suffix is used to indicate the preferred order of implementation when optional redundant pins are allowed. An alphabetic suffix is used to indicate pins which have a specific power circuit or loop connection. The use of a common suffix for different supplies indicates that those pins connect to a common power loop.

2.3.1 - VBB, SUBSTRATE POWER VOLTAGE

A bias voltage that maintains the substrate at a potential which is negative with respect to GND or VSS in an NMOS or CMOS part.

2.3.2 - VCC, LOGIC POWER VOLTAGE

The most positive potential of the two logic power supply pins. This is used for the memory device power voltage when the supply voltage is nominally 5 V. VCC is also commonly used to designate the ground reference power supply voltage for ECL interface devices.

2.3.3 - VCCQ, OUTPUT STAGE LOGIC POWER VOLTAGE

See VDDQ for definition. VCCQ is restricted to 5 V applications only

2.3.4 - VDD, DRAIN POWER VOLTAGE

The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use 5 V.

2.3.5 - VDDID, VDD Identification Flag

In certain modules, this signal is created by the module to identify the relationship between the VDD and VDDQ on that module. Its characteristics are defined specifically in the Standard for that module.

2.3.6 - VDDQ, OUTPUT STAGE DRAIN POWER VOLTAGE

The power pin that is intended to feed power to the output transistors of the device to supply the Potential and energy to drive the load applied to the data output (Q) pins or data input/output (DQ) pins. Other, non-data, output pin transistors may also be designated to be fed by this power pin. VDDQ/VCCQ may be specified to have the same or a different potential from that feeding the primary device power pins (VDD/VCC) but is DC isolated on the chip from these and any other chip power pins. For chips with multiple VDDQ/VCCQ pins, there is no requirement that all of the VDDQ/VCCQ pins be DC common within the device. Since some VDDQ pins internal to the device may not be connected in common, it is recommended that external to the device ALL VDDQ pins be common.

2.3.7 - VEE, EMITTER POWER VOLTAGE

For ECL interface devices, the primary and most negative power supply terminal.

2.3.8 - VHH, SPECIAL FUNCTION ENABLE VOLTAGE

A special high voltage logic level (super voltage) that enables special on-chip functions.

2.3.9 - VPP, PROGRAMMING POWER VOLTAGE

A special high voltage supply that supplies the potential and energy for altering the state of certain non-volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).

2.3.10 - VREF, REFERENCE POWER SUPPLY

A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.

2.3.11 - VSS, (GND), GROUND REFERENCE or SOURCE POWER VOLTAGE

The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.

2.3.12 - VSSQ, (GNDQ), OUTPUT STAGE SOURCE POWER VOLTAGE or OUTPUT STAGE GROUND REFERENCE

The ground reference voltage for the data output (Q) or data input/output (DQ) pins. Other, non-data, output pin transistors may also be designated to be referenced to this ground pin. Internal to the device, it is a design decision whether this pin shall be DC isolated from the primary ground reference (VSS) pin and/or any other ground reference pin. External to the device, VSSQ must be DC common with the primary ground reference, VSS. For chips with multiple VSSQ pins, there is no requirement that all of the VSSQ pins be DC common within the device. Since some VSSQ pins internal to the device may not be connected in common, it is recommended that external to the device ALL VSSQ pins be common.

2.4 DEVICE TYPE NAMES

2.4.1 - ASIC, Programmable Application Specific Device

A complex array of logic elements whose interconnection pattern can be field programmed to fill the needs of specific applications.

2.4.2 - BDRAM, Burst DRAM

A DRAM that has BURST mode data capability.

2.4.3 - Bxxx,

Device names that have the prefix "B" are devices that have a "Burst" data capability.

2.4.4 - Burst SRAM

- Also commonly known as "Burst RAM", "Sync Burst SRAM" and similar names. A synchronous SRAM that includes an on-chip address incrementing counter controlled by three burst control pins. Originally designed to serve as a front-side L2 cache data SRAM, the burst control pins typically named ADV# (Advance-bar), ASP# (Address Strobe Processor-bar) and ASC# (Address Strobe Cache Controller-bar) were designed to facilitate the 4 beat synchronous L1 cache line fill required by 80486 and 68040 microprocessors.

2.4.5 - DPM, Dual Port Memory

Any memory that has two essentially identical data ports.

2.4.6 - DPSRAM, Dual Port Static RAM

A static RAM that contains two sets of identical random access address and data ports.

2.4.7 - DRAM, Dynamic Random Access Memory

These devices are made using Dynamic RAM circuit configurations that have data storage that must be refreshed periodically.

2.4.8 - FEEPROM, Flash EEPROM

An EEPROM in which clearing can be performed only on blocks or the entire array.

Note: there are no restrictions on the block architecture in the definition of FEEPROM. The blocks within a device may be of various capacities ranging from a single address to the entire memory array.

2.4.9 - EEPROM, Electrically Erasable Programmable Read Only Memory

A reprogrammable ROM in which cells may be erased electrically and in which each cell may be reprogrammed electrically.

2.4.10 - EPROM, Erasable Programmable Read Only Memory

A reprogrammable ROM in which all cells may be simultaneously erased using ultraviolet light and in which each cell may be reprogrammed electrically.

2.4.11 - ESDRAM, Enhanced Synchronous DRAM

An ESDRAM is functionally and architecturally equivalent to JEDEC standard SDRAM with the exception that an ESDRAM integrates a row cache per bank. A row cache as implemented in the ESDRAM is a static row register that is used for the purpose of being loaded with the selected addressed DRAM row. The row cache of a given bank is loaded on a read command or optionally a write command to the same banks. Read data always comes from the row cache, even when the DRAM is idle.

2.4.12 - GRAM, Graphics DRAM

A DRAM that contains special graphics features, similar to those contained in a MPDRAM. When the term has a prefix "S", it becomes synchronous GRAM.

2.4.13 - LPROM, Latched PROM

A PROM that contains a latch register for the output data.

2.4.14 - MPDRAM, Multiport DRAM

A dynamic RAM that contains in addition to the conventional random access data and address port, a serial access port that allows serial access to a portion of the stored data in a way which is independent of the normal RAM data terminals and in which simultaneous serial and random operations may be executed. This type of memory has been referred to as "Video RAM" because of its primary field of application.

2.4.15 - MPM, Multiport Memory

Any memory array that has two or more data ports which do not have the same architecture. The most common form of MPM is one in which there is a random access port and a serial access port.

2.4.16 - MPRAM, Multiport RAM

A RAM that has more than one port for data, address, and control, that are not identical in nature. Normally at least one port provides parallel access while one other provides serial access. When the term has a prefix "S", it becomes synchronous MPDRAM.

2.4.17 - NVRAM, Non-Volatile Random-Access Memory

An SRAM in which provisions exist on chip for the state of the cells to be saved when power is removed.

2.4.18 - PLD, Programmable Logic Array

An array of logic elements in which the interconnection pattern can be programmed (either mask or user programmed) to perform specific logic functions.

2.4.19 - PROM, Programmable Read-Only Memory

A field programmable ROM which can have the data content of each cell altered only once.

2.4.20 - PSRAM, Pseudo Static Random-Access Memory

A combinational form of dynamic RAM that incorporates various refresh and control circuits on-chip (e.g. refresh address counter and multiplexer, interval timer, and/or arbiter). These circuits allow the PSRAM operating characteristics to closely resemble those of a SRAM.

2.4.21 - RAM, Random-Access Memory

A memory in which access to all storage data can be achieved in essentially the same time, independent of the location. In a multiport memory, this term refers to that portion of the array which contains the memory cell array and its drivers, sense amplifiers, and control circuitry and the circuitry associated with the normal random access data port.

2.4.22 - ROM, Read-Only Memory

A memory in which the contents are not intended to be altered during operation.

2.4.23 - ROW CACHE

A row cache as implemented in the ESDRAM is a static row register that is used for the purpose of being loaded with the selected addressed DRAM row. The row cache of a given bank is loaded on a read command or optionally a write command to the same bank. Read data always comes from the row cache, even when the DRAM is idle.

2.4.24 - RPRM, Registered PROM

A PROM that contains a "D" type FF register for the output data.

2.4.25 - Sxxx

The prefix "S" on a device term can mean either "Static" as in SRAM, "Serial" as in SAM, or "Synchronous" as in SDRAM and SGRAM.

2.4.26 - SAM, Serial Access Memory

A memory (or serial port in a multiport memory) in which data is accessed sequentially and the time for access depends on the location of the data desired. In a multiport memory, this term refers to that portion of the device which is related to the serial access port and its associated functions.

2.4.27 - SDRAM, Synchronous DRAM, SDR or DDR

A DRAM that has a clocked synchronous interface. SDRAMs come in two versions, SDR and DDR. The SDR, Single Data Rate, is one in which one data access is achieved for each clock cycle. The DDR, Double Data Rate, is one in which there is a data access for each edge transition of the clock.

2.4.28 - SGRAM, Synchronous Graphics DRAM

A GRAM that has a synchronous interface.

2.4.29 - Sigma RAM

- One of a family of functionally distinct synchronous SRAMs that share a common package and have very similar pinouts, whose logic characteristics are programmed by three mode control pins per the following truth table:

M2	M3	M4	Function
0	0	0	Early Write, Flow through Read
0	0	1	Late Write, Flow through Read
0	1	0	RFU
0	1	1	Early Write, Pipelined Read
1	0	0	DDR
1	0	1	Double Late Write, Pipelined Read
1	1	0	Late Write, Pipelined Read
1	1	1	RFU

2.4.30 - SLDRAM, Synchronous Linked DRAM

SLDRAM is an evolution of Synchronous Dynamic Random Access Memory, SDRAM,. It differs principally from SDRAM in that a Command Link using a packet protocol replaces address and control inputs. It also uses adaptive interface to facilitate high data rate operation.

2.4.31 - SMPDRAM, SVRAM, Synchronous MPDRAM (VRAM)

An MPDRAM that has a synchronous interface on all ports.

2.4.32 - SRAM, Static Random Access Memory

A read/write memory in which the data is retained in the absence of control signals generated inside or outside the integrated circuit.

2.4.33 - SSRAM, Synchronous Static RAM

An SRAM that has input and/or output buffers (either register or latch), that are controlled by an externally supplied clock (or clocks).

2.4.34 - VC SDRAM, Virtual Channel SDRAM

Virtual Channel Memory is an SDRAM that uses multiple channels to transfer row-wide data between memory banks and channels. A segment of the row being accessed is loaded into the channel. A later access of the row will be directed to the channel. The channels, consisting of static memory, can be randomly accessed without the DRAM access overhead, affording a much faster access time. Operations of the channels are completely controlled by commands issued by the system and can be used as application specific registers.

2.4.35 - VRAM, Video Ram

A term commonly used in the Industry to describe the device class referred to in this standard as MPDRAM. It is a multi-ported DRAM that has features keyed to the video buffer application

2.5 MISCELLANEOUS DEVICE RELATED TERMS

2.5.1 - Bit Plane

In a semiconductor memory device having a data interface that is wider than 1 bit, those storage cells and associated circuitry which are associated with a given bit in the data interface.

2.5.2 - Bit Wide

A class of memory devices that have only a single-bit data interface.

2.5.3 - Byte Wide

A class of memory devices that have a parallel 8-bit or occasionally 9-bit data interface.

2.5.4 - K

When describing the storage capacity of a memory device the quantity $K=1024$ is used.

2.5.5 - M

When describing the storage capacity of a memory device, the quantity $M=2 \text{ exp } 20$ or 1024 K is used.

2.5.6 - MX, Multiplexed

A term describing a device that has pins used for different purposes at different times as a function of one or more of its control inputs. The signal groups that are multiplexed onto a common pin set are given together as in: AA MX signifying ADDRESS, ADDRESS multiplex, OR ADQ MX signifying ADDRESS, DATA IN, DATA OUT multiplex.

2.5.7 - Nibble Wide

A class of memory devices that have a parallel 4-bit data interface. This term should not be confused with "nibble mode" (see 3.1.3.2), which refers to a serial data access mode in memories.

2.5.8 - Word Wide

A class of memory devices that have a parallel 16-bit or longer data interface.

2.6 SPECIAL OPERATIONAL CYCLES FOR MPDRAM

The following terms describe a series of special operational cycles for MPDRAM. They are presented in the order of their logical relationships rather than alphabetically.

2.6.1 - LOGIC SETUP, (LS)

A special non-memory cycle in which the logic state of the device is set up to actuate the desired mode of operation for future memory cycles. The selected mode is normally persistent until canceled by some subsequent special control cycle.

2.6.2 - INTERNAL REFRESH, (CBR)

Defined in 3.9.2.3.

2.6.3 - WRITE TRANSFER, (WT)

An operation in which the data to be written is introduced through the serial port and is then transferred internally to the memory array data bus for writing into the cells. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial register into which data is entered. Data is entered serially from this point with wrap around when the end of the register is reached. The contents of the full serial register are transferred in parallel. In addition to the normal write transfer, there are numerous other types of special write transfers defined in the following paragraphs.

2.6.4 - PSEUDO WRITE TRANSFER, (PWT)

This is a non-memory cycle in which the operational mode of the serial port is changed from output to input. At the same time the "Tap Pointer" is set. This is a counter that defines the starting point in the serial data register into which data is entered. Data is entered serially from this point with wrap around when the end is reached.

2.6.5 - MASKED WRITE TRANSFER, (MWT)

A write transfer in which the transfer of new data from the serial register into the memory array is controlled by a "Write Mask" that is supplied on the DQ(n) terminals. This mask allows the selective writing of new data into one or more of the data bit planes of the storage array corresponding to the data bits of the parallel array. In a normal implementation, a high M value enables the writing of new data while a low M inhibits the writing and leaves the existing data unchanged. A new mask value must be supplied for each masked write cycle.

2.6.6 - FLASH WRITE WITH MASK, (FWM)

A write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. The "mask" value determines which bit planes are to be altered while the "color register" (qv) contains the data value to be written. The color register is loaded in a previous "Load Color Register" cycle with a persistent value. The mask value is supplied during the cycle on the DQ(n) terminals. A new mask value must be supplied for each cycle performed. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.7 - SPECIAL WRITE TRANSFER

A write transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal SAM to RAM data transfers. These variations are defined in the following paragraphs.

2.6.8 - SPLIT WRITE TRANSFER, (SWT)

A write transfer in which the SAM data register is split into two halves and the data is transferred to the RAM data bus separately after each half of the SAM register is filled.

2.6.9 - AUTO-LOAD WRITE TRANSFER, (AWT)

A split SAM data register transfer in which the transfer from each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is filled.

2.6.10 - READ TRANSFER, (RT)

A read operation in which the contents of one row of the memory array is transferred into the SAM data register in parallel.

2.6.11 - SPECIAL READ TRANSFER

A read transfer in a device that has variations in the architecture of the SAM data register to allow improved performance in the internal RAM to SAM data transfers. These variations are defined in the following paragraphs.

2.6.12 - SPLIT READ TRANSFER, (SRT)

A read transfer in which the SAM data register is split into two halves and the data is transferred from the RAM data bus separately into each half of the SAM register as it is needed for transfer to the SDQn terminals.

2.6.13 - AUTO-LOAD READ TRANSFER, (ART)

A split SAM data register transfer in which the transfer into each half is automatically triggered by the state of the tap pointer counter after each half of the SAM register is emptied.

2.6.14 - DOUBLE BUFFERED READ TRANSFER, (DRT)

A read transfer in an array that contains two full SAM data registers which are used alternately. Each one is loaded while the contents of the other is being transferred to the SDQ(n) port. The selection of the two SAM registers is automatic.

2.6.15 - RAM WRITE WITH NEW MASK, (RWNM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask which is supplied at the beginning of the write cycle on the DQ(n) terminals. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.16 - RAM WRITE WITH OLD MASK, (RWOM)

A RAM write cycle in which the data bits that are to be written are controlled by a write mask register which was loaded in a previous "load write mask" cycle. A high mask bit normally enables the write function for that bit. A low mask bit leaves the data unaltered.

2.6.17 - RAM READ/WRITE, NO MASK, (RR), (RW)

A normal RAM read or write access cycle with no SAM or special RAM features or functions actuated.

2.6.18 - BLOCK WRITE, NO MASK, (BW)

A RAM write cycle in which four (4) bits are written into each bit plane as defined by the contents of the color register. The four (4) bits are those locations controlled by the two LSB of the column address.

2.6.19 - BLOCK WRITE WITH NEW MASK, (BWNM)

A Block Write cycle in which the data written is also controlled by the write mask supplied on the DQ(n) terminals in that cycle.

2.6.20 - BLOCK WRITE WITH OLD MASK, (BWOM)

A Block Write cycle in which the data written is controlled by the contents of the write mask register which was previously loaded in a "Load Write Mask" cycle.

2.6.21 - LOAD WRITE MASK REGISTER, (LWR)

A non-memory cycle in which the write mask register is loaded with a new value for use in subsequent masked write cycles.

2.6.22 - LOAD COLOR REGISTER, (LCR)

A non-memory cycle in which the color register is loaded with a new value for use in subsequent special cycles which utilize its contents.

2.6.23 - READ WRITE MASK REGISTER, (RWR)

A non-memory cycle in which the contents of the "Write Mask Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

2.6.24 - READ COLOR REGISTER, (RCR)

A non-memory cycle in which the contents of the "Color Register" are interrogated with the results placed on the RAM data terminals, DQ(n).

2.7 Package-Related Terms

A series of package-related terms have been used in the Standard and are included in the glossary. The recently published JEDEC Standard JESD30, "Descriptive Designation System for Semiconductor-Device Packages" has obsoleted many of the package designations previously used. As new standards are published in Std. No. 21-C, the JESD30 approved term will be used or referenced. Commonly used industry package terms will be included in this section, but the reader is referred to JESD30 for definitions of the approved terms.

2.7.1 - BGA, Ball Grid Array

A package in which the external connections to the package are made via a rectangular array of ball type connections, all on a common plane.

2.7.2 - CC, Leadless or Leaded Chip Carrier

A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application.

2.7.3 - DIP, Dual-In-line Package

A device package configuration that has two parallel rows of pins that are spaced nominally 0.3", 0.4", or 0.6" apart with the pins on 0.1" centers.

2.7.4 - LCC, Lateral Chip Carrier

A family of device packages that can be square (SCC) or rectangular (RCC) depending on the application and can be with or without leads.

2.7.5 - PLDCC, Plastic Leaded Chip Carrier

A chip-carrier package that has a molded plastic body and J formed leads (see CC, 2.7.1). The often used term "PLCC" is ambiguous and is deprecated in favor of this term.

2.7.6 - PP, Pin Pitch

The nominal center to center distance between adjacent pins or terminals along the side of an IC package.

2.7.7 - QFP, Quad Flat Pack

A flat pack package that has leads on all four sides (see SFP).

2.7.8 - RCC, Rectangular Chip Carrier

See LCC, par 2.7.3.

2.7.9 - SCC, Square Chip Carrier

See LCC, par. 2.7.3.

2.7.10 - SFP, Square Flat Pack

A square package body of uniform thickness with flexible, flat leads exiting, on 0.050" centers, peripherally from the center plane of the four package sides.

2.7.11 - SIMM, Single-In-line-Memory-Module

A multichip module in which the body has a SIP form and is made up primarily of memory devices. (see SIP/SIMM and ZIP/SIMM).

2.7.12 - SIP, Single-in-line Package

A rectangular package with the leads along one side, normally one of the long sides.

2.7.13 - SIP/SIMM, SIP/SIMM Module

A multichip memory module in which the body has a SIP form, and the pins are formed into an in-line configuration.

2.7.14 - SOG, (SOP), Small Outline, Gull Wing Lead

A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "gull wing" configuration.

2.7.15 - SOJ, Small Outline J Lead

A surface mount package that conforms to the "small outline" concept and which has the leads formed into a "J" configuration.

2.7.16 - TSOP, Types I and II, TSOP1, TSOP2

These are small outline packages with gull wing lead formation and whose thickness is substantially less than the standard SOG package. TSOP1 has the leads on the end or short edges of the package while TSOP2 has the leads on the sides or long edges of the package. The lead pitch is often finer than that commonly used in the standard SOG package.

2.7.17 - ZIP, Zig-Zag In-line Package

A package whose body resembles that of a DIP, except that the external leads are all along one edge of the package. The leads emerge on 0.050" centers and are formed alternately into two rows of pins that are separated by 0.100" with the individual leads on 0.100" centers along the rows. The package is mounted standing on one edge.

2.7.18 - ZIP/SIMM, ZIP/SIMM Module

A multichip memory module in which the body has a SIP form but the leads have been formed into a ZIP foot-print.

2.8 Memory Card Pin Names

The following pin names were developed for use with the 68 pin Multiple Technology Memory Card described on pages 4-24 & 4-25. Some of these terms, however, may be used on other standards to follow. The pin names used on the card but not given in this section are standard terms defined in Sec. 2.1.

2.8.1 - BD(n), Battery Voltage Detect

The signals, BD1 and BD2 are generated by the memory card, as an indication of the condition of the battery on the memory card.

Both signals are kept asserted when the battery is in good condition. When BD2 is negated while BD1 is still asserted, the battery is in a warning condition and should be replaced, although data integrity on the card is still assured. If BD1 is negated with BD2 either asserted or negated, the battery is no longer serviceable and data is lost.

2.8.2 - CD(n), Card Detect

The CD1\ and CD2\ signals provide for proper memory card insertion detection, and have been positioned at opposite ends of the connector to facilitate the detection process. The signals are connected to ground internally on the memory card; thus they will be forced low whenever a card is placed in a host socket. The host socket interface circuitry shall provide 10K pull-up resistors to Vcc on each of these signal pins.

2.8.3 - RFU, Reserved Pins

Several pins have been identified as Reserved for Future Use. Neither memory cards, nor Host systems shall make any electrical connections to these pins.

2.8.4 - RG, Attribute Memory Select

The memory card defines two planes selected by the Register (RG\) pin. When this signal is active low, the register or Attribute Memory is selected. Normal access to main memory is obtained when the RG\ signal is high (inactive). Attribute Memory is a separately accessed section of memory on the card and is generally used to record card capacity and other configuration and attribute information. Main Memory is used to store user data.

The timing of Attribute Memory may be different than that of Main Memory's; refer to manufacturers specifications for details. When Attribute Memory is accessed, only data signals DQ0-DQ7 are valid and signals DQ8-DQ15 shall be ignored. Signals E1\ and E2\ and A0 are still valid, but it is only possible to select even addresses, (a combination of E1\|E2\|A0 that requests an odd byte will result in invalid data on the bus.

For those PC memory cards that do not have a section reserved for Attribute Memory, all Main Memory addresses shall begin with address (hex) 0H and proceed for a minimum of 16 kilobytes of contiguous space.

2.8.5 - WP, Write Protect

The WP output signal is used to reflect the status of the Write Protect switch on the memory card. If the memory card Write Protect switch is present, this signal will be asserted by the card when the switch is enabled, and deasserted when the switch is disabled. If the memory card has no Write Protect switch, the card will connect this line to ground or Vcc, depending on the condition of the card memory. If the card can always be written, the pin will be connected to VSS. If the card is permanently Write Protected, the pin will be connected to VCC.

2.9 SRAM & SSRAM SPECIAL PIN NAMES

The following standards are applicable to SRAM AND SSRAM devices. Some of the terms are also covered in Sec 2.1 on general pin names but are repeated here for completeness.

2.9.1 - $\overline{\text{ADSC}}$

Address Strobe Cache Controller-bar – A address burst counter control pin on an L2 Cache SRAM that is designed to be connected to a cache controller's address output valid strobe.

2.9.2 - $\overline{\text{ADSP}}$

Address Strobe Processor-bar – A address burst counter control pin on an L2 Cache SRAM that is designed to be connected to a processor's address output valid strobe.

2.9.3 - ADV

Advance – A control input pin that allows an internal counter (usually an address counter) to advance count, typically in response to a clock input.

2.9.4 - Bn\# - **Byte Write Enable-bar**

A write control pin that qualifies a write command by a general Write Enable pin to particular bytes (of 8 or 9 data bits each) on a multi byte device. The pin does not usually have any impact on reads.

2.9.5 - BW\#

Byte Write-bar – A write control input that enables write cycles to bytes concurrently enabled by Byte Write Enable-bar (Bx\#) pins.

2.9.6 - DCD

Dual Cycle Deselect – A mode of operation common in synchronous pipelined SRAMs where output driver deselection is implemented is pipelined to the same degree as the data flow in the data path. See SCD for contrast.

2.9.7 - $\overline{\text{FT}}$, **Flow-Through**

A control input which when driven true places the RAM register into the flow-through mode; when false, the RAM register is in Register Mode.

2.9.8 - $\overline{\text{LBO}}$, **Linear Burst Order**

A control input which when driven true causes the Burst counter to generate addresses in sequential order; when false the Burst addresses are generated in a specified interleaved order.

2.9.9 - M , **Mode Control**

A control input that implements special functions. It may be a DC or active input signal, but is always intended to be tied to a logic high level or not connected by the user unless otherwise specified.

2.9.10 - SA_n , SA , **Sync Address**

One of the clocked address inputs. In devices where the address order is significant, the SA_n form is used with the values SA_0 thru SA_n , where "n" is the binary numeric order of the address or data bit.

2.9.11 - $\overline{\text{SBx}}$, **Sync Byte "x" Write Enable**

A clocked control input that enables writes to byte "x" in conjunction with the $\overline{\text{SW}}$ input. SBx has no effect on read cycles.

2.9.12 - SCD

– Single Cycle Deselect – A mode of operation common in synchronous pipelined SRAMs where output driver deselection is implemented immediately after the deselect command is clocked into the RAM, one clock cycle sooner than the enable of the output drivers (which, in a pipelined synchronous device, is pipelined to the same degree as the data flow in the data path). See DCD for contrast.

2.9.13 - $\overline{\text{SE}}$, **Sync Enable**

A clocked control input that logically selects the RAM and removes it from power-down mode.

2.9.14 - $\overline{\text{SG}}$, **Sync Output Enable**

A clocked control input that enables output drivers

2.9.15 - $\overline{\text{SGW}}$, **Sync Global Write**

A clocked control input that writes all bytes regardless of status of Sync Byte Select ($\overline{\text{SSx}}$) or Sync Byte Write Enable ($\overline{\text{SBx}}$) inputs.

2.9.16 - $\overline{\text{SSx}}$, $\overline{\text{SS}}$, **Sync Byte "x" Select**

A clocked control input that logically selects byte "x" for reads and writes. Where no "x" designator is given, the signal selects all bits of the device.

2.9.17 - $\overline{\text{SW}}$, **Sync Write**

A clocked control input that writes all bytes, or on devices with Sync Byte Select ($\overline{\text{SSx}}$), or Sync Byte Write Enable ($\overline{\text{SBx}}$) inputs, writes all selected or enabled bytes.

2.9.18 - $\overline{\text{SWx}}$, **Sync Byte (Group) "x" Write**

A clocked control input that writes byte (group) "x". "x" takes the values of a, b, c, d, etc. In devices where the write control is applied to bit groupings that is other than a "byte", the definition still applies.

2.9.19 - TCK , **Test Port Clock**

Serial Scan Test Clock Input

2.9.20 - TDI, Test Data In

Serial Scan Data Input

2.9.21 - TDO, Test Data Out

Serial Scan Test Data Output

2.9.22 - TMS, Test Mode Select

A control input that enables Scan Test Clock, and is used to select test modes.

2.9.23 - TRST, Test Port Reset

Serial Scan Test Port Reset

2.9.24 - x, Byte or Word Identifier

In the pin names in this section and their definitions, this is an alphabetic identifier for the word or byte being accessed.

2.9.25 - ZQ, Output Impedance Control

An analog signal input that sets output buffer impedance and operating mode. .

2.9.26 - ZZ Sleep Mode Enable

A control input that logically deselects RAM and places it in Sleep Mode. Devices that implement Sleep Mode may require several cycles to implement the "Go-to-Sleep" or "Wake-up"

2.10 SLDRAM SPECIAL PIN NAMES

The following pin names are specific to the SLDRAM family of SDRAM devices defined in Sec.,3.11 of this Standard. They differ substantially from the pin names used in all other SDRAM devices so care must be exercised to prevent confusion.

2.10.1 - CAn, Command/Address n

A group of input signals used to provide command and address information (the combined command and address information associated with a specific transaction is referred to as a request packet).

2.10.2 - CCLK, Command Clock

An input that controls the input capture of command and address signals, and that serves as a master clock from which other internal clock signals are derived.

2.10.3 - CCLK \bar , Command Clock Bar

The differential complement of CCLK.

2.10.4 - DCLKn, Data Clock n

An I/O that, as an input, controls the input capture of data being written to the device, and as an output, transmits a signal along with data being read from the device so that the receiving device can use this signal to control input capture of such data. The number n allows for more than one DCLK signal, which can be used to facilitate transitions from one bus master to another. The number n does not indicate a mapping between a particular DCLK signal and some subset of data signals.

2.10.5 - DCLKn \bar , Data Clock n Bar

The differential complement of DCLKn.

2.10.6 - FLAG

A control input that indicates the start of a valid request packet (valid data on the command/address inputs).

2.10.7 - LISTEN

An input that controls the activation/deactivation of input and output circuitry for power management.

2.10.8 - LINKON

An input that controls the activation/deactivation of input, output and internal circuitry for power management.

2.10.9 - RESET \bar , Reset Bar

An input that allows the device to be asynchronously restored to a defined initial state.

2.10.10 - SI, Select In

A control input used to select the device (activate the device to respond to additional control input). Multiple devices in a system will have SI and SO signals connected in a serial manner so as to construct a single serial link among the devices.

2.10.11 - SO, Select Out

A control output used to indicate completion of a particular operation and/or allow selection of a downstream device. Multiple devices in a system will have SI and SO signals connected in a serial manner so as to construct a single serial link among the devices.

2.10.12 - TEST

An input used to initiate a vendor specific device testing mode or operation.

MCP Signal Name Glossary

Color Legend: Symbol exists within 21C

Color Legend: Symbol in **red bold** text exists within 21C, other symbol listed is commonly used within Industry

Color Legend: White indicates new symbol/definition currently NOT in JESD21C

Blue bold highlight indicates proposed changes to existing JESD21C definitions

Signal Name	Signal Type	Description
.	Rule	Where alternative functions are allowed by the standard (or different technologies), the allowed functions are listed separated by commas.
/	Rule	Where a pin has a dual-function (on same technology), and those functions are invoked at substantially different times, the names and symbols for the functions are separated by a slash (/)(e.g., VPP/G).
l, overbar, #, _n, _t, _c	Rule	Where the pin function has an inverted logic sense, that is, the function is true or invoked for a low signal, the overbar, trailing reverse slash (\), #, or _n symbol is appended to the symbol. The _t and _c symbols represent true and complementary logic states for differential pairs.
x-, x	Rule	Where the signal is specific to a technology contained within the MCP a dash (-) is used to differentiate the technologies.
D-, d	Rule	Prefix / Suffix for DRAM specific signal
F-, f	Rule	Prefix / Suffix for NOR FLASH specific signal
N-, n	Rule	Prefix / Suffix for NAND specific signal
P-, p	Rule	Prefix / Suffix for PSRAM specific Signal
S-, s	Rule	Prefix / Suffix for SRAM specific Signal
E-, e	Rule	Prefix / Suffix for eMMC specific Signal
O-, o	Rule	One / Suffix NAND
U-, u	Rule	Prefix / Suffix UFS
(n) -function	Rule	When multiple die are used, a number (n) suffix after technology name designates function order (F1-CE, F2-CE)
NC	Rule	No Connection - A pin to which no internal electrical connection is present or allowed
NU	Rule	Not Usable - A device pin to which there may or may not be an internal connection but to which no external connections are allowed.
RSVD	Rule	Reserved - In a family of standards where some devices in the family are subsets of others, terminals that are defined in some devices but not used in others. To allow for upgradeability, the unused terminals are "RESERVED" to prevent their being used. NC has often been used in similar situations.
RFU	Rule	Reserved for Future Use - A terminal whose function is not currently defined, but which is intended to be defined in some future enhancement of this Standard. This terminal should not be used (either internally or externally) until it has been further defined

MCP Signal Name Glossary (Cont'd)

ADQ31:0	I/O	ADDRESS DATA INPUT/OUTPUT: The pins that are multiplexed three ways to serve as address input, data input, and data output pins. When the address data input/output numbering is significant for device operation, the addresses are numbered, beginning with 0.
AMAX:A0	I	ADDRESS INPUTS: Those inputs that select (address) a particular cell or set of cells within a memory array for presentation on the device outputs. The integer (n) serves to differentiate the address inputs, one from another. When the address numbering is significant for device operation, the addresses are numbered, beginning with 0.
ADV#	I	ADDRESS DATA VALID: Low-true input during synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first.
ALE, AL	I	Address Latch Enable - Address is latched to the address register through NAND I/O ports on the rising edge of WE# when ALE is High
BA(n)	I	BANK ADDRESS: In a RAM that has multiple banks in its architecture, the BANK ADDRESS is used, to select any one of the available banks.
CAS \setminus	I	COLUMN ENABLE: See 21C for full definition
CE, E	I	CHIP ENABLE
CE#, E\setminus	I	CHIP ENABLE: Low-true input selects the associated memory die
CKE	I	CLOCK ENABLE: In certain synchronous memory devices, a logic level input that enables the clock input and allows it to fulfill its defined function.
CLE	I	Command Latch Enable - Commands are latched to the command register through NAND I/O ports on the rising edge of WE# when CLE is High
CLK, CK	I	CLOCK: An input that controls the activation of both input and output circuitry, normally storage registers or latches.
CLK#, CK\setminus	I	DDR CLOCK: Complement of CLK for DDR-enabled memory
CRE	I	CONTROL REGISTER ENABLE: High-true input when active write operations load the Refresh Control Register or Bus Control Register
DM(n), DQM(n)	I/O	INPUT/OUTPUT MASK: A control signal used primarily on SDRAMs that acts as mask for reading and writing functions. In some instances, the DQM term will include a prefix "U" or "L" indicating upper or lower byte control. In devices where more than two data bit groupings have a data mask applied, a "x" is applied where "x" takes the values of a, b, c, etc.
DPD	I	Deep Power Down. Control pin used with some flash memory
DQS0, DQS1...	IO	DATA STROBE PIN 0,1: Edge detector for when data is available on the bus (DQ7-0, DQ15-8 respectively)
DQ0 – DQ31	I/O	DATA INPUT/OUTPUT - see 21C for full definition
LB \setminus	I	LOWER BYTE ENABLE: An input, on wordwide devices, that, when true, enables the lower byte data input/outputs, pins DQ0 through DQ7.
N-I/O	I/O	INPUT/OUTPUT: A generic term for otherwise undefined signal pins which can have either an input and/or an output function. This term is not used as a specific pin name, only as a generic indicator of the nature of the function of the pin.
N-PRE	I	Power on auto read enable. Used with some NAND memory
OE \setminus	I	OUTPUT ENABLE: See 21C for full definition
RAS \setminus	I	ROW ADDRESS STROBE: A chip enable signal that, on certain dynamic RAMs, actuates only row address oriented internal circuitry. In modules that have multiple RAS \setminus s, the RAS \setminus s are numbered beginning with 0.

MCP Signal Name Glossary (Cont'd)

RY/BA	O	Ready / Busy: see 21C for full definition
RE#	I	Read Enable. Active low. Controls read timing. Clocking RE# increments the internal address and reads out data
RST#	I	HARDWARE RESET: Low-true input initializes internal circuitry to reading array data
UB#	I	UPPER BYTE ENABLE: An input that, on worldwide devices, when true, enables the upper byte data input/outputs, pins DQ8 through DQ15.
VREF	O	REFERENCE POWER SUPPLY: A power supply that acts as a reference for determining internal threshold voltages but does not supply any substantial power to the device.
VDD	Power	DRAIN POWER VOLTAGE: The primary power voltage on MOS devices that require a potential that is different from the normal system logic voltage. This is used interchangeably with VCC on devices that use 5 V.
VDDQ	Power	OUTPUT STAGE DRAIN POWER VOLTAGE: See 21C for full definition
ACC, VPP	I	PROGRAMMING POWER VOLTAGE: A special high voltage supply that supplies the potential and energy for altering the state of certain non-volatile memory arrays. On some devices the presence of VPP also acts as a PROGRAM ENABLE signal (see P).
VSS	Power	GROUND REFERENCE or SOURCE POWER VOLTAGE: The ground reference voltage for NMOS, CMOS, and TTL devices, commonly the reference pin for all other device pins. VSS is normally the system ground and the symbol is often used interchangeably with GND.
VSSQ	Power	OUTPUT STAGE GROUND REFERENCE: See 21C for full definition
WAIT	O	WAIT: Indicates the status of the burst read operation
WE#	I	WRITE ENABLE: see 21C for full definition
WP#	I	Write Protect: When this signal is applied to a memory module or an EEPROM, it is an input signal that when true, protects the EEPROM memory array from being written into or erased. When false, the write functions inherent in the device are activated. When applied to a memory card, it is an output signal defined in Par. 2.8.5 of this Standard.