

CONFIGURATIONS FOR SOLID STATE MEMORIES

Contents

Section	Title	Release #.....	Page #
1	Background	1	1-1
2	Terms and Definitions	1	2-1
2.1	Conventional Device Pin Names.....	9.10	2-2
2.2	Multiport DRAM Pin Names	3	2-5
2.3	Power Pin Names	9	2-6
2.4	Device Type Names.....	9.11	2-7
2.5	Miscellaneous Device Related Terms.....	1	2-9
2.6	Special Operational Cycles for MPDRAM.....	1	2-10
2.7	Package-Related Terms	5	2-12
2.8	Memory Card Pin Names.....	3	2-13
2.9	SRAM and SSRAM Special Pin Names.....	6.11	2-14
2.10	SLDRAM Special Pin Names.....	9	2-15
2.11	MCP Signal Names.....	19r20	2-17
3	Memory Device Standards	1	3-1
3.1	General Standards	1	3.1-1
3.1.1	Byte Wide.....	1	3.1-1
3.1.1.1	32K to 256K by 8 A/A MX Family in DIP	1	3.1-1
3.2	Read Only Memory (ROM)	1	3.2-1
3.2.0	ROM General Standards.....	5	3.2-2
3.2.0.1	Mask ROM Fast Address Mode Definition	5	3.2-2
3.2.1	ROM, Byte Wide	1	3.2.1-1
3.2.1.1	2K to 8K by 8 ROM Family in DIP, Type A	1	3.2.1-1
3.2.1.2	4K by 8 ROM in DIP, Type B	1	3.2.1-1
3.2.1.3	8K to 128K by 8 ROM Family in DIP.....	1	3.2.1-1
3.2.1.4	2K to 32K by 8 ROM Family in RCC.....	1	3.2.1-1
3.2.1.5	32K to 512K by 8 ROM Family in SOJ.....	1	3.2.1-1
3.2.1.6	128K to 1M by 8 ROM in DIP.....	1	3.2.1-1
3.2.1.7	64K to 512K by 9 ROM in DIP	1	3.2.1-1
3.2.1.8	2 to 64 X 16K by 8 Page Select ROM in DIP	1	3.2.1-1
3.2.1.9	512K and 1M by 8 ROM in QFP	2	3.2.1-1
3.2.2	ROM, Word Wide	1	3.2.2-1
3.2.2.1	32K to 256K by 16 ROM in DIP	1	3.2.2-3
3.2.2.2	32K to 256K by 16 ROM in SCC.....	1	3.2.2-3
3.2.2.3	16K to 256K by 16 Address/Data MX ROM in DIP	1	3.2.2-3
3.2.2.4	16K to 256K by 16 Address/Data MX ROM in RCC	1	3.2.2-3
3.2.2.5	256K and 512K by 16 ROM in QFP.....	2	3.2.2-3
3.2.2.6	512K to 128M by 16 ROM in DIP and SOP	6	3.2.2-3
3.2.2.7	512K and 1M by 16 ROM in SCC	3	3.2.2-3
3.3	Programmable Read Only Memory (PROM)	1	3.3-1
3.3.1	PROM, Nibble Wide.....	1	3.3.1-1
3.3.1.1	25K and .5K by 4 TTL PROM in DIP.....	1	3.3.1-3
3.3.1.2	25K by 4 ECL PROM in DIP	1	3.3.1-3

Contents (Cont'd)

Section	Title	Release #	Page #
3.3.1.3	1K and 2K by 4 TTL PROM in DIP	1	3.3.1-3
3.3.1.4	1K and 2K by 4 TTL PROM in SOP	1	3.3.1-3
3.3.1.5	4K to 8K by 4 TTL PROM in DIP	2	3.3.1-3
3.3.1.6	25K to 2K by 4 TTL PROM Family in RCC	1	3.3.1-3
3.3.1.7	4K by 4 TTL PROM, 4K by 4 TTL R PROM in SCC.....	1	3.3.1-3
3.3.1.8	1K to 8K TTL by 4 PROM Family in RCC	1	3.3.1-3
3.3.1.9	1K to 8K TTL by 4 PROM Family in SCC.....	1	3.3.1-3
3.3.1.10	1K to 4K by 4 D PROM Families in DIP and SCC.....	1	3.3.1-4
3.3.1.11	1K to 16K by 4 ECL PROM Family in DIP	1	3.3.1-4
3.3.2	PROM, Byte Wide	1	3.3.2-1
3.3.2.1	32 by 8 TTL PROM in DIP and SCC	1	3.3.2-3
3.3.2.2	32 by 8 ECL PROM in DIP and SCC	1	3.3.2-3
3.3.2.3	25K and .5K by 8 TTL PROM in DIP and SCC	1	3.3.2-3
3.3.2.4	25K to 8K by 8 TTL PROM Family in DIP	1	3.3.2-3
3.3.2.5	5K to 4K by 8 TTL L PROM Family in DIP	1	3.3.2-3
3.3.2.6	5K to 4K by 8 TTL R PROM Family in DIP	1	3.3.2-3
3.3.2.7	5K to 8K by 8 TTL PROM FAMILIES in RCC and SCC	1	3.3.2-3
3.3.2.8	5K to 2K by 8 TTL R PROM Family in SCC	1	3.3.2-4
3.3.2.9	16K to 64K by 8 TTL PROM Family in DIP	1	3.3.2-4
3.3.2.10	512 by 8 ECL R PROM in DIP and SCC.....	2	3.3.2-4
3.3.3	PROM, Word Wide.....	1	3.3.3-1
3.3.3.1	32 and 64 by 16 PROM in DIP and SCC	1	3.3.3-3
3.3.4	PROM Package Conversion	1	3.3.4-1
3.3.4.1	PROM DIP to SO Conversion, 16, 18, 20, 24 DIP	1	3.3.4-1
3.4	Erasable Programmable Read Only Memory (EPROM)	1	3.4-1
3.4.1	EPROM, Byte Wide.....	1	3.4.1-1
3.4.1.1	4K by 8 EPROM in DIP, Type A.....	1	3.4.1-3
3.4.1.2	4K and 8K by 8 EPROM in DIP.....	1	3.4.1-3
3.4.1.3	8K to 64K by 8 EPROM Family in DIP	1	3.4.1-3
3.4.1.4	2K to 512K by 8 EPROM Family in RCC	1	3.4.1-3
3.4.1.5	32K to 512K by 8 EPROM Family in SOJ	1	3.4.1-3
3.4.1.6	128K to 1M by 8 EPROM Family in DIP.....	1	3.4.1-3
3.4.1.7	64K to 512K by 9 EPROM Family in DIP	1	3.4.1-3
3.4.1.8	2 to 64 X 16K by 8 PAGE SELECT EPROM Family in DIP	1	3.4.1-3
3.4.1.9	128K to 512K by 8 EPROM Family in TSOP1	4	3.4.1-3
3.4.2	EPROM, Word Wide	1	3.4.2-1
3.4.2.1	32K to 256K by 16 EPROM in DIP.....	1	3.4.2-3
3.4.2.2	32K to 256K by 16 EPROM in SCC	1	3.4.2-3
3.4.2.3	16K to 256K by 16 Address/Data MX EPROM in DIP	1	3.4.2-3
3.4.2.4	16K to 256K by 16 Address/Data MX EPROM in RCC	1	3.4.2-3
3.4.2.5	512K to 128M by 16 EPROM or OTP in DIP and SOP	6	3.4.2-3
3.4.2.6	512K and 1M by 16 EPROM in SCC.....	3	3.4.2-3
3.4.2.7	64K to 256K by 16 EPROM in TSOP1	4	3.4.2-3
3.5	Electrically Erasable Programmable Read Only Memory, EEPROM	1	3.5-1
3.5.1	EEPROM, Byte Wide	1	3.5.1-1
3.5.1.1	5K to 2K by 8 EEPROM Family in DIP	1	3.5.1-2

Contents (Cont'd)

Section	Title	Release #	Page #
3.5.1.2	2K and 4K by 8 EEPROM in RCC	1	3.5.1-2
3.5.1.3	1K to 32K by 8 EEPROM Family in DIP	1	3.5.1-2
3.5.1.4	5K to 32K by 8 EEPROM Family in RCC	1	3.5.1-2
3.5.1.5	32K to 256K by 8 EEPROM Family in SOJ	1	3.5.1-2
3.5.1.6	32K to 512K by 8 EEPROM Family in DIP	1	3.5.1-2
3.5.1.7	32K to 256K by 8 EEPROM Family in RCC.....	1	3.5.1-2
3.5.1.8	32K to 256K by 9 EEPROM Family in DIP	1	3.5.1-2
3.5.1.9	128K to 1M by 8 EEPROM Family in SCC	1	3.5.1-2
3.5.1.10	32K to 256K by 8 EEPROM Family in TSOP1	2	3.5.1-3
3.5.1.11	Extended Feature Set for 256K Bit EEPROM	2	3.5.1-3
3.5.1.12	Optional Command Set for Dual-Supply EEPROM	3	3.5.1-3
3.5.1.13	512K by 8 Dual-Supply EEPROM in RCC	5	3.5.1-3
3.5.1.14	128K to 512K by 8 Single-Supply EEPROM Family in DIP RCC and TSOP1	5	3.5.1-3
3.5.1.15	256K to 512K and 1M by 8 Dual-Supply EEPROM in TSOP1.....	6	3.5.1-4
3.5.1.16	1M to 8M by 8 Single-Supply EEPROM Family in TSOP1	5	3.5.1-4
3.5.1.17	8K by 256B or 264B SERIAL ACCESS EEPROM in TSOP2	6	3.5.1-4
3.5.1.18	1M, 2M BU 8 Single- or Dual-Supply EEPROM in PSOP2.....	7	3.5.1-4
3.5.1.19	4Mb to 32Mb Density by 8 Dual Supply Flash EEPROM in 8 X 5 GRID Micro BGA Package	9	3.5.1-4
3.5.1.20	2K Bit Serial, Single-Supply EEPROM in 8 Pin SOG	9	3.5.1-4
3.5.1.21	2-WIRE EEPROM in Small Footprint Package	14	3.5.1-4
3.5.2	EEPROM, Word Wide.....	1	3.5.2-1
3.5.2.1	4K to 32K by 16 EEPROM in DIP	1	3.5.2-2
3.5.2.2	4K to 256K by 16 EEPROM in SCC	1	3.5.2-2
3.5.2.3	256K to 128M by 16 EEPROM in DIP and SOG	6	3.5.2-2
3.5.2.4	1M to 4M by 16 DS EEPROM in SSOP	6	3.5.2-2
3.5.2.5	1M to 4M Density, by 8 or 16 FEEPROM in PSOP	7	3.5.2-2
3.5.2.6	1M to 32M Density, by 8 or 16 FEEPROM in TSOP1.....	7	3.5.2-2
3.5.2.7	4Mb to 32Mb Density by 8 and 16 Dual Supply Flash EEPROM in 8 X 6 GRID Micro BGA Package	9	3.5.2-2
3.5.2.8	16Mb to 64Mb Density by 8 and 16, Dual supply Flash EEPROM in 8 X 9 GRID Micro BGA Package	9	3.5.2-3
3.5.2.9	8Mb to 128Mb Density FEEPROM/SRAM in BGA	10	3.5.2-3
3.5.2.10	4M to 64M by 16 FEEPROM in TSOP1	11	3.5.2-3
3.5.2.11	2M to 64M by 16 FEEPROM in FBGA	11	3.5.2-3
3.5.2.12	4M to 8M and 16M by 16 FEEPROM with SDRAM Interface	11	3.5.2-3
3.5.2.13	128Mb to 4Gb Density FEEPROM, User Selectable as X8 or X16 in SSOP	11	3.5.2-4
3.5.2.14	Single-Supply 16Mb and 32Mb (x16/x32) FEEPROM in 80-Pin PQFP	12	3.5.2-4
3.5.2.15	128Mb TO1Gb(x8/x16) FEEPROM in 64-Ball LBGA	14	3.5.2-4
3.5.2.16	28Mb to 1Gb (x8/x16) FEEPROM in 64-Ball LBGA	14	3.5.2-4
3.5.2.17	16Mb to 512Mb (x8/x16) FEEPROM in 52-Pin TSOP2	14	3.5.2-4
3.5.2.18	16Mb to 512Mb (x16) Synchronous 1.8V/3.0V FEEPROM in 56-Pin TSOP1	16	3.5.2-5
3.5.2.19	16Mb to 1Gb (x16) Synchronous 1.8V/3.0 VFEEPROM in 64-Ball LFBGA	16	3.5.2-5
3.5.3	EEPROM Extended FEATURES	1	3.5.3-1

Contents (Cont'd)

Section	Title	Release #	Page #
3.5.3.1	Extended Feature Set for 256Kb EEPROM	1	3.5.3-3
3.5.3.2	Dual-Supply EEPROM Command Set	7	3.5.3-13
3.5.3.3	Single-Supply EEPROM Command Codes	7	3.5.3-14
3.5.3.4	EEPROM Toggle Bit Feature	7	3.5.3-15
3.5.3.5	Synchronous DRAM Interface EEPROM (Flash) in 86-Pin TSOP2 and 90-Ball FBGA	12	3.5.3-16
3.5.3.6	EEPROM with Two SPD Software Write Protect Methods	14	3.5.3-19
3.6	Nonvolatile Random Access Memory (NVRAM).....	1	3.6-1
3.6.1	NVRAM , Nibble Wide	1	3.6-3
3.6.1.1	25K and 1K by 4 NVRAM in DIP	1	3.6-3
3.6.2	NVRAM , Byte Wide	1	3.6-3
3.6.2.1	5K, 1K by 8 NVRAM in DIP	1	3.6-3
3.6.2.2	5K and 1K by 8 NVRAM in RCC	1	3.6-3
3.6.2.3	5K to 16K by 8 NVRAM Family in DIP	1	3.6-3
3.6.2.4	5K to 16K by 8 NVRAM Family in RCC	1	3.6-3
3.6.2.5	32K to 256K by 8 NVRAM Family in SOJ	1	3.6-3
3.6.2.6	32K to 256K by 8 NVRAM Family in DIP	1	3.6-3
3.6.2.7	16K to 128K by 9 NVRAM Family in DIP	1	3.6-3
3.6.3	LPDDR NVRAM	18	3.6.3-1
3.7	Static Random Access Memory (SRAM).....	1	3.7-1
3.7.1	JTAG Extension to Revolutionary Pinout SRAM Devices	4	3.7-1
3.7.1	Bit Wide TTL SRAM	1	3.7.1-1
3.7.1.1	25K and 1K by 1 TTL SRAM in DIP	1	3.7.1-3
3.7.1.2	25K and 1K by 1 TTL SRAM in SCC.....	1	3.7.1-3
3.7.1.3	4K to 2M by 1 TTL SRAM Family in DIP	1	3.7.1-3
3.7.1.4	16K by 1 TTL SRAM in RCC.....	1	3.7.1-3
3.7.1.5	64K by 1 TTL SRAM in RCC.....	1	3.7.1-3
3.7.1.6	16K to 2M by 1 TTL SRAM in SOJ.....	5	3.7.1-3
3.7.1.7	256K to 16M by 1 TTL SRAM and 4M by 1 SSRAM in DIP, SOJ, and TSOP2	4	3.7.1-3
3.7.1.8	256K by 1 TTL SRAM in RCC.....	1	3.7.1-3
3.7.1.9	4M and 16M SRAMConfigurable to X1 or X4 in DIP, SOJ, and TSOP2	4	3.7.1-3
3.7.2	Bit Wide ECL SRAM.....	1	3.7.2-1
3.7.2.1	1K to 256K by 1 ECL SRAM Family in DIP	1	3.7.2-3
3.7.2.2	256K to 16M by 1 ECL SRAM and 4M by 1 SSRAM in DIP, SOJ, and TSOP2	4	3.7.2-3
3.7.2.3	64K and 256K by 1 ECL SRAM in FLATPACK	2	3.7.2-3
3.7.2.4	256K to 16M by 1 ECL SSRAM Family in DIP, SOJ, and TSOP2	4	3.7.2-3
3.7.3	Nibble Wide TTL SRAM	1	3.7.3-1
3.7.3.1	16 by 4, Inverting and Noninverting TTL SRAM in DIP and SCC	1	3.7.3-3
3.7.3.2	25K by 4 TTL SRAM in DIP and RCC.....	1	3.7.3-3
3.7.3.3	256 by 4 TTL SRAM with G in SCC	1	3.7.3-3
3.7.3.4	4K to 64K by 4 TTL SRAM without G Family in DIP	1	3.7.3-3
3.7.3.5	4K by 4 TTL SRAM in RCC.....	1	3.7.3-3
3.7.3.6	4K to 1M by 4 TTL SRAM with G Family in DIP.....	1	3.7.3-3
3.7.3.7	16K to 256K by 4 TTL SRAM with and without G Family in RCC	1	3.7.3-3
3.7.3.8	16K and 64K by 4 TTL SRAM in RCC	1	3.7.3-3

Contents (Cont'd)

Section	Title	Release #	Page #
3.7.3.9	4K to 1M by 4 TTL SRAM with and without G Family in SOJ, and TSOP2	5	3.7.3-4
3.7.3.10	64K to 4M by 4 TTL SRAM in DIP, SOJ, and TSOP2	4	3.7.3-4
3.7.3.11	64K to 4M by 4 TTL SRAM with Separate Data I/O in DIP, SOJ, and TSOP2	4	3.7.3-4
3.7.3.12	64K to 4M by 4 Synchronous SRAM (SSRAM) in DIP, SOJ, and TSOP2	4	3.7.3-4
3.7.3.13	4K and 16K by 4 CACHE TAG SRAM in DIP and SOJ	1	3.7.3-4
3.7.3.14	4M and 16M SRAM, Configurable to X1 or X4 in DIP and SOJ	1	3.7.3-4
3.7.4	Nibble Wide ECL SRAM	1	3.7.4-1
3.7.4.1	25K and 1K by 4, 100K ECL SRAM in DIP and SFP	1	3.7.4-3
3.7.4.2	1K to 16K by 4, 10K and 100K ECL SRAM in DIP	1	3.7.4-3
3.7.4.3	25K to 16K by 4, 10K and 100K ECL SRAM Family in DIP	1	3.7.4-3
3.7.4.4	16K by 4, 10K and 100K ECL SSRAM in DIP	1	3.7.4-3
3.7.4.5	64K to 4M by 4 ECL SRAM in DIP, SOJ, and TSOP2	4	3.7.4-3
3.7.4.6	64K to 4M by 4 ECL SRAM with Separate Data I/O in DIP, SOJ, and TSOP2	4	3.7.4-3
3.7.4.7	64K to 4M by 4 ECL Synchronous SRAM (SSRAM) in DIP, SOJ, and TSOP2	4	3.7.4-4
3.7.4.8	64K by 4 ECL SRAM in FP	2	3.7.4-4
3.7.4.9	256K by 4/512K by 2 Reconfigurable SRAM in DIP and SOJ	2	3.7.4-4
3.7.4.10	64K to 4M by 4 SRAM Family in DIP and SOJ in DIP, SOJ, and TSOP2	4	3.7.4-4
3.7.4.11	64K to 4M by 4 SSRAM Family in SIP and SOJ in DIP, SOJ, and TSOP2	4	3.7.4-4
3.7.4.12	64K to 4M by 4 SSRAM Family in SIP and SOJ in DIP, SOJ, and TSOP2	4	3.7.4-4
3.7.5	Byte Wide TTL SRAM	1	3.7.5-1
3.7.5.1	64 by 9 TTL SRAM in SCC	1	3.7.5-3
3.7.5.2	1K and 2K by 8 TTL SRAM in DIP	1	3.7.5-3
3.7.5.3	2K and 4K by 8 TTL SRAM in RCC	1	3.7.5-3
3.7.5.4	2K to 32K by 8 TTL SRAM Family in DIP and SOJ	1	3.7.5-3
3.7.5.5	5K to 32K by 8 TTL SRAM Family in RCC	1	3.7.5-3
3.7.5.6	32K to 512K by 8 TTL SRAM Family in SOJ or TSOP2	4	3.7.5-3
3.7.5.7	64K to 512K by 8 TTL SRAM Family in DIP	1	3.7.5-3
3.7.5.8	32K to 256K by 9 TTL SRAM Family in DIP	1	3.7.5-3
3.7.5.9	32K to 2M by 8 and 512K to 2M by 9 TTL SRAM in DIP, SOJ, and TSOP2	4	3.7.5-3
3.7.5.10	32K and 128K by 8 TTL SSRAM in DIP and SOJ	1	3.7.5-3
3.7.5.11	2K to 32K by 9 DPSRAM Family in 68 SCC	1	3.7.5-3
3.7.5.12	32K by 9 CACHE SRAM in 44 SCC	2	3.7.5-3
3.7.5.13	128K by 8 SRAM in TSOP1	2	3.7.5-3
3.7.5.14	128K by 8 and 9 SSRAM in SOJ	2	3.7.5-3
3.7.5.15	1K and 2K by 8 DPSRAM Family in 48 DIP	2	3.7.5-3
3.7.5.16	128K to 512K by 8 SRAM Family in 32 CDSO-N	3	3.7.5-3
3.7.5.17	128K to 512K by 8 and 9 SSRAM and 128K by 9 SRAM in 33 DIP and SOJ	3	3.7.5-4
3.7.5.18	128K to 2M by 8/9 Burst SRAM in BGA	5	3.7.5-4
3.7.5.19	128K to 2M by 8/9 SSRAM in BGA	5	3.7.5-4
3.7.5.20	32K by 8 SRAM in TSOP1	7	3.7.5-4

Contents (Cont'd)

Section	Title	Release #	Page #
3.7.5.21	128K to 16M by 9 SYNC Separate I/O SRAM in 209 BGA	12	3.7.5-4
3.7.5.22	128K to 16M by 9 SYNC Separate I/O SRAM in 221 BGA	12	3.7.5-4
3.7.6	Byte Wide ECL SRAM.....	1	3.7.6-1
3.7.6.1	32K and 128K by 8 ECL SSRAM in SOJ, SSOP, and FP	2	3.7.6-1
3.7.7	Word Wide TTL SRAM.....	11	3.7.7-1
3.7.7.1	4K to 64K by 16 TTL SRAM in DIP	1	3.7.7-2
3.7.7.2	4K to 256K by 16 TTL SRAM in SCC.....	1	3.7.7-2
3.7.7.3	16K to 256K by 16 Address/Data MX TTL SRAM in DIP	1	3.7.7-2
3.7.7.4	16K to 256K by 16 Address/Data MX TTL SRAM in RCC	1	3.7.7-2
3.7.7.5	16K and 64K by 18 SRAM in SCC	1	3.7.7-2
3.7.7.6	64K by 16 and 18 SRAM in 44 SOJ.....	3	3.7.7-2
3.7.7.7	32K and 64K by 16 and 18 SRAM and SSRAM in 52 SCC with Logic Features	4	3.7.7-2
3.7.7.8	64K to 256K by 18 SRAM and SSRAM in TQFP	5,15	3.7.7-3
3.7.7.9	64K to 1M by 16/18 Burst SRAM in BGA	5,15	3.7.7-3
3.7.7.10	64K to 1M by 16/18 SSRAM in BGA.....	5,15	3.7.7-3
3.7.7.11	64K to 256K by 16/18 Burst SRAM in QFP/TQFP	6,15	3.7.7-3
3.7.7.12	256K and 1M by 16/18 SRAM in TSOP2	6	3.7.7-3
3.7.7.13	1Mb to 128Mb Density, by 16 or 18 Burst SRAM in 221 BGA.....	16	3.7.7-3
3.7.7.14	1Mb to 128Mb Density, by 16 or 18 SIGMA SRAM in 209 BGA, with Common I/O	11,15	3.7.7-3
3.7.7.15	1Mb to 128Mb Density, by 16 or 18 SIGMA SRAM in 221 BGA, with Common I/O	16	3.7.7-3
3.7.7.16	1Mb to 128Mb Density, by 18 Sigma SRAM in 209 BGA, with Separate I/O	12	3.7.7-4
3.7.7.17	1Mb to 128Mb Density, by 18 Sigma SRAM in 221 BGA, with Separate I/O	16	3.7.7-4
3.7.7.18	8Mb to 128Mb Density, by 18 SRAM in 165 BGA, with Separate I/O	12	3.7.7-4
3.7.7.19	2Mb to 256Mb Density, by 16 or 18 Burst SRAM in 165 BGA, with Common I/O	12,15	3.7.7-4
3.7.7.20	2Mb to 256Mb Density, by 16 or 18 Network SRAM in 165 BGA, with Common I/O	12,15	3.7.7-4
3.7.7.21	52-Pin TSOP II Pin Assignment for Low Power SRAMs	14	3.7.7-4
3.7.8	Double Word Wide SRAM.....	5	3.7.8-1
3.7.8.1	32K to 128K by 36 SSRAM with Burst in TQFP	6,15	3.7.8-2
3.7.8.2	32K to 128K by 36 SRAM and SSRAM in TQFP	5,15	3.7.8-2
3.7.8.3	32K to 512K by 32/36 Burst SRAM BGA PADOUT	5,15	3.7.8-2
3.7.8.4	32K to 512K by 32/36 SSRAM BGA PADOUT	5c,11,15	3.7.8-2
3.7.8.5	16K to 36K by 32 and 64 SSRAM With Burst Counter in QFP	7	3.7.8-2
3.7.8.6	16K to 256K by 36 and 72 Burst SRAM in BGA	7,16	3.7.8-2
3.7.8.7	1Mb to 128Mb Density, by 32 or 36 Burst SRAM in 221 BGA	11,16	3.7.8-2
3.7.8.8	1Mb to 128Mb Density, by 32 or 36 SIGMA SRAM in 209 BGA, with Common I/O	11	3.7.8-3
3.7.8.9	1Mb to 128Mb Density, by 32 or 36 SIGMA SRAM in 221 BGA, with Common I/O	11,16	3.7.8-3
3.7.8.10	1Mb to 128Mb Density, by 36 SIGMA SRAM in 209 BGA, with Separate I/O	12	3.7.8-3
3.7.8.11	1Mb to 128Mb Density, by 36 SIGMA SRAM in 221 BGA, with Separate I/O	12,16	3.7.8-3

Contents (Cont'd)

Section	Title	Release #	Page #
3.7.8.12	16Mb to 256Mb Density, by 36 SRAM in 165 BGA, with Separate I/O	12	3.7.8-3
3.7.8.13	8Mb to 128Mb Density, by 36 DDR SRAM in 165 BGA, with Common I/O	12	3.7.8-3
3.7.8.14	2Mb to 256Mb Density, by 32 or 36 Burst SRAM in 165 BGA, with Common I/O	12,15	3.7.8-3
3.7.8.15	2Mb to 256Mb Density, by 32 or 36 Network SRAM in 165 BGA, with Common I/O	12, 15	3.7.8-4
3.7.9	Eight Byte Wide SRAM	11a	3.7.9-1
3.7.9.1	1Mb to 128Mb Density, by 64 or 72 Burst SRAM in 209 BGA	11a,16	3.7.9-2
3.7.9.2	1Mb to 128Mb Density, by 64 or 72 Burst SRAM in 221 BGA	11a,16	3.7.9-2
3.7.9.3	1Mb to 128Mb Density, by 64 or 72 SIGMA SRAM in 209 BGA	11a	3.7.9-2
3.7.9.4	1Mb to 128Mb Density, by 64 or 72 SIGMA SRAM in 221 BGA	11a,16	3.7.9-2
3.7.10	High Speed DDR SRAM in 165 BGA	17	3.7.10-1
3.8	Pseudostatic Random Access Memory (PSRAM)	1	3.8-1
3.8.1	PSRAM Byte Wide	1	3.8-3
3.8.1.1	2K to 8K by 8 PSRAM Family in DIP	1	3.8-3
3.8.1.2	2K to 16K by 8 PSRAM Family in RCC	1	3.8-3
3.8.1.3	32K to 512K by 8 PSRAM Family in SOJ	1	3.8-3
3.8.2	PSRAM Word Wide	1	3.8-3
3.8.2.1	4K to 32K by 16 PSRAM in DIP	1	3.8-3
3.8.2.2	4K to 256K by 16 PSRAM in SCC	1	3.8-3
3.8.2.3	8M to 6M by 16 Burst PSRAM in BGA	15	3.8-3
3.8.2.4	16Mb to 512Mb by 16 PSRAM in VFPGA	16	3.8-3
3.9	Dynamic Random Access Memory (DRAM)	1	3.9-1
3.9.1	Bit Wide DRAM	1	3.9.1-1
3.9.1.1	16K by 1 DRAM in DIP with 3 Supply Voltages	1	3.9.1-3
3.9.1.2	16K to 256K by 1 DRAM Family in DIP	1	3.9.1-3
3.9.1.3	16K to 256K by 1 DRAM in RCC	1	3.9.1-3
3.9.1.4	64K and 256K by 1 DRAM in ZIP	1	3.9.1-3
3.9.1.5	1M and 4M by 1 DRAM Family in DIP	1	3.9.1-3
3.9.1.6	1M to 16M by 1 DRAM Family in SOJ or TSOP2	4	3.9.1-3
3.9.1.7	1M to 16M by 1 DRAM Family in ZIP	4	3.9.1-3
3.9.1.8	1M to 16M by 1 NON-MUX DRAM Family in SOJ	1	3.9.1-3
3.9.1.9	1M by 1 DRAM in TSOP1	1	3.9.1-4
3.9.1.10	16M by 1/4M by 4 Configurable DRAM in SOJ	1	3.9.1-4
3.9.1.11	64M by 1 DRAM in SOJ or TSOP2	5	3.9.1-4
3.9.1.12	2 X 16M by 1 DRAM in TSOP2	4	3.9.1-4
3.9.1.13	16M by 1 DRAM in USON	9	3.9.1-4
3.9.2	Nibble Wide DRAM	1	3.9.2-1
3.9.2.1	16K and 64K by 4 DRAM in DIP	1	3.9.2-2
3.9.2.2	16K by 4 DRAM in DIP	1	3.9.2-2
3.9.2.3	64K by 4 DRAM in RCC	1	3.9.2-2
3.9.2.4	256K and 1M by 4 DRAM Family in DIP	2	3.9.2-2
3.9.2.5	256K to 4M by 4 DRAM Family in SOJ and TSOP2	4	3.9.2-2
3.9.2.6	64K to 4M by 4 DRAM in ZIP	2	3.9.2-2
3.9.2.7	256K and 1M by 4 DRAM with 4 CE in SOJ and TSOP2	3	3.9.2-2
3.9.2.8	256K by 4 DRAM in TSOP1	2	3.9.2-2

Contents (Cont'd)

Section	Title	Release #	Page #
3.9.2.9	16M by 1/4M by 4 Configurable DRAM in SOJ	2	3.9.2-3
3.9.2.10	256K to 4M by 4 Non-Mux DRAM Family in SOJ	2	3.9.2-3
3.9.2.11	4M by 4 DRAM with 1 CE and 4 CE in TSOP2	2	3.9.2-3
3.9.2.12	16M by 4 DRAM in SOJ and TSOP2	5,7	3.9.2-3
3.9.2.13	1M, 2M, 4M by 2 DRAM in SOJ and TSOP2	3,7	3.9.2-3
3.9.2.14	16M by 4 DRAM with 4 CAS in SOJ and TSOP2	6	3.9.2-3
3.9.2.15	64M by 4 DRAM in TSOP2 Pin Rotation	6	3.9.2-3
3.9.2.16	4M by 4 DRAM in USON.....	9	3.9.2-4
3.9.2.17	16M by 4 DRAM in USON.....	9	3.9.2-4
3.9.3	Byte Wide DRAM	1	3.9.3-1
3.9.3.1	32K by 8 DRAM in DIP.....	1	3.9.3-3
3.9.3.2	32K by 8 DRAM in RCC.....	1	3.9.3-3
3.9.3.3	512K by 8 and by 9 DRAM in SOJ, TSOP2, and ZIP	2	3.9.3-3
3.9.3.4	512K by 8 and by 9 Non-Mux DRAM in SOJ	2	3.9.3-3
3.9.3.5	2M by 8 and 9 DRAM in SOJ and TSOP2	5	3.9.3-3
3.9.3.6	8M by 8 and 9 DRAM in SOJ and TSOP2	5	3.9.3-3
3.9.3.7	32M by 8 DRAM in TSOP2 Pin Rotation	6	3.9.3-3
3.9.3.8	4M and 8M by 8 DRAM in SOP.....	8	3.9.3-4
3.9.3.9	2M by 8 DRAM in USON.....	9	3.9.3-4
3.9.3.10	8M by 8 DRAM in USON.....	9	3.9.3-4
3.9.4	Word Wide DRAM.....	1	3.9.4-1
3.9.4.1	64K by 16 DRAM with 2 W in SOJ and TSOP2	1	3.9.4-3
3.9.4.2	256K and 1M by 16 and 18 DRAM with 2 CE in SOJ and TSOP2	5	3.9.4-3
3.9.4.3	256K by 16 DRAM with Extended Functions in DIP and SOJ.....	4	3.9.4-3
3.9.4.4	2M by 16, 4M by 16 and 18 DRAM in TSOP2	6,7	3.9.4-3
3.9.4.5	128K and 256K by 16 Burst DRAM with 2 CAS in SOJ, TSOP2, and ZIP	6	3.9.4-3
3.9.4.6	16M by 16 DRAM in TSOP2 Pin Rotation	6	3.9.4-4
3.9.4.7	128K ANS 256K by 32 DRAM with 4 CAS in TSOP2	6	3.9.4-4
3.9.4.8	512K and 2M by 32 and 36 DRAM with 4 CAS in TSOP2	6,10	3.9.4-4
3.9.4.9	8M by 32 DRAM in TSOP2 Pin Rotation	6,9	3.9.4-4
3.9.4.10	2M by 32 DRAM in TSOP2	7	3.9.4-4
3.9.4.11	2M by 32 DRAM with EDO in QFP.....	6,8	3.9.4-4
3.9.4.12	1M by 16 DRAM in USON.....	9	3.9.4-4
3.9.4.13	4M by 16 DRAM in USON.....	9	3.9.4-4
3.9.5	DRAM Optional Features	1	3.9.5-1
3.9.5.1	OPTIONAL Operational Modes and cycles for DRAM.....	1	3.9.5-3
3.9.5.2	1M DRAM Built in Test Function	1	3.9.5-3
3.9.5.3	On-Chip Refresh Control for X8 DRAM	1	3.9.5-3
3.9.5.4	G Before E Refresh.....	1	3.9.5-3
3.9.5.5	DRAM Special Test and Operational Modes	1	3.9.5-3
3.9.5.6	Non-Multiplexed DRAM Operation	1	3.9.5-3
3.9.5.7	DRAM Extended Data Out Definition	6	3.9.5-3
3.9.5.8	256m DRAM Test Mode Data and Address Compression	7	3.9.5-3
3.9.5.9	Pipelined Nibble Mode Definition	7	3.9.5-3

Contents (Cont'd)

Section	Title	Release #	Page #
3.10	Multiport Dynamic RAM (MPDRAM)	1	3.10-1
3.10.1	Nibble Wide MPDRAM.....	1.....	3.10.1-1
3.10.1.1	64K by 4 MPDRAM in DIP, SOJ, and ZIP	1.....	3.10.1-1
3.10.1.2	256K by 4 MPDRAM in DIP, SOJ, TSOP2, and ZIP	3.....	3.10.1-1
3.10.1.3	256K by 4 MPDRAM in SOJ.....	2.....	3.10.1-1
3.10.2	Byte Wide MPDRAM.....	1.....	3.10.2-1
3.10.2.1	128K and 256K by 8 MPDRAM in DIP, SOJ, and TSOP2	3.....	3.10.2-1
3.10.3	Word Wide MPDRAM	1.....	3.10.3-1
3.10.3.1	128K and 256K by 16 MPDRAM in SOG with Multiple Clocks	2.....	3.10.3-1
3.10.3.2	128K and 256K by 16 MPDRAM in TSOP2 with Multiple Clocks	5.....	3.10.3-1
3.10.3.3	256K by 16 SGRAM in TSOP2.....	6.....	3.10.3-1
3.10.3.4	128K, 256K, and 512K by 32, 2 and 4 Bank SGRAM in QFP/TQFP.....	6,9,10.....	3.10.3-1
3.10.3.5	256K by 32 GRAM in TSOP2	6.....	3.10.3-1
3.10.3.6	256K by 32 SMPDRAM in TSOP2.....	6.....	3.10.3-2
3.10.3.7	256K by 32 SMPDRAM in TSOP2.....	7.....	3.10.3-2
3.10.3.8	256K by 32 MPDRAM in TSOP2	7.....	3.10.3-2
3.10.3.9	128K, 256K, and 512K by 32 X 4 Bank Synchronous DDR SGRAM in LQFP	9.....	3.10.3-2
3.10.3.10	4M by 32 DDR SGRAM (4 Bank) in FBGA	11.....	3.10.3-2
3.10.3.11	8M by 32 GDDR3 Graphics RAM in 144-Ball FBGA	13.....	3.10.3-2
3.10.4	MPDRAM Optional Features	1.....	3.10.4-1
3.10.4.1	256K X 4 MPDRAM Minimum Feature Set Truth Table	1.....	3.10.4-3
3.10.4.2	256K X 4 MPDRAM Extended Feature Set Truth Table.....	1.....	3.10.4-3
3.10.4.3	MPDRAM Bit Write Optional Feature	1.....	3.10.4-3
3.10.4.4	128K X 8 MPDRAM Minimum Feature Set Truth Table	1.....	3.10.4-3
3.10.4.5	128K X 8 MPDRAM Extended Feature Set Truth Table.....	1.....	3.10.4-3
3.10.4.6	128K X 16, 256K X 8, and 256K X 16 MPDRAM Minimum Feature Set Truth Table	5.....	3.10.4-3
3.10.4.7	128K X 16, 256K X 8, and 256K X 16 MPDRAM Extended Feature Set Truth Table	5.....	3.10.4-3
3.10.4.8	Split Register with Programmable Stops for MPDRAM	3.....	3.10.4-3
3.10.4.9	Pipelined Fast Page Mode for MPDRAM	2.....	3.10.4-4
3.10.4.10	Extended Data Out Fast Page Mode for MPDRAM.....	2.....	3.10.4-4
3.10.4.11	SAM Length Definition for 2/4M MPDRAM	5.....	3.10.4-4
3.10.4.12	Synchronous GRAM SPECIAL Mode Set Procedure	6.....	3.10.4-4
3.10.4.13	Synchronous MPDRAM SPECIAL Mode Set Procedure	6.....	3.10.4-4
3.10.4.14	Synchronous GRAM Operational Function Truth Tables.....	6.....	3.10.4-4
3.10.4.15	8Mb MPDRAM Feature Set Function Table	7.....	3.10.4-4
3.10.4.16	Extended Functions for SGRAM and MPDRAM	6,7.....	3.10.4-4
3.11	Synchronous Dynamic Random Access Memory (SDRAM)	4	3.11-1
3.11.1	Bit Wide SDRAM.....	4.....	3.11.1-1
3.11.2	Nibble Wide SDRAM.....	4.....	3.11.2-1
3.11.2.1	4M by 4 SDRAM in TSOP2.....	6,7,8.....	3.11.2-1
3.11.2.2	16M by 4 SDRAM in TSOP2.....	6.....	3.11.2-1
3.11.2.3	64M by 4 SDRAM in TSOP2 Pin Rotation	7,9	3.11.2-1
3.11.2.4	16M, 32M, 64M, 128M, and 256M by 4 DDR SDRAM in TSOP2	8,9,10,11,12.....	3.11.2-1
3.11.2.5	32M, 64M, 64M, and 256M by 4 SDRAM in TSOP2	8,9,10,12.....	3.11.2-1

Contents (Cont'd)

Section	Title	Release #	Page #
3.11.2.6	16M by 4 Virtual Channel SDRAM in TSOP2	9	3.11.2-1
3.11.2.7	16M, 32M, and 64M by 4 Stackable SDR SDRAM in LSOJ	9	3.11.2-2
3.11.2.8	16M, 32M, and 64M by 4 Virtual Channel DDR SDRAM in TSOP2	9,11	3.11.2-2
3.11.2.9	16M, 32M, 64M, and 128M by 4 Stackable DDR SDRAM in LSOJ	9,10,11	3.11.2-2
3.11.2.10	16M by 4 SDR SDRAM in USON.....	9	3.11.2-2
3.11.2.11	16M, 32M, and 64M by 4 SDR SDRAM in TSOP2	9	3.11.2-2
3.11.2.12	16M, and 32M by 4 SDR SDRAM in LFBGA	9	3.11.2-2
3.11.2.13	16M, and 32M by 4 DDR SDRAM in LFBGA	9	3.11.2-3
3.11.2.14	16M, and 32M by 4 SDR SDRAM in LFBGA	9	3.11.2-3
3.11.2.15	16M, and 32M by 4 DDR SDRAM in LFBGA	9,11	3.11.2-3
3.11.2.16	64M, and 128M by 4 SDR SDRAM in LFBGA	11a	3.11.2-3
3.11.2.17	16M, 32M, 64M, and 128M by 4 DDR SDRAM in LFBGA	11a	3.11.2-3
3.11.2.18	16M, 32M, 64M, and 128M by 4 DDR SDRAM in FBGA, with Optional Support Balls	12	3.11.2-3
3.11.2.19	64M, 128M, 256M, 512M, and 1G by 4 DDR2 SDRAM in TFBGA	12,13	3.11.2-4
3.11.2.20	16M, 32M, 64M, and 128M by 4 SDRAM in sTSP	12	3.11.2-4
3.11.2.21	64M, 128M, 256M, 512M, and 1G by 4 by 2 DDR2 SDRAM in Stacked FBGA	13	3.11.2-4
3.11.2.22	64M, 28M, 256M, 512M, and 1G by 4 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls	13	3.11.2-4
3.11.3	Byte Wide SDRAM.....	4	3.11.3-1
3.11.3.1	2M by 8 or 9 SDRAM in TSOP2.....	6,7	3.11.3-1
3.11.3.2	8M by 8 SDRAM in TSOP2.....	6	3.11.3-1
3.11.3.3	32M by 8 SDRAM Pin Rotation.....	7,9	3.11.3-1
3.11.3.4	8M, 16M, 32M, 64M, and 128M by 8 DDR SDRAM in TSOP2	8,9,10,11,12	3.11.3-1
3.11.3.5	16M, 32M, 64M, and 128M by 8 SDRAM in TSOP2	8,9,10,12	3.11.3-1
3.11.3.6	8M, 16M, and 32M by 8 SDR SDRAM in TSOP2	9	3.11.3-1
3.11.3.7	8M, 16M, and 32M by 8 Stackable SDR SDRAM in LSOJ	9	3.11.3-2
3.11.3.8	8M, 16M, 32M, and 64M by 8 Stackable DDR SDRAM in LSOJ	9,10,11	3.11.3-2
3.11.3.9	2M by 8 SDR SDRAM in USON.....	9	3.11.3-2
3.11.3.10	8M by 8 SDR SDRAM in USON.....	9	3.11.3-2
3.11.3.11	8M by 8 Virtual Channel SDRAM in TSOP2	9	3.11.3-2
3.11.3.12	8M, 16M, and 32M by 8 Virtual Channel DDR SDRAM in TSOP2.....	9,11	3.11.3-2
3.11.3.13	8M, and 16M by 8 SDR SDRAM in LFBGA	9	3.11.3-3
3.11.3.14	8M, and 16M by 8 DDR SDRAM in LFBGA	9	3.11.3-3
3.11.3.15	8M, and 16M by 8 SDR SDRAM in LFBGA	9	3.11.3-3
3.11.3.16	8M, 16M, 32M, and 64M by 8 DDR SDRAM in LFBGA	9,11	3.11.3-3
3.11.3.17	16M, 32M, and 64M by 8 Low Power SDR SDRAM in FBGA.....	11a	3.11.3-3
3.11.3.18	32M, and 64M by 8 SDR SDRAM in LFBGA	11a	3.11.3-3
3.11.3.19	16M, 32M, 64M, and 128M by 8 DDR SDRAM in FBGA	11a	3.11.3-4
3.11.3.20	16M, 32M, 64M, and 128M by 8 DDR SDRAM in 60 Ball FBGA, with Optional Support Balls	12	3.11.3-4
3.11.3.21	32M, 64M, 128M, 256M, and 512M by 8 DDR2 SDRAM in 60-Ball TFBGA	12,13	3.11.3-4
3.11.3.22	8M, 16M, 32M, and 64M by 8 SDRAM in sTSP	12	3.11.3-4
3.11.3.23	32M, 64M, 128M, 256M, and 512M by 8 by 2 DDR2 SDRAM in Stacked FBGA	13	3.11.3-4
3.11.3.24	32M, 64M, 128M, 256M, and 512M by 8 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls	13	3.11.3-4

Contents (Cont'd)

Section	Title	Release #	Page #
3.11.4	WORD Wide SDRAM	5.....	3.11.4-1
3.11.4.1	256K by 16 and 1M by 16/18 SDRAM in TSOP2	6,7.....	3.11.4-1
3.11.4.2	2M and 4M by 16 SDRAM in TSOP2.....	6,7.....	3.11.4-1
3.11.4.3	16M by 16 SDRAM in TSOP2 Pin Rotation	6,9.....	3.11.4-1
3.11.4.4	128K, 256K, and 512K, 2 and 4 Bank by 32 SDRAM in QFP/TQFP/LQFP	6,7,9,10.....	3.11.4-1
3.11.4.5	2M by 32 SDRAM in TSOP2.....	6,7,10.....	3.11.4-1
3.11.4.6	8M by 32 SDRAM in TSOP2 Pin Rotation	6,9.....	3.11.4-2
3.11.4.7	2M by 32 and 36, 4M and 8M by 32 SDRAM in TSOP2	7,8,10,11a,12.....	3.11.4-2
3.11.4.8	4M, 8M, 16M, 32M, and 64M by 16 DDR SDRAM in TSOP2	8,9,10,11,12.....	3.11.4-2
3.11.4.9	8M, 16M, 32M, and 64M by 16 SDRAM in TSOP2	8,9,10,12.....	3.11.4-2
3.11.4.10	4M, 8M, and 16M by 16 SDR SDRAM in TSOP2	9.....	3.11.4-2
3.11.4.11	4M, 8M, and 16M by 16 Stackable SDR SDRAM in LSOJ	9.....	3.11.4-2
3.11.4.12	4M, 8M, 16M, 32M, and 64M by 16 Stackable DDR SDRAM in LSOJ.....	9,11,12.....	3.11.4-3
3.11.4.13	4M by 16 SDR SDRAM in USON	9.....	3.11.4-3
3.11.4.14	4M by 16 Virtual Channel SDRAM in TSOP2	9.....	3.11.4-3
3.11.4.15	4M, 8M, and 16M by 16 Virtual Channel DDR SDRAM in TSOP2	9,11.....	3.11.4-3
3.11.4.16	4M, and 8M by 16 SDR SDRAM in LFBGA	9,12.....	3.11.4-3
3.11.4.17	4M, and 8M by 16 DDR SDRAM in LFBGA	9.....	3.11.4-3
3.11.4.18	4M, and 8M by 16 SDR SDRAM in LFBGA	9.....	3.11.4-4
3.11.4.19	4M, and 8M by 16 DDR SDRAM in LFBGA	9,11.....	3.11.4-4
3.11.4.20	4M by 16/18 SLDRAM in TSOP2.....	9.....	3.11.4-4
3.11.4.21	4M to 64M by 16/18 SLDRAM in R-PZIP	9.....	3.11.4-4
3.11.4.22	128K, 256K, and 512K by 32, 4 Bank DDR SDRAM in LQFP	9,10,11.....	3.11.4-4
3.11.4.23	2M and 4M by 32, 4 Bank DDR SDRAM in FBGA	11a.....	3.11.4-4
3.11.4.24	8M, 16M, 32M, and 64M by 16 Low Power SDR SDRAM in FBGA	11a.....	3.11.4-5
3.11.4.25	16M, and 32M by 16 SDR SDRAM in FBGA	11a.....	3.11.4-5
3.11.4.26	8M, 16M, 32M, and 64M by 16 DDR SDRAM in FBGA	11a.....	3.11.4-5
3.11.4.27	2M and 4M by 32 SDR SDRAM in LFBGA	11a.....	3.11.4-5
3.11.4.28	2M, 4M, 8M, and 16M by 32, Low Power SDR SDRAM in FBGA	11a,12,13.....	3.11.4-5
3.11.4.29	8M, 16M, 32M, and 64M by 16 DDR SDRAM in FBGA with Optional Support Balls	12.....	3.11.4-5
3.11.4.30	16M, 32M, 64M, 128M, and 256M by 16 DDR2 SDRAM in TFBGA.....	12,13.....	3.11.4-6
3.11.4.31	4M, 8M, 16M, and 32M by 16 SDRAM in sTSOP	12.....	3.11.4-6
3.11.4.32	16M, 32M, 64M, 128M, and 256M by 16 by 2 DDR2 SDRAM in Stacked FBGA13.....		3.11.4-6
3.11.4.33	16M, 32M, 64M, 128M, and 256M by 16 by 2 DDR2 SDRAM for Stacked FBGA Requiring Support Balls	13.....	3.11.4-6
3.11.4.34	4M by 32 DDR2 SDRAM in 144-Ball LF-XBGA	13.....	3.11.4-6
3.11.4.35	8M by 16 DDR SDRAM in 78-Ball BGA.....	14.....	3.11.4-7
3.11.4.36	8M, 16M, and 32M by 32 Low Power DDR SDRAM in 90-Ball FBGA.....	14,15.....	3.11.4-7
3.11.4.37	256M, 512M, 1G, and 2G by 32 DDR2 SDRAM in 128-Ball BGA	17.....	3.11.4-7
3.11.5	SDRAM Architectural and Operational Features (See P 3.11.5-1 for detailed Table of Contents)	4-9,12.....	3.11.5-1
3.11.5.1	General SDRAM Functions.....	4,9,12,13.....	3.11.5.1-1
3.11.5.2	DDR Specific SDRAM Functions	9,12.....	3.11.5.2-1
3.11.5.3	ESDRAM Specific SDRAM Functions	9.....	3.11.5.3-1
3.11.5.4	VCSDRAM Specific SDRAM Functions.....	9.....	3.11.5.4-1
3.11.5.5	DDR2 Specific SDRAM Functions.....	13,18.....	3.11.5.5-1

Contents (Cont'd)

Section	Title	Release #	Page #
3.11.5.6	GDDR2 Specific SDRAM Functions.....	13	3.11.5.6-1
3.11.5.7	GDDR3 Specific SDRAM Functions.....	14,15	3.11.5.7-1
3.11.5.4	GDDR4 Specific SDRAM Functions.....	16	3.11.5.8-1
3.11.6	SDRAM Parametric Specifications.....	9	3.11.6-1
3.11.6.1	DDR SDRAM/SGRAM I/O Voltage	9	3.11.6-3
3.11.6.2	256M SDRAM/SGRAM Refresh Standard	9	3.11.6-3
3.11.6.3	16MB and 64MB Timing Specifications (LVTTTL)	8	3.11.6-4-6
3.11.6.4	Standard for Double Data Rate (DDR) SDRAM/SGRAM Input Interface	9	3.11.6-7
3.11.6.5	DDR SDRAM Self-Refresh Exit Timing.....	9	3.11.6-8
3.11.6.6	AC Timing Parameters for DDR SDRAMs/SGRAMs	9	3.11.6-9-19
3.12	Multi-Chip Packages (MCP).....	16	3.12-1
3.12.1	MCP and Discrete eMMC, e2MMC, and UFS	17,18,19,20,22,22A,22B,23,23A,25,27	3.12.1-1
3.12.2	Package-on-Package (PoP) and Internal Stacked Module (ISM)	17,18,19, 20, 21, 22	3.12.2-1
3.12.3	Silicon Pad Sequences	16	3.12.3-1
3.20	Memory Device Complete Standard Annex	11	3.20-1
3.20.1	DDR SDRAM Device Standard	11	3.20-1
3.20.2	DDR2 SDRAM Device Standard	11,12	3.20-1
4	Multi-Chip Memory Modules and Cards	7,11	4-1
4.1	Memory Module Nomenclature and General Features	7,11,13,17,18	4.1-1
4.1.1	Memory Module Nomenclature	1-7	4.1-1
4.1.2	Serial Presence Detect General Standard	1-7,9,18,19	4.1.2-1
4.1.2.1	Annex A, Table of Fundamental Memory Types	8,9,12	4.1.2.1-1
4.1.2.2	Annex B, Table of Superset Memory Types	7,9,11	4.1.2.2-1
4.1.2.3	Annex C, SPD for FP and EDO DRAM.....	7	4.1.2.3-1
4.1.2.4	Annex D, SPD for DDR SDRAM (Rev. 1.0)	7,11,12,13	4.1.2.4-1
4.1.2.5	Annex E, SPD for SDR SDRAM.....	7,8 _{2c} ,9,11,12	4.1.2.5-1
4.1.2.6	Annex F, SPD for Address MX ROM	7	4.1.2.6-1
4.1.2.7	Annex G, SPD for Fully Buffered DIMM (Rev 1.1)	9,16	4.1.2.7-1
4.1.2.8	Annex H, Table of ESDRAM Attributes	9	4.1.2.8-1
4.1.2.9	Annex I, SPD for VCSDRAM.....	9A	4.1.2.9-1
4.1.2.10	Annex J, SPDs for DDR2 SDRAM Revisions 1.0, 1.2, and 1.3.....	17	4.1.2.10-1
4.1.2.11	Annex K, SPDs for DDR3 SDRAM Revision 6.0	18, 20, r21, 22, 24	4.1.2.11-1
4.1.2.12	Annex L, SPDs for DDR4 SDRAM Revision 1.0	23, 23A, 25	4.1.2.12-1
4.1.2.L-4	Annex L, Doc Release 4, SPDs for DDR4 SDRAM	26, 27	4.1.2.L.4-1
4.1.2.M-1	Annex M, Doc Release 1, SPDs for LPDDR3 and LPDDR4 SDRAM.....	25	4.1.2.M-1
4.1.2.M-2	Annex M, Doc Release 2, SPDs for LPDDR3 and LPDDR4 SDRAM.....	26	4.1.2.M-1
4.1.3	Definition of the EE1002 and EE1002A SPD EEPROMs.....	17,19	4.1.3-1
4.1.4	Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor	18,19, 21	4.1.4-1
4.1.5	TS3000 Standalone Thermal Sensor Component	19,19A	4.1.5-1
4.1.6	EE1004 and TSE2004 Device Specifications	22, 24, 25, r26	4.1.6-1
4.2	One Byte Modules	7	4.2-1
4.2.1	22 Pin SIP/SIMM 4 bit DRAM Module.....	1-7	4.2-1
4.2.2	24 Pin SIP/SIMM 4 bit DRAM Module.....	1-7	4.2-1

Contents (Cont'd)

Section	Title	Release #	Page #
4.2.3	30 Pin SIP/SIMM 8 or 9 bit DRAM Module	4-7.....	4.2-1
4.2.4	30 Pin SIP/SIMM 1, 2, 4, 5, or 8 bits DRAM Module Family	1-7.....	4.2-1
4.2.5	23/25/26/28 Pin ZIP/SIMM 1 or 4 bit DRAM Module Family	1-7.....	4.2-2
4.2.6	60 Pin ZIP/SIMM 4 bit SRAM Module.....	1-7.....	4.2-2
4.2.7	70 Pin ZIP/SIMM 9 bit SRAM Module.....	1-7.....	4.2-2
4.3	Two Byte Modules and Cards.....	7.....	4.3-1
4.3.1	76 Pin ZIP/SIMM 9 or 18 bit SRAM Module	1-7.....	4.3-1
4.3.2	40 Pin SIP/SIMM 1, 2, 4, 5, 8, 9, 16, or 18 DRAM MOD Family	1-7.....	4.3-1
4.3.3	60 Pin DRAM 16 or 18 bit Card Family.....	2-7.....	4.3-1
4.3.4	68 Pin Multiple Technology Memory 16-Bit Card Family	3-7.....	4.3-1
4.4	Four Byte Modules and Cards.....	7.....	4.4-1
4.4.1	64 and 72 Pin ZIP/SIMM 32 bit SRAM Module	6-7.....	4.4.1-1
4.4.2	72 Pin SIMM 32 or 36 bit DRAM Module Family and 72 Pin SIMM 36 or 39 DRAM ECC Module Family	6-7.....	4.4.2-1
4.4.3	88 Pin, 32/36/39 bit DRAM Card Family.....	6-7.....	4.4-1
4.4.4	72 Pin 32 or 36 bit DRAM SO-DIMM Family	5-7.....	4.4.4-1
4.4.5	88 Pin 32 or 36 bit DRAM SO-DIMM Family	5-7.....	4.4.5-1
4.4.6	112 Pin 32 bits MPDRAM SO-DIMM Family	5-7.....	4.4.6-1
4.4.7	80 Pin 32 bit EEPROM SIMM Family	4-7c8.....	4.4.7-1
4.4.8	100 Pin 32, 36, or 40 Bit DRAM, SDRAM, ROM DIMM Family	7.....	4.4.8-1
4.5	Eight Byte Modules and Cards	7,8,9,12.....	4.5-1
4.5.1	168 Pin Buffered DRAM, 64, 72, or 80-Bit DIMM Family	6-7.....	4.5.1-1
4.5.2	200 Pin SDRAM, 64, 72, or 80, DIMM Family	5-7c8c9,11.....	4.5.2-1
4.5.3	168 Pin Unbuffered DRAM, 64, 72, or 80, DIMM Family with SPD	5-7.....	4.5.3-1
4.5.4	168 Pin Unbuffered SDRAM, 64, 72, or 80, DIMM Family with SPD	5-7c8.....	4.5.4-1
4.5.5	144 Pin Unbuffered DRAM, 64, or 72, SO-DIMM Family with SPD	5-7,8.....	4.5.5-1
4.5.6	144 Pin Unbuffered SDRAM, 64, or 72, SO-DIMM Family with SPD	5-7.....	4.5.6-1
4.5.7	168 Pin Registered SDRAM, 64, 72, or 80, DIMM Family with SPD	8,11.....	4.5.7-1
4.5.8	144 Pin SGRAM SDRAM, 32, and 64, SO-DIMM Family with SPD	8,10.....	4.5.8-1
4.5.9	144 Pin SGRAM SO-DIMM Family.....	9.....	4.5.9-1
4.5.10	184 Pin Unbuffered DDR SDRAM DIMM Family	9.....	4.5.10-1
4.5.11	184 Pin Unbuffered SDR SDRAM DIMM Family	10.....	4.5.11-1
4.5.12	184 Pin DIMM Family Supplementary Design Standards.....	10.....	4.5.12-1
4.5.13	144 and 168 Pin Processor Enhanced Memory Module Families with EDO-DRAM or SDRAM	10.....	4.5.13-1
4.5.13.1	PEMM Specific Terms and Definitions.....	10.....	4.5.13-2
4.5.13.2	PEMM Modes OF Operation.....	10.....	4.5.13-3
4.5.13.3	Representative Block Diagrams.....	10.....	4.5.13-12
4.5.14	240 Pin Unbuffered and Registered DDR2 SDRAM DIMM Family.....	12.....	4.5.14-1
4.6	Sixteen Byte Modules.....	7.....	4.6-1
4.6.1	278 Pin Buffered SDRAM, 144 Bit DIMM Family	7.....	4.6.1-1
4.7	Mobile Platform Memory Module Thermal Sensor Component	15.....	4.7-1
4.8	DDR3 240-Pin Connector S-Parameters Specification.....	21.....	4.8-1
4.20	Module Standard Annex	11,12,13,14,15,16,17,18,19,22,23,24.....	4.20-1
4.20.1	Standard Template for JEDEC Module Specification Standards	11.....	4.20.1-1
4.20.2	168 Pin PC133 SDRAM Registered DIMM Design Standard	11.....	4.20.2-1

Contents (Cont'd)

Section	Title	Release #	Page #
4.20.3	144 Pin PC133 SDRAM Unbuffered SO-DIMM Reference Design Standard	11	4.20.3-1
4.20.4	184 Pin PC1600/2100 DDR SDRAM Registered DIMM Design Standard	11,12	4.20.4-1
4.20.5	184 Pin PC1600/2100 DDR SDRAM Unbuffered DIMM Design Standard	11,12	4.20.5-1
4.20.6	200 Pin PC3200/PC2700 DDR SDRAM Unbuffered SO-DIMM Reference Design Standard	11,13	4.20.6-1
4.20.7	184 Pin, PC2700/3200 DDR SDRAM Registered DIMM Reference Design Standard, Rev. 2.09 1	2,14,15,16	4.20.7-1
4.20.8	184 Pin, PC3200/PC2700 DDR SDRAM Unbuffered DIMM with TSOP-Based DRAMs Reference Design Standard	12,13	4.20.8-1
4.20.9	100 Pin, DDR SDRAM Unbuffered 32b DIMM Reference Design Standard, Rev 1.1	13,14	4.20.9-1
4.20.10	240-Pin PC2-3200/4200/5300/6400 DDR2 SDRAM Registered DIMM Reference Design Standard, Rev. 3.98	14,15,16,18,19,19A	4.20.10-1
4.20.11	200-Pin PC2-6400/PC2-5300/PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered SO-DIMM Reference Design Standard, Rev. 2.5	18	4.20.11-1
4.20.12	214-Pin PC2-4200/PC2-3200 DDR2 SDRAM Unbuffered MicroDIMM Reference Design Standard, Rev 0.5	14	4.20.12-1
4.20.13	240-Pin PC2-3200/4200/5300/6400 DDR2 SDRAM Unbuffered DIMM Reference Design Standard, Rev. 3.1	14,15,16,18,22	4.20.13-1
4.20.14	244-Pin, PC2-4200/PC2-3200 DDR2 SDRAM Registered Mini-DIMM Reference Design Standard, Rev. 2.0	16	4.20.14-1
4.20.15	240-Pin, PC2-4200/PC2-5300/PC2-6400 DDR2 SDRAM Fully Buffered DIMM Reference Design Standard, Rev. 3.0	16	4.20.15-1
4.20.16	144-Pin, EP2-2100 DDR2 SDRAM 32b-SO-DIMM Reference Design Standard, Rev. 1.0	16	4.20.16-1
4.20.17	214-Pin PC2-12800/ DDR3 SDRAM Unbuffered MicroDIMM Reference Design Standard, Rev 0.34	17	4.20.17-1
4.20.18	204-Pin PC3-6400/PC3-8500/PC3-10600 DDR3 SDRAM Unbuffered SO-DIMM Reference Design Standard	17,18,20,22,23,23A,23B,24	4.20.18-1
4.20.19	204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Unbuffered DIMM Reference Design Standard	18,19,20,21,22	4.20.19-1
4.20.20	204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard, Rev. 0.80	18,21,22	4.20.20-1
4.20.20.A	Annex A, R/C A in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,20,21	4.20.20-A1
4.20.20.B	Annex B, R/C B in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,20,21	4.20.20-B1
4.20.20.C	Annex C, R/C C in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,20,21	4.20.20-C1
4.20.20.D	Annex D, R/C D in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18	4.20.20-D1
4.20.20.E	Annex E, R/C E in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,20,21	4.20.20-E1
4.20.20.F	Annex F, R/C F in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,19,21	4.20.20-F1
4.20.20.G	Annex G, R/C G in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18	4.20.20-G1
4.20.20.H	Annex H, R/C H in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,19	4.20.20-H1
4.20.20.J	Annex J, R/C J in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18,20,21	4.20.20-J1

Contents (Cont'd)

Section	Title	Release #	Page #
4.20.20.K	Annex K, R/C K in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18, 21	4.20.20-K1
4.20.20.L	Annex L, R/C L in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18, 22	4.20.20-L1
4.20.20.M	Annex M, R/C M in 204-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Reference Design Standard	18	4.20.20-M1
4.20.20.N	Annex N, R/C N in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	19, 22	4.20.20-N1
4.20.20.U	Annex U, R/C U in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	22	4.20.20-U1
4.20.20.V	Annex V, R/C V in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	21	4.20.20-V1
4.20.20.W	Annex W, R/C W in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	19	4.20.20-W1
4.20.20.Y	Annex Y, R/C Y in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	19	4.20.20-Y1
4.20.20.AB	Annex AB, R/C AB in PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification.....	19,21	4.20.20-AB1
4.20.21	EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification, Revision 0.05.....	19, 22	4.20.21-1
4.20.21.A	Annex A, R/C A, in EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification, Revision	21	4.20.21-A1
4.20.21.B	Annex B, R/C B, in EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification, Revision.....	21	4.20.21-B1
4.20.21.C	Annex C, R/C C, in EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification, Revision.....	21, 23	4.20.21-C1
4.20.21.D	Annex D, R/C D, in EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification, Revision.....	21, 21,23	4.20.21-D1
4.20.22	EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	22	4.20.22-1
4.20.22.A	Annex A, R/C A, in EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	22	4.20.22-A1
4.20.22.B	Annex B, R/C B, in EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	22,23	4.20.22-B1
4.20.22.C	Annex C, R/C C, in EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	22	4.20.22-C1
4.20.22.D	Annex D, R/C D, in EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	22	4.20.22-D1
4.20.23	240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/ PC3-17000 DDR3 SDRAM Registered DIMM Design Specification.....	22	4.20.23-1
4.20.23.M	Annex M, R/C M, in 240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/ PC3-17000 DDR3 SDRAM Registered DIMM Design Specification.....	22	4.20.23-M1
4.20.23.AD	Annex AD, R/C AD, in 240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3- 14900/ PC3-17000 DDR3 SDRAM Registered DIMM Design Specification.....	22	4.20.23-AD1
4.20.24	240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/ PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	24	4.20.24-1
4.20.24.A	Annex A, R/C A, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/ PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	24	4.20.24-A1
4.20.24.C	Annex C, R/C C, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/ PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	24	4.20.24-C1
4.20.24.K	Annex K, R/C K, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/ PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced		

Contents (Cont'd)

Section	Title	Release #	Page #
	DIMM Design Specification	24	4.20.24-K1
4.20.25	260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24, 25, 25A, 26	4.20.25-1
4.20.25.A	Annex A, R/C A, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24, 26, 27	4.20.25-A1
4.20.25.B	Annex B, R/C B, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	26	4.20.25-B1
4.20.25.C	Annex C, R/C C, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	26, 27	4.20.25-C1
4.20.25.D	Annex D, R/C D, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24	4.20.25-D1
4.20.25.E	Annex E, R/C E, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24, 25, 27	4.20.25-E1
4.20.25.F	Annex F, R/C F, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24	4.20.25-F1
4.20.25.G	Annex G, R/C G, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	24, 26	4.20.25-G1
4.20.25.H	Annex H, R/C H, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/ PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	26, 27	4.20.25-H1
4.20.26	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification.....	24, 25, 25A, 26	4.20.26-1
4.20.26.A	Annex A, R/C A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	24, 25	4.20.26-A1
4.20.26.B	Annex B, R/C B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	24, 25, 27	4.20.26-B1
4.20.26.C	Annex C, R/C C, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	26	4.20.26-C1
4.20.26.D	Annex D, R/C D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	24, 25	4.20.26-D1
4.20.26.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	25, 25A	4.20.26-E1
4.20.27	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	24, 25	4.20.27-1
4.20.27.A	Annex A, R/C A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	24	4.20.27-A1
4.20.27.B	Annex B, R/C B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	24	4.20.27-B1
4.20.27.D	Annex D, R/C D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	26	4.20.27-D1
4.20.27.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	24	4.20.27-E1
4.20.28	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25, 25A, 26	4.20.28-1
4.20.28.A	Annex A, R/C A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	25, 25A, 26	4.20.28-A1

Contents (Cont'd)

Section	Title	Release #	Page #
4.20.28.B	Annex B, R/C B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25, 27	4.20.28-B1
4.20.28.C	Annex C, R/C C, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	25, 27	4.20.28-C1
4.20.28.D	Annex D, R/C D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25, 26	4.20.28-D1
4.20.28.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25, 26, 27	4.20.28-E1
4.20.28.F	Annex F, R/C F, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25	4.20.28-F1
4.20.28.G	Annex G, R/C G, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 25	4.20.28-G1
4.20.28.H	Annex H, R/C H in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	26, 27	4.20.28-H1
4.20.28.J	Annex J, R/C J, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/ PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	24, 26	4.20.28-J1
4.20.29	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Non-Volatile NAND-Flash DIMM Design Specification	26	4.20.29-1
5	Programmable Logic and ASIC Devices.....	1	5-1
5.1	Pin Out Standards.....	1	5-1
5.1.1	Pin-Out Standards for PLD DIP to SCC Conversion	4	5-1
5.1.1.1	20 Pin DIP to 20 Terminal SCC, 0.350" by 0.350", Figure 5-1.....	1	5-1
5.1.1.2	24 Pin DIP to 28 Terminal SCC, 0.450" by 0.450", Figure 5-2.....	1	5-1
5.1.1.3	28 Pin DIP to 28 Terminal SCC, 0.450" by 0.450", Figure 5-2.....	1	5-1
5.1.1.4	24 Pin Functions in 28 Pin DIP and 28 Terminal SCC, Figure 5-9	1	5-1
5.1.1.5	20 Pin Functions in 28 Terminal SCC and 24 Pin DIP for High Speed Operation, Figure 5-11	4	5-1
5.1.2	Power Pin Locations for PLD and ASIC DEVICES	1	5-1
5.1.2.1	Power Pin Locations for ECL PLD in DIP	1	5-1
5.1.2.2	Power Pin Locations for TTL PLD in DIP and CC	1	5-1
5.1.2.3	Power Pin Locations for TTL Programmable ASIC in DIP and CC.....	1	5-1
5.1.2.4	Power Pin Locations for PLD in 132 Pin QFP	1	5-1
5.1.3	Nomenclature for FPLD	1	5-1
5.1.4	PLD Data Transfer Format.....	1	5-1
5.1.5	PLD Standard Output Loads.....	5	5-1
6	Applicable Other Documents.....	1	6-1
6.1	JEDEC Standard Manufacturers Identification Code, JEP106A.....	1	6-1
6.2	JEDEC Interface Standard for Low Voltage TTL-Compatible Devices (LVTTTL), JESD8 and JESD8-1	1	6-1
6.3	JEDEC Package Outlines, JEP95	1	6-1
6.4	JEDEC PLD Data Transfer Format, JESD3-B	1	6-1

Tables

Table	Title	Release #	Page #
6.5	Nomenclature for FPLD, EIA Standard RS-428	1	6-1
6.6	JEDEC DDR SDRAM Device Standard, JESD79	11	6-1
6.7	JEDEC DDR SDRAM Device Standard, JESD79-2	16	6-2
6.8	JEDEC DDR SDRAM Device Standard, JESD79-3	16	6-2
6.9	JEDEC Specialty DDR2-1066 SDRAM Standard, JESD208	17	6-2
6.10	JEDEC LPDDR SDRAM Standard, JESD290.....	17	6-2
Annex A	(Informative) Differences Between Release 27 and Release 26.....		A-1

Figures

Figure	Title	Release #	Page #
3.10.4-1	256K X 4 MPDRAM Feature Set Truth Table	1	3.10.4-5
3.10.4-2	128K X 8 MPDRAM Feature Set Truth Table	1	3.10.4-6
3.10.4-3	2Mb and 4Mb MPDRAM Feature Set Truth Table	5	3.10.4-8
3.10.4-4A-C	SGRAM Function Truth Table	6,7	3.10.4-17-19
3.10.4-5	8Mb Burst MPDRAM Function Table	7	3.10.4-20

Figures (Cont'd)

Figure	Title	Release #	Page #
3.1-1	32K to 256K A/A Multiplexed Memory in DIP	1	3.1-2
3.2.1-1	2K to 8K by 8 ROM in DIP, Types A and B	1	3.2.1-2
3.2.1-2	8K to 128K by 8 ROM in DIP	1	3.2.1-3
3.2.1-3	2K to 32K by 8 ROM in CC.	1	3.2.1-4
3.2.1-4	32K to 512K by 8 ROM in SOJ.....	1	3.2.1-5
3.2.1-5	128K to 1M by 8 ROM in DIP	1	3.2.1-6
3.2.1-6	64K to 512K by 9 ROM in DIP.....	1	3.2.1-7
3.2.1-7	2 to 64 X 16K by 8 Page Select	1	3.2.1-8
3.2.1-8	512K and 1M by 8 ROM in QFP.....	2	3.2.1-9
3.2.2-1	32K to 256K by 16 ROM in DIP.....	1	3.2.2-5
3.2.2-2	32K to 256K by 16 ROM in CC	1	3.2.2-6
3.2.2-3	16K to 256K by 16 AQ MX ROM in DIP	1	3.2.2-7
3.2.2-4	16K to 256K by 16 AQ MX ROM in CC.....	1	3.2.2-8
3.2.2-5	256K and 512K by 16 ROM in QFP.....	2	3.2.2-9
3.2.2-6	4M to 128M by 16 ROM in DIP and SOP	2	3.2.2-10
3.2.2-7	512K and 1M by 16 ROM in SCC	3	3.2.2-11
3.2.2-8	512K to 2M by 16 ROM in DIP and SOG	6	3.2.2-12
3.3.1-1	.25K to 2K by 4 TTL PROM in DIP	1	3.3.1-5
3.3.1-2	256 by 4 ECL PROM in DIP	1	3.3.1-6
3.3.1-3	1K and 2K by 4 TTL PROM in SOG.....	1	3.3.1-7
3.3.1-4	4K and 8K by 4 TTL PROM in DIP	2	3.3.1-8
3.3.1-5	.25K to 4K by 4 TTL PROM Family in CC	1	3.3.1-9
3.3.1-6	1K to 8K by 4 TTL PROM in RCC	1	3.3.1-10
3.3.1-7	1K to 8K by 4 TTL PROM in SCC	1	3.3.1-11
3.3.1-8	1K to 4K by 4 TTL DPROM in DIP	1	3.3.1-12
3.3.1-9	1K to 4K by 4 DPROM in CC	1	3.3.1-13
3.3.1-10	1K to 16K by 4 ECL PROM in DIP	1	3.3.1-14
3.3.2-1	32 by 8 TTL and ECL PROM in DIP.....	1	3.3.2-5
3.3.2-2	32, 256, and 512 by 8 TTL PROM in CC, 32 by 8 ECL PROM in CC	1	3.3.2-6
3.3.2-3	256 and 512 by 8 TTL PROM in DIP.....	1	3.3.2-7
3.3.2-4	.25K to 8K by 8 TTL PROM in DIP.....	1	3.3.2-8
3.3.2-5	.5K to 4K by 8 TTL LPROM in DIP.....	1	3.3.2-9
3.3.2-6	.5K to 4K by 8 TTL RPPROM in DIP	1	3.3.2-10
3.3.2-7	.5K to 8K by 8 TTL PROM in SCC	1	3.3.2-11
3.3.2-8	.5K to 8K by 8 TTL PROM in RCC.....	1	3.3.2-12
3.3.2-9	.5K to 2K by 8 RPPROM in CC	1	3.3.2-13
3.3.2-10	16K to 64K by 8 TTL PROM in DIP.....	1	3.3.2-14
3.3.2-11	512 by 8 10K and 100K ECL RPPROM in DIP and SCC	2	3.3.2-15
3.3.3-1	32 and 64 by 16 TTL PROM in DIP.....	1	3.3.3-5
3.3.3-2	32 and 64 by 16 TTL PROM in CC	1	3.3.3-6
3.3.4-1	1K and 2K TTL PROM 18 DIP to 20 SO CONVERSION	1	3.3.4-3
3.4.1-1	4K and 8K by 8 EPROM in DIP, TYPES A and B	1	3.4.1-5
3.4.1-2	8K to 64K by 8 EPROM in DIP.....	1	3.4.1-6
3.4.1-3	2K to 512K by 8 EPROM in CC.....	1	3.4.1-7
3.4.1-4	32K to 512K by 8 EPROM in SOJ.....	1	3.4.1-8
3.4.1-5	128K to 1M by 8 EPROM in DIP	1	3.4.1-9
3.4.1-6	64K to 512K by 9 EPROM in DIP.....	1	3.4.1-10

Figures (Cont'd)

Figure	Title	Release #	Page #
3.4.1-7	2 to 64 X 16K by 8 Page Select EPROM in DIP	1	3.4.1-11
3.4.1-8	128K to 512K by 8 EPROM in TSOP1	4	3.4.1-12
3.4.2-1	32K to 256K by 16 EPROM in DIP	1	3.4.2-5
3.4.2-2	32K to 256K by 16 EPROM in SCC.....	1	3.4.2-6
3.4.2-3	16K to 256K by 16 Address/Data MX EPROM in DIP	1	3.4.2-7
3.4.2-4	16K to 256K by 16 Address/Data MX EPROM in RCC	1	3.4.2-8
3.4.2-5	4M to 128M by 16 EPROM or OTP in DIP and SOP	1	3.4.2-9
3.4.2-6	512K and 1M by 16 EPROM in CC.....	3	3.4.2-10
3.4.2-7	64K by 256K by 16 EPROM in TSOP1	4	3.4.2-11
3.4.2-8	512K to 2M by 16 EPROM in DIP and SOG	6	3.4.2-12
3.5.1-1	0.5K to 2K by 8 EEPROM in DIP	1	3.5.1-5
3.5.1-2	2K and 4K by 8 EEPROM in RCC	1	3.5.1-6
3.5.1-3	1K to 32K by 8 EEPROM Family in DIP	1	3.5.1-7
3.5.1-4	0.5K to 32K by 8 EEPROM Family in RCC	1	3.5.1-8
3.5.1-5	32K to 256K by 8 EEPROM Family in SOJ	1	3.5.1-9
3.5.1-6	32K to 512K by 8 EEPROM Family in DIP	1	3.5.1-10
3.5.1-7	32K to 256K by 8 EEPROM Family in RCC	1	3.5.1-11
3.5.1-8	32K to 256K by 9 EEPROM Family in DIP	1	3.5.1-12
3.5.1-9	128K to 1M by 8 EEPROM Family in SCC	1	3.5.1-13
3.5.1-10	32K to 256K by 8 EEPROM Family in TSOP1	2	3.5.1-14
3.5.1-11	Dual-Supply EEPROM Command Set	3	3.5.1-23
3.5.1-12	512K by 8 Dual-Supply EEPROM in RCC	5	3.5.1-24
3.5.1-13	128K to 512K Single-Supply EEPROM Family in DIP	5	3.5.1-25
3.5.1-14	128K to 512K Single-Supply EEPROM Family in RCC	5	3.5.1-26
3.5.1-15	128K to 512K Single-Supply EEPROM Family in TSOP1	5	3.5.1-27
3.5.1-16	1M by 8 Dual-Supply EEPROM in TSOP1	5	3.5.1-28
3.5.1-17	1M to 8M Single-Supply EEPROM Family in TSOP1	5	3.5.1-29
3.5.1-18	256K and 512K by 8 Dual-Supply EEPROM in TSOP1	6	3.5.1-30
3.5.1-19A-C	8K by 256B or 264B Serial Access EEPROM in TSOP2	6	3.5.1-31-33
3.5.1-20	1M, 2M BU 8 Single or Dual-Supply EEPROM in PSOP1	7	3.5.1-34
3.5.1-21	512K to 4096K X 8 Dual Supply Flash EEPROM in 8 X 5 Grid Micro BGA Package	9	3.5.1-35
3.5.1-22	2K Bit Serial, Single-Supply EEPROM in 8 Pin SOG	9	3.5.1-36
3.5.1-23	2-Wire EEPROM, MLP 2X3 MM Pinout	14	3.5.1-37
3.5.2-1	4K to 32K by 16 EEPROM Family in DIP	1	3.5.2-6
3.5.2-2	4K to 256K by 16 EEPROM Family in SCC	1	3.5.2-7
3.5.2-3	4M to 128M by 16 EEPROM Family in DIP and SOG	2	3.5.2-8
3.5.2-4	256K to 2M by 16 EEPROM Family in DIP and SOG	6	3.5.2-9
3.5.2-5	1M to 4M by 16 DS EEPROM in SSOP	6	3.5.2-10
3.5.2-6	1M to 4M Density by 8 or 16 FEEPROM in PSOP	7	3.5.2-11
3.5.2-7	1M to 32M Density by 8 or 16 FEEPROM in PSOP	7	3.5.2-12
3.5.2-8	512K to 2048K X 8,-256K to 2048K X 16, Dual-Supply Flash EEPROM in 8X6 Grid Micro BGA Package	9	3.5.2-13
3.5.2-9	2048K and 8192K X 8, 1024K and 4096K X 16, Dual-Supply Flash EEPROM in 8X9 Grid Micro BGA Package	9	3.5.2-14
3.5.2-10	FEEPROM/SRAM Mixed Technology, Multi Chip Device.....	10,11	3.5.2-15-20
3.5.2-11	4M to 64M by 16 FEEPROM in TSOP1	11	3.5.2-21
3.5.2-12	32Mb to 1Gb Density by 16 FEEPROM in BGA	11	3.5.2-22

Figures (Cont'd)

Figure	Title	Release #	Page #
3.5.2-13	4MTO 16M by 16 FEEPROM with SDRAM Interface In TSOP2	11	3.5.2-23
3.5.2-14	4M to 16M by 16 FEEPROM with SDRAM Interface in FGBA	11	3.5.2-24
3.5.2-15	128Mb to 4Gb FEEPROM, user selectable as X8 or X16 in SSOP	11	3.5.2-25
3.5.2-16	Single-Supply 16Mb and 32Mb (x16/x32) FEEPROM in 80-Pin PQFP	12	3.5.2-26
3.5.2-17	128Mb to 1Gb (x8/x16) FEEPROM in 64-Ball LBGA	14	3.5.2-27
3.5.2-18	128Mb to 1Gb (x8/x16) FEEPROM in 64-Ball TFBGA	14	3.5.2-28
3.5.2-19	16Mb to 256Mb (x8/x16) FEEPROM in 56-Pin TSOP II	14	3.5.2-29
3.5.2-20	16Mb to 512Mb (x16) Synchronous 1.8V/3.0V FEEPROM in 56-Pin TSOP I	16	3.5.2-31
3.5.2-21	16Mb to 1Gb (x16) Synchronous 1.8V/3.0 VFEEPROM in 64-Ball LFBGA	16	3.5.2-28
3.6-1	.25K and 1K by 4 NVRAM in DIP	1	3.6-5
3.6-2	.5K and 1K by 8 NVRAM in DIP	1	3.6-6
3.6-3	.5K and 1K by 8 NVRAM in RCC	1	3.6-7
3.6-4	.5K to 16K by 8 NVRAM Family in DIP	1	3.6-8
3.6-5	.5K to 16K by 8 NVRAM Family in RCC.....	1	3.6-9
3.6-6	32K to 256K by 8 NVRAM Family in SOJ	1	3.6-10
3.6-7	32K to 256K NY 8 NVRAM Family in DIP	1	3.6-11
3.6-8	16K to 128K by 9 NVRAM Family in DIP	1	3.6-12
3.7-1	JTAG Addition to Revolutionary Pinout SRAM	4	3.7-3
3.7-2	State Diagram for Pipelined-Burst SRAM	7	3.7-4
3.7.1-1	0.25K and 1K by 1 TTL SRAM in DIP	1	3.7.1-5
3.7.1-2	0.25K and 1K by 1 TTL SRAM in SCC.....	1	3.7.1-6
3.7.1-3	4K to 2M by 1 TTL SRAM Family in DIP	1	3.7.1-7
3.7.1-4	16K by 1 TTL SRAM in RCC.....	1	3.7.1-8
3.7.1-5	64K by 1 TTL SRAM in RCC.....	1	3.7.1-9
3.7.1-6	16K to 2M by 1 TTL SRAM in SOJ and TSOP2	5	3.7.1-10
3.7.1-7	256K to 16M by 1 TTL SRAM and SSRAM Family in DIP, TSOP2, and SOJ	4	3.7.1-11
3.7.1-8	256K by 1 TTL SRAM in RCC.....	1	3.7.1-12
3.7.1-9	4M and 16M Configurable SRAM in DIP, TSOP2, and SOJ	4	3.7.1-13
3.7.2-1	1K to 256K by 1 ECL SRAM Family in DIP	1	3.7.2-5
3.7.2-2	256K to 16M by 1 ECL SRAM and SSRAM Family in DIP, TSOP2, and SOJ.	4	3.7.2-6
3.7.2-3	64K and 256K by 1 ECL SRAM in FP	2	3.7.2-7
3.7.2-4	256K to 16M by 1 ECL SSRAM Family in DIP, TSOP2, and SOJ	4	3.7.2-8
3.7.3-1	16 by 4 Inverting and Noninverting TTL SRAM in DIP	1	3.7.3-5
3.7.3-2	16 by 4 Inverting and Noninverting TTL SRAM in SCC	1	3.7.3-6
3.7.3-3	256 by 4 TTL SRAM in DIP	1	3.7.3-7
3.7.3-4	256 by 4 TTL SRAM in RCC	1	3.7.3-8
3.7.3-5	256 by 4 TTL SRAM in SCC	1	3.7.3-9
3.7.3-6	4K to 64K by 4 TTL SRAM Family WITHOUT G in DIP	1	3.7.3-10
3.7.3-7	4K by 4 TTL SRAM in RCC.....	1	3.7.3-11
3.7.3-8	4K to 256K by 4 TTL SRAM Family with G in DIP	1	3.7.3-12
3.7.3-9	16K to 256K by 4 TTL SRAM Family in RCC	1	3.7.3-13
3.7.3-10	16K and 64K by 4 TTL SRAM in RCC	1	3.7.3-14
3.7.3-11	4K to 1M by 4 TTL SRAM with and W/O G in SOJ and TSOP2	1	3.7.3-15

Figures (Cont'd)

Figure	Title	Release #	Page #
3.7.3-12	64K to 4M by 4 TTL SRAM Family in DIP, TSOP2, and SOJ	4	3.7.3-16
3.7.3-13	64K to 4M by 4 TTL SRAM Family with Separate Data I/O in DIP, TSOP2, and SOJ	4	3.7.3-17
3.7.3-14	64K to 4M by 4 Synchronous SRAM (SSRAM) Family in DIP, SOJ, and TSOP2	4	3.7.3-18
3.7.3-15	4K and 16K by 4 Cache Tag SRAM in DIP and SOJ	1	3.7.3-19
3.7.4-1	256 by 4, 100K ECL SRAM in DIP, 1K to 16K by 4, 10K and 100K ECL SRAM in DIP	1	3.7.4-5
3.7.4-2	256 and 1K by 4, 100K ECL SRAM in SFP	1	3.7.4-6
3.7.4-4	0.25K to 16K by 4, 10K and 100K ECL SRAM Family in DIP	1	3.7.4-7
3.7.4-5	16K by 4, 10K and 100K ECL SSRAM in DIP	1	3.7.4-8
3.7.4-6	64K to 4M by 4 ECL SRAM Family in DIP, SOJ, and TSOP2	4	3.7.4-9
3.7.4-7	64K to 4M by 4 ECL SRAM with Separate I/O Family in DIP, SOJ, and TSOP2	4	3.7.4-10
3.7.4-8	64K to 4M by 4 ECL SSRAM Family in DIP, SOJ, and TSOP2.....	4	3.7.4-11
3.7.4-9	64K by 4 ECL SRAM in FP	2	3.7.4-12
3.7.4-10	256K by 4 or 512K by 2 Configurable ECL SRAM in DIP and SOJ.....	2	3.7.4-13
3.7.4-11	64K to 4M by 4 Bit Selectable ECL SRAM Family in DIP, SOJ, and TSOP2	4	3.7.4-14
3.7.4-12	64K to 4M by 4 ECL SSRAM Family in DIP, SOJ, and TSOP2.....	4	3.7.4-15
3.7.4-13	64K to 4M by 4 Bit Selectable ECL SSRAM Family in DIP, SOJ, and TSOP2	4	3.7.4-16
3.7.5-1	64 by 9 SRAM in SCC	1	3.7.5-5
3.7.5-2	1K and 2K by 8 TTL SRAM in DIP.....	1	3.7.5-6
3.7.5-3	2K and 4K by 8 TTL SRAM in RCC.....	1	3.7.5-7
3.7.5-4	2K to 32K by 8 TTL SRAM Family in DIP and SOJ	1	3.7.5-8
3.7.5-5	0.5K to 32K by 8 TTL SRAM Family in RCC	1	3.7.5-9
3.7.5-6	32K to 512K by 8 TTL SRAM Family in SOJ	4	3.7.5-10
3.7.5-7	64K to 512K by 8 TTL SRAM Family in DIP	1	3.7.5-11
3.7.5-8	32K to 256K by 9 TTL SRAM Family in DIP	1	3.7.5-12
3.7.5-9	32K to 2M by 8 and 9 TTL SRAM Family in DIP, TSOP2, and SOJ.....	4	3.7.5-13
3.7.5-10	32K and 128K by 8 TTL SSRAM in DIP, TSOP2, and SOJ	4	3.7.5-14
3.7.5-11	2K to 32K by 9 DPSRAM Family in SCC	1	3.7.5-15
3.7.5-12	32K by 9 TTL Cache SRAM in SCC	2	3.7.5-16
3.7.5-13	128K by 8 TTL SRAM in TSOP1	2c9	3.7.5-17
3.7.5-14	128K by 8 and 9 TTL SSRAM in SOJ.....	2	3.7.5-18
3.7.5-15A	1K and 2K by 9 DPSRAM in DIP	2	3.7.5-19
3.7.5-15B	1K and 2K by 9 DPSRAM Truth Table	2	3.7.5-20
3.7.5-16	128K to 512K by 8 SRAM in CDSO-N	3	3.7.5-21
3.7.5-17	128K and 512K by 8 and 9 SSRAM and 128K by 9 SRAM in DIP, TSOP2, and SOJ	4	3.7.5-22
3.7.5-18	128K to 2M by 8/9 Burst SRAM in BGA	5	3.7.5-23
3.7.5-19	128K to 2M by 8/9 SSRAM BGA in BGA	5	3.7.5-24
3.7.5-20	128K to 2M by 8/9 SSRAM BGA Boundary Scan Order.....	5	3.7.5-25
3.7.5-21	32K by 8 SRAM in TSOP2.....	7	3.7.5-26
3.7.5-22	1Mb - 128Mb (x9) Sync Separate I/O SRAM in 209 BGA	12	3.7.5-27
3.7.5-23	1Mb - 128Mb (x9) Sync Separate I/O SRAM in 221 BGA	12	3.7.5-28
3.7.6-1	32K and 256K by 9 ECL SSRAM in SOJ, SOP, and FP	2	3.7.6-3
3.7.7-1	4K to 64K by 16 TTL SRAM Family in DIP	1	3.7.7-5

Figures (Cont'd)

Figure	Title	Release #	Page #
3.7.7-2	4K to 256K by 16 TTL SRAM Family in RCC	1	3.7.7-6
3.7.7-3	16K to 256K by 16 Address/Data MX SRAM Family in DIP	1	3.7.7-7
3.7.7-4	16K to 256K by 16 Address/Data MX SRAM Family in RCC	1	3.7.7-8
3.7.7-5	16K and 64K by 18 SRAM in SCC	1	3.7.7-9
3.7.7-6	64K by 16 and 18 SRAM in SOJ	3	3.7.7-10
3.7.7-7A	32K and 64K by 16 and 18 SRAM and SSRAM with Logic Features in SCC	4	3.7.7-11
3.7.7-7B	Write Clock Timing for SSRAM with Burst Mode	4	3.7.7-12
3.7.7-8	64K to 256K by 18 SRAM and SSRAM in TQFP	5,15	3.7.7-13
3.7.7-9	64K to 1M by 16/18 Burst SRAM BGA Padout	5,15	3.7.7-14
3.7.7-10	64K to 1M by 16/18 SSRAM BGA Padout	5,15	3.7.7-15
3.7.7-11	64K to 1M by 16/18 SSRAM BGA Boundary Scan Order	5c8,15	3.7.7-16
3.7.7-12	64K to 256K by 16/18 Burst SRAM in TQFP	6,15	3.7.7-17
3.7.7-13	256K and 1M by 16/18 SRAM in TSOP2	6	3.7.7-18
3.7.7-14	1Mb to 128Mb Density, by 16 or 18 Burst SRAM in 221 BGA	11a,16	3.7.7-19
3.7.7-15	1Mb to 128Mb Density, by 16 or 18 Sigma SRAM in 209 BGA	11a,15	3.7.7-20
3.7.7-16	1Mb to 128Mb Density, by 16 or 18 SIGMA SRAM in 221 BGA	11a,16	3.7.7-21
3.7.7-17	X18 SIGMA SRAM with Separate I/O in 209 BGA	12	3.7.7-22
3.7.7-18	X18 SIGMA SRAM with Separate I/O in 221 BGA	12,16	3.7.7-23
3.7.7-19	8Mb to 128Mb Density in X18 SRAM with Separate I/O in 165 BGA	12	3.7.7-24
3.7.7-20	2 Mb to 256 Mb Density in X16/18 Burst SRAM with Common I/O in 165 BGA	12,15	3.7.7-25
3.7.7-21	2 Mb to 256 Mb Density in X16/18 Network SRAM with Common I/O in 165 BGA	12,15	3.7.7-26
3.7.7-22	52-Pin TSOP II Pin Assignment for Low Power SRAMs	14	3.7.7-28
3.7.8-1	32K to 128K by 36 SSRAM with Burst in TQFP	6c9,15	3.7.8-5
3.7.8-2	32K to 128K by 36 SRAM and SSRAM in TQFP	5,15	3.7.8-6
3.7.7-3	32K to 512K by 32/36 Burst SRAM BGA Padout	5,15	3.7.8-7
3.7.7-4	32K to 512K by 32/36 SSRAM BGA Padout	5,15	3.7.8-8
3.7.7-5	32K to 512K by 32/36 SSRAM BGA Boundary Scan Order	5	3.7.8-9
3.7.8-6	16K to 36K by 32 and 64 SSRAM With Burst Counter in QFP	7	3.7.8-10
3.7.8-7	16K to 256K by 36 and 72 Burst SSRAM in BGA	7,16	3.7.8-11
3.7.8-8	1Mb to 128Mb Density, by 32 or 36 Burst SRAM in 221 BGA	11a,16	3.7.8-12
3.7.8-9	1Mb to 128Mb Density, by 32 or 36 SIGMA SRAM in 209 BGA	11a	3.7.8-13
3.7.8-10	1Mb to 128Mb Density, by 32 or 36 SIGMA SRAM in 221 BGA	11a,16	3.7.8-14
3.7.8-11	X36 SIGMA SRAM with Separate I/O in 209 BGA	12	3.7.8-15
3.7.8-12	X36 SIGMA SRAM with Separate I/O in 221 BGA	12,16	3.7.8-16
3.7.8-13	X36 SRAM with Separate I/O in 165 BGA	12	3.7.8-17
3.7.8-14	X36 DDR SRAM with Common I/O in 165 BGA	12	3.7.8-18
3.7.8-15	X32/36 Burst SRAM with Common I/O in 165 BGA	12,15	3.7.8-19
3.7.8-16	X32/36 NETWORK SRAM with Common I/O in 165 BGA	12,15	3.7.8-20
3.7.9-1	1Mb to 128Mb Density, by 64 or 72 Burst SRAM in 209 BGA	11a,16	3.7.9-3
3.7.9-2	1Mb to 128Mb Density, by 64 or 72 Burst SRAM in 221 BGA	11a,16	3.7.9-4
3.7.9-3	1Mb to 128Mb Density, by 64 or 72 Sigma SRAM in 209 BGA	11a	3.7.9-5
3.7.9-4	1Mb to 128Mb Density, by 64 or 72 Sigma SRAM in 221 BGA	11a,16	3.7.9-6
3.7.10-1	X8 B2 QUAD SRAM in 165 BGA	17	3.7.10-2
3.7.10-2	X8 B4 QUAD SRAM in 165 BGA	17	3.7.10-3
3.7.10-3	X8 B2 CIO DDR SRAM in 165 BGA	17	3.7.10-4

Figures (Cont'd)

Figure	Title	Release #	Page #
3.7.10-4	X8 B4 CIO DDR SRAM in 165 BGA	17	3.7.10-5
3.7.10-5	X8 B2 SIO DDR SRAM in 165 BGA	17	3.7.10-6
3.7.10-6	X9 B2 QUAD SRAM in 165 BGA	17	3.7.10-7
3.7.10-7	X9 B4 QUAD SRAM in 165 BGA	17	3.7.10-8
3.7.10-8	X9 B2 CIO DDR SRAM in 165 BGA	17	3.7.10-9
3.7.10-9	X9 B4 CIO DDR SRAM in 165 BGA	17	3.7.10-10
3.7.10-10	X9 B2 SIO DDR SRAM in 165 BGA	17	3.7.10-11
3.7.10-11	X18 B2 QUAD SRAM in 165 BGA	17	3.7.10-12
3.7.10-12	X18 B4 QUAD SRAM in 165 BGA	17	3.7.10-13
3.7.10-13	X18 B2 CIO DDR SRAM in 165 BGA	17	3.7.10-14
3.7.10-14	X18 B4 CIO DDR SRAM in 165 BGA	17	3.7.10-15
3.7.10-15	X18 B2 SIO DDR SRAM in 165 BGA	17	3.7.10-16
3.7.10-16	X36 B2 QUAD SRAM in 165 BGA	17	3.7.10-17
3.7.10-17	X36 B4 QUAD SRAM in 165 BGA	17	3.7.10-18
3.7.10-18	X36 B2 CIO DDR SRAM in 165 BGA	17	3.7.10-19
3.7.10-19	X9 B4 CIO DDR SRAM in 165 BGA	17	3.7.10-20
3.7.10-20	X36 B2 SIO DDR SRAM in 165 BGA	17	3.7.10-21
3.8-1	2K to 8K by 8 PSRAM Family in DIP	1	3.8-5
3.8-2	2K to 16K by 8 PSRAM Family in RCC	1	3.8-6
3.8-3	32K to 512K by 8 PSRAM Family in SOJ	1	3.8-7
3.8-4	4K to 32K by 16 PSRAM Family in DIP	1	3.8-8
3.8-5	4K to 256K by 16 PSRAM Family in SCC	1	3.8-9
3.8-6	8M to 64M Burst PSRAM in BGA	15	3.8-10
3.8-7	16Mb though 512Mb PSRAM in 6x8mm and 8x10mm 54-ball VFBGA	16	3.8-11
3.9.1-1	16K by 1 DRAM in DIP with 3 Supply Voltages, 16K to 256K by 1 DRAM Family in DIP	1	3.9.1-5
3.9.1-2	16K to 256K by 1 DRAM in RCC	1	3.9.1-6
3.9.1-3	64K and 256K by 1 DRAM in ZIP	1	3.9.1-7
3.9.1-4	1M to 64M by 1 DRAM Family in DIP	1	3.9.1-8
3.9.1-5	1M to 16M by 1 DRAM Family in SOJ and TSOP2	4	3.9.1-9
3.9.1-6	1M to 16M by 1 DRAM Family in ZIP	4	3.9.1-10
3.9.1-7	1M to 16M by 1 NON-MUX DRAM Family in SOJ	2	3.9.1-11
3.9.1-8	1M by 1 DRAM in TSOP1	2	3.9.1-12
3.9.1-9	16M X 1/4M X 4 Configurable DRAM in SOJ	2	3.9.1-13
3.9.1-10	64M by 1 DRAM in SOJ and TSOP2	4a	3.9.1-14
3.9.1-11	2 X 16M by 1 DRAM in TSOP2	4	3.9.1-15
3.9.1-12	64M by 1 DRAM in SOJ and TSOP2	5,7	3.9.1-16
3.9.1-13	16M by 1 DRAM in USON	9	3.9.1-17
3.9.2-1	16K and 64K by 4 DRAM in DIP	1	3.9.2-5
3.9.2-2	16K and 64K by 4 DRAM in RCC	1	3.9.2-6
3.9.2-3	256K and 1M by 4 DRAM Family in DIP	1	3.9.2-7
3.9.2-4	256K to 4M by 4 DRAM in SOJ and TSOP2	4	3.9.2-8
3.9.2-5	64K to 4M by 4 DRAM in ZIP	1	3.9.2-9
3.9.2-6	256K and 1M by 4 DRAM with 4 CE in SOJ and TSOP2	6	3.9.2-10
3.9.2-7	256K by 4 DRAM in TSOP1	2	3.9.2-11
3.9.2-8	4M by 4/16M by 1 Configurable DRAM in SOJ	2	3.9.2-12

Figures (Cont'd)

Figure	Title	Release #	Page #
3.9.2-9	256K to 4M by 4 Non-Mux DRAM in SOJ	2	3.9.2-13
3.9.2-10	4M by 4 DRAM with 4 CE in SOJ and TSOP2	6	3.9.2-14
3.9.2-11	16M by 4 DRAM in SOJ and TSOP2	4a	3.9.2-15
3.9.2-12	1M, 2M, 4M by 2 DRAM with 2 CE in SOJ and TSOP2	4,7	3.9.2-16
3.9.2-13	16M by 4 DRAM in SOJ and TSOP2	5,7	3.9.2-17
3.9.2-14	16M by 4 DRAM with 4 CAS in SOJ and TSOP2	6,7	3.9.2-18
3.9.2-15	64M by 4 DRAM in TSOP2 Pin Rotation	6	3.9.2-19
3.9.2-16	4M by 4 DRAM in USON.....	9	3.9.2-20
3.9.2-17	16M by 4 DRAM in USON.....	9	3.9.2-21
3.9.3-1	32K by 8 DRAM in DIP.....	1	3.9.3-5
3.9.3-2	32K by 8 DRAM in RCC	1	3.9.3-6
3.9.3-3	512K by 8 and 9 DRAM in SOJ.....	2	3.9.3-7
3.9.3-4	512K by 8 and 9 DRAM in ZIP	2	3.9.3-8
3.9.3-5	512K by 8 and 9 Non-Mux DRAM in SOJ	2	3.9.3-9
3.9.3-6	2M by 8 and 9 DRAM in SOJ and TSOP2	5	3.9.3-10
3.9.3-7	8M by 8 and 9 DRAM in SOJ and TSOP2	4a	3.9.3-11
3.9.3-8	8M by 8 DRAM in SOJ and TSOP2	5,7	3.9.3-12
3.9.3-9	32M by 8 DRAM in TSOP2 Pin Rotation	6	3.9.3-13
3.9.3-10	4M and 8M by 8 DRAM in SOP.....	8	3.9.3-14
3.9.3-11	2M by 8 DRAM in USON.....	9	3.9.3-15
3.9.3-12	8M by 8 DRAM in USON.....	9	3.9.3-16
3.9.4-1	64K by 16 DRAM in SOJ.....	1	3.9.4-5
3.9.4-2	256K by 16 and 18 DRAM with 2 W or 2 CE in SOJ	2	3.9.4-6
3.9.4-3	256K by 16 and 18 DRAM with 2 W or 2 CE in TSOP2	4	3.9.4-7
3.9.4-4	1M by 16 and 18 DRAM with 2 CE in SOJ	5	3.9.4-8
3.9.4-5	1M by 16 and 18 DRAM with 2 CE in TSOP2	5	3.9.4-9
3.9.4-6	64K by 16 DRAM with 2 W in TSOP2	3	3.9.4-10
3.9.4-7A	256K by 16 DRAM with Extended Functions in DIP and SOJ.....	4	3.9.4-11
3.9.4-7B	256K by 16 DRAM Mandatory Extended FUNCTION Truth Table	4	3.9.4-12
3.9.4-8	2M by 16, 4M by 16 and 18 DRAM in TSOP2.....	6,7	3.9.4-13
3.9.4-9	128K and 256K by 16 Burst DRAM in SOJ	6	3.9.4-14
3.9.4-10	128K and 256K by 16 Burst DRAM in TSOP2	6	3.9.4-15
3.9.4-11	128K and 256K by 16 Burst DRAM in ZIP	6	3.9.4-16
3.9.4-12	16M by 16 DRAM in TSOP2 Pin Rotation	6	3.9.4-17
3.9.4-13	128K and 256K by 32 DRAM with 4 CAS in SSOP	8	3.9.4-18
3.9.4-14	512K and 2M by 32 and 36 DRAM in SOJ and TSOP2	6,10	3.9.4-19
3.9.4-15	8M by 32 DRAM in TSOP2 Pin Rotation	9	3.9.4-20
3.9.4-16	2M by 32 DRAM in TSOP2	7	3.9.4-21
3.9.4-17	256K by 32 DRAM in QFP	8	3.9.4-22
3.9.4-18	1M by 16 DRAM in USON.....	9	3.9.4-23
3.9.4-19	4M by 16 DRAM in USON.....	9	3.9.4-24
3.9.5-1A	DRAM On-Chip Refresh Timing	1	3.9.5-5
3.9.5-1B	DRAM Self Refresh Mode Timing	4	3.9.5-5
3.10.1-1	64K by 4 MPDRAM in DIP and SOJ	1	3.10.1-2
3.10.1-2	64K by 4 MPDRAM in ZIP.....	1	3.10.1-3
3.10.1-3	256K by 4 MPDRAM in DIP, SOJ, and TSOP2	3	3.10.1-4
3.10.1-4	256K by 4 MPDRAM in ZIP.....	1	3.10.1-5

Figures (Cont'd)

Figure	Title	Release #	Page #
3.10.1-5	256K by 4 TPDRAM in SOJ.....	2.....	3.10.1-6
3.10.2-1	128K and 256K by 8 MPDRAM in DIP and SOJ	2.....	3.10.2-2
3.10.2-2	128K by 8 MPDRAM in TSOP2	3.....	3.10.2-3
3.10.3-1	128K and 256K by 16 MPDRAM in SOG with 2 W and 2 CE	3.....	3.10.3-3
3.10.3-2	128K and 256K by 16 MPDRAM in TSOP2 with 2 W and 2 CE	5.....	3.10.3-4
3.10.3-3	256K by 16 SGRAM in TSOP2.....	6.....	3.10.3-5
3.10.3-4	128K, 256K, and 512K by 32 SGRAM, 2 and 4 Bank in QFP/TQFP.....	6c7,9,10	3.10.3-6
3.10.3-5	256K by 32 SGRAM in TSOP2.....	6.....	3.10.3-7
3.10.3-6	256K by 32 Synchronous MPDRAM in QFP/TQFP	6.....	3.10.3-8
3.10.3-7	256K by 32 MPDRAM in QFP/TQFP	7.....	3.10.3-9
3.10.3-8	128K, 256K, and 512K by 32 X 4 Bank DDR SGRAM in LQFP	9,10.....	3.10.3-10
3.10.3-9	4M X 32 (4 Bank) DDR SGRAM in 144 Ball FBGA	11.....	3.10.3-11
3.10.3-10	8M X 32 GDDR3 Graphics RAM in 144-Ball FBGA	13.....	3.10.3-12
3.10.4-1	Bit Write Timing.....	1.....	3.10.4-7
3.10.4-2	Split Register with Programmable STOPS	2.....	3.10.4-9
3.10.4-3A	Pipelined Fast Page Mode.....	2.....	3.10.4-10
3.10.4-3B	Pipelined Fast Page Mode.....	2.....	3.10.4-11
3.10.4-4	MPDRAM Extended Data Out Fast Page Mode	4.....	3.10.4-12
3.10.4-5A,B	SAM Length Definition for 4M MPDRAM.....	5.....	3.10.4-13, 14
3.10.4-6	Synchronous GRAM Special Mode Set Procedure	6.....	3.10.4-15
3.10.4-7	Synchronous MPDRAM Special Mode Set Procedure	6.....	3.10.4-16
3.11.2-1	4M X 4 SDRAM in TSOP2.....	6,7.....	3.11.2-5
3.11.2-2	16M X 4 SDRAM in TSOP2.....	6.....	3.11.2-6
3.11.2-3	64M X 4 SDRAM in TSOP2 Pin Rotation	7,9.....	3.11.2-7
3.11.2-4	16M, 32M, 64M, and 128M X 4 DDR SDRAM in TSOP2	8,9,10,11,12.....	3.11.2-8
3.11.2-5	32M, 64M, and 128M X 4 SDRAM in TSOP2	8,9,10,11,12.....	3.11.2-9
3.11.2-6	16M X 4 VC SDRAM in TSOP2.....	9.....	3.11.2-10
3.11.2-7	16M, 32M, and 64M by 4 Stackable SDR SDRAM in LSOJ	9.....	3.11.2-11
3.11.2-8	16M, 32M, and 64M by 4 VC DDR SDRAM in TSOP2.....	9c10,11,12	3.11.2-12
3.11.2-9	16M, 32M, 64M and 128M by 4 Stackable DDR SDRAM in LSOJ.....	9,10,11,12	3.11.2-13
3.11.2-10	16M by 4 SDRAM in USON.....	9.....	3.11.2-14
3.11.2-11	16M, 32M, and 64M by 4 SDR SDRAM in TSOP2.....	9,12.....	3.11.2-15
3.11.2-12	16M and 32M by 4 SDR SDRAM in LFBGA	9.....	3.11.2-16
3.11.2-13	16M and 32M by 4 DDR SDRAM in LFBGA	9.....	3.11.2-17
3.11.2-14	16M, 32M, and 64M by 4 SDR SDRAM in LFBGA	9c10.....	3.11.2-18
3.11.2-15	16M, 32M, and 64M by 4 DDR SDRAM in LFBGA	9c10,11	3.11.2-19
3.11.2-16	64M, and 128M by 4 SDR SDRAM in FBGA	11a.....	3.11.2-20
3.11.2-17	32M, 64M, 128M, and 256M by 4 DDR SDRAM in FBGA	11a.....	3.11.2-21
3.11.2-18	32M, 64M, 128M, and 256M by 4 DDR SDRAM in 60-Ball FBGA with Optional Support Balls	12.....	3.11.2-22
3.11.2-19	64M, 128M, 256M, 512M, and 1G by 4 DDR2 SDRAM in 60-Ball TF-FBGA	12,13.....	3.11.2-23
3.11.2-20	16M, 32M, 64M, and 128M X 4 SDRAM in sTSOP	12.....	3.11.2-24
3.11.2-21	64M, 128M, 256M, 512M, and 1G by 4 X 2 DDR2 SDRAM in 60-Ball Stacked FBGA	13.....	3.11.2-25
3.11.2-22	64M, 128M, 256M, 512M, and 1G by 4 X 2 DDR2 SDRAM for 60-Ball Stacked FBGA Requiring Support Balls	13.....	3.11.2-26
3.11.3-1	2M by 8 or 9 SDRAM in TSOP2	6,7.....	3.11.3-5

Figures (Cont'd)

Figure	Title	Release #	Page #
3.11.3-2	8M by 8 SDRAM in TSOP2	6	3.11.3-6
3.11.3-3	32M by 8 SDRAM in TSOP2 Pin Rotation	7,9	3.11.3-7
3.11.3-4	8M, 16M, 32M, 64M, and 128M by 8 DDR SDRAM in TSOP2	8,9,10,11,12	3.11.3-8
3.11.3-5	16M, 32M, 64M, and 128M by 8 SDRAM in TSOP2	8,9,10,12	3.11.3-9
3.11.3-6	8M, 16M, and 32M by 8 SDR SDRAM in TSOP2	9	3.11.3-10
3.11.3-7	8M, 16M, and 32M by 8 Stackable SDR SDRAM in LSOJ	9	3.11.3-11
3.11.3-8	8M, 16M, 32M, 64M and 128M by 8 Stackable DDR SDRAM in LSOJ	9,10,11,12	3.11.3-12
3.11.3-9	2M by 8 SDRAM in USON	9	3.11.3-13
3.11.3-10	8M by 8 SDRAM in USON	9	3.11.3-14
3.11.3-11	8M X 8 VC SDRAM in TSOP2	9	3.11.3-15
3.11.3-12	8M, 16M, and 32M by 8 VC DDR SDRAM in TSOP2	9c10,11	3.11.3-16
3.11.3-13	8M and 16M by 8 SDR SDRAM in LFBGA	9	3.11.3-17
3.11.3-14	8M and 16M by 8 DDR SDRAM in LFBGA	9	3.11.3-18
3.11.3-15	8M, 16M, and 32M by 8 SDR SDRAM in LFBGA	9c10	3.11.3-19
3.11.3-16	8M, 16M, 32M, and 64M by 8 DDR SDRAM in LFBGA	9c10,11	3.11.3-20
3.11.3-17	16M, 32M and 64M by 8 SDR SDRAM in FBGA	11a	3.11.3-21
3.11.3-18	32M and 64M by 8 SDR SDRAM in FBGA	11a	3.11.3-22
3.11.3-19	16M, 32M, 64M, and 128M by 8 DDR SDRAM in FBGA	11a	3.11.3-23
3.11.3-20	16M, 32M, 64M, and 128M by 8 DDR SDRAM in 60-Ball FBGA with Optional Support Balls	12	3.11.3-24
3.11.3-21	32M, 64M, 128M, 256M, and 512M by 8 DDR2 SDRAM in 60-Ball TF-FBGA	12,13	3.11.3-25
3.11.3-22	8M, 16M, 32M, and 64M X 8 SDRAM in sTSOP	12	3.11.3-26
3.11.3-23	32M, 64M, 256M, 128M, and 512M by 8 X 2 DDR2 SDRAM in 60-Ball Stacked FBGA	13	3.11.3-27
3.11.3-24	32M, 64M, 128M, 256M, and 512M by 8 X 2 DDR2 SDRAM for 60-Ball Stacked FBGA Requiring Support Balls	13	3.11.3-28
3.11.4-1	256 by 16 and 1M by 16/18 SDRAM in TSOP2	6,7	3.11.4-8
3.11.4-2	4M by 16 SDRAM in TSOP2	6,7	3.11.4-9
3.11.4-3	16M by 16 SDRAM in TSOP2	6c7,9	3.11.4-10
3.11.4-4	128K, 256K and 512K by 32 SDRAM in QFP/TQFP	6c7,9,10	3.11.4-11
3.11.4-5	2M by 32 SDRAM in TSOP2	6,7,10	3.11.4-12
3.11.4-6	8M by 32 SDRAM in TSOP2 Pin Rotation	6c7,9	3.11.4-13
3.11.4-7	2M by 32 and 36, 4M and 8M by 32 SDRAM in TSOP2	7,8,10,12	3.11.4-14
3.11.4-8	4M, 8M, 16M, 32M, and 64M by 16 DDR SDRAM in TSOP2	8,9,10,11,12	3.11.4-15
3.11.4-9	8M, 16M, 32M, and 64M by 16 SDRAM in TSOP2	8,9,10,12	3.11.4-16
3.11.4-10	4M, 8M, and 16M by 16 SDR SDRAM in TSOP2	9	3.11.4-17
3.11.4-11	4M, 8M, and 16M by 16 SDR Stackable SDRAM in LSOJ	9	3.11.4-18
3.11.4-12	4M, 8M, 16M, and 32M by 16 Stackable DDR SDRAM in LSOJ	9,10,11,12	3.11.4-19
3.11.4-13	4M by 16 SDRAM in USON	9	3.11.4-20
3.11.4-14	4M X 16 VC SDRAM in TSOP2	9	3.11.4-21
3.11.4-15	4M, 8M, and 16M by 16 VC DDR SDRAM in TSOP2	9c10,11	3.11.4-22
3.11.4-16	4M and 16M by 16 SDR SDRAM in LFBGA	9,12	3.11.4-23
3.11.4-17	4M and 16M by 16 DDR SDRAM in LFBGA	9	3.11.4-24
3.11.4-18	4M, 8M, and 16M by 16 SDR SDRAM in LFBGA	9c10	3.11.4-25
3.11.4-19	8M, 16M, and 32M by 16 DDR SDRAM in LFBGA	9c10,11	3.11.4-26
3.11.4-20	4M to 64M by 16 and 18 SLDRAM in R-PZIP	9	3.11.4-27

Figures (Cont'd)

Figure	Title	Release #	Page #
3.11.4-21	4M by 16/18 SLRAM in TSOP2	9.....	3.11.4-28
3.11.4-22	128K, 256K, and 512K X 32 X 4 Bank DDR SDRAM in QFP	9,10,11	3.11.4-29
3.11.4-23	2M, 4M, and 8M by 32 DDR SDRAM in FBGA	11a.....	3.11.4-30
3.11.4-24	8M, 16M, 32M, and 64M by 16 SDR SDRAM in FBGA	11a,12.....	3.11.4-31
3.11.4-25	16M and 32M by 16 SDR SDRAM in FBGA	11a.....	3.11.4-32
3.11.4-26	8M, 16M, 32M, and 64M by 16 DDR SDRAM in FBGA	11a.....	3.11.4-33
3.11.4-27	2M and 4M by 32 SDR SDRAM in LFBGA	11a.....	3.11.4-34
3.11.4-28	2M, 4M, 8M, and 16M by 32, Low Power SDR SDRAM in LFBGA	11a,12,13	3.11.4-35
3.11.4-29	8M, 16M, 32M, and 64M by 16 DDR SDRAM in 60-Ball FBGA with Optional Support Balls	12.....	3.11.4-36
3.11.4-30	16M, 32M, 64M, 128M, and 256M by 16 DDR2 SDRAM in 60-Ball TFBGA	12,13	3.11.4-37
3.11.4-31	4M, 8M, 16M, and 32M X 16 SDRAM in sTSOP	12.....	3.11.4-38
3.11.4-32	16M, 32M, 64M, 128M, and 256M by 16 X 2 DDR2 SDRAM in Stacked FBGA	13.....	3.11.4-39
3.11.4-33	16M, 32M, 64M, 128M, and 256M by 16 X 2 DDR2 SDRAM for Stacked FBGA Packages Requiring Support Balls	13.....	3.11.4-40
3.11.4-34	4M x 32M DDR2 SDRAM in 144-Ball LF-XBGA	13.....	3.11.4-41
3.11.4-35	8M x 16 DDR SDRAM in 78-Ball TF-BGA	14.....	3.11.4-42
3.11.4-36	8M, 16M, and 32M x 32 Low Power DDR SDRAM in 90-Ball FBGA.....	14,15	3.11.4-43
3.11.4-37	256M, 2G x 32w DDR2 SDRAM in 128-Ball BGA	17.....	3.11.4-44
4.2-1	22, 24, and 30 Pin DRAM Modules.....	4-7.....	4.2-3
4.2-2	30 Pin DRAM Module Family.....	1-7.....	4.2-4
4.2-3	23/25/26/28 Pin DRAM Module Family	1-7.....	4.2-5
4.2-4	2 X 64K to 1M by 4, 60 Pin SRAM Module Family	1-7.....	4.2-6
4.2-5	64K to 1M by 9, 70 Pin SRAM Module Family	1-7.....	4.2-7
4.3-1	2 X 64K to 1M by 9, 76 Pin SRAM Module Family	1-7.....	4.3-3
4.3-2	40 Pin DRAM Module Family.....	1-7.....	4.3-4
4.3-3A	60 Pin DRAM Card Family Pin Connections	2-7.....	4.3-5
4.3-3B	60 Pin CARD Family Block Diagrams	2-7.....	4.3-6
4.3-4A	68 Pin Multiple Technology Card Family	3-7.....	4.3-7
4.3-4B	68 Pin Multiple Technology Card Family Function Truth Tables	3-7.....	4.3-8
4.4.1-1	16K to 4M by 32, 64 and 72 Pin SRAM Module Family	6-7.....	4.4.1-2
4.4.2-2A	256K to 256M by 36. 72 Pin DRAM Module Pinout	6-7c8.....	4.4.2-3
4.4.2-2B-K	72 Pin 36 Bit DRAM SIMM Block Diagrams	6-7.....	4.4.2-4-13
4.4.2-3A	256K to 256M by 32, 36, and 40-Bit 72 Pin DRAM Module.....	6-7.....	4.4.2-14
4.4.2-3B-C	72 Pin 32, 36, and 40-Bit DRAM SIMM Block Diagrams	6-7.....	4.4.2-15-16
4.4.3-1A	256K to 128M by 36, 88 Pin DRAM Card Family	6-7.....	4.4.3-3
4.4.3-1B	256K to 128M by 36, 88 Pin DRAM Card Family Configuration Tables	6-7.....	4.4.3-4
4.4.3-1C	256K to 128M by 36, 88 Pin DRAM Card Family Block Diagram	6-7.....	4.4.3-5
4.4.3-1D	256K to 128M by 36, 88 Pin DRAM Card Family Block Diagram	6-7.....	4.4.3-6
4.4.3-1E	256K to 128M by 36, 88 Pin DRAM Card Family Block Diagram	6-7.....	4.4.3-7
4.4.3-1F	256K to 128M by 36, 88 Pin DRAM Card Family Block Diagram	6-7.....	4.4.3-8
4.4.3-2A	256K to 128M by 40 DRAM C	4-7.....	4.4.3-9
4.4.3-2B	256K to 128M by 40 DRAM Card PD Truth Table	4-7.....	4.4.3-10
4.4.3-2C	256K to 64M by 40 DRAM Card Using by 4 Devices	4-7.....	4.4.3-11
4.4.3-2D	512K to 128M by 40 DRAM Card Using by 4 Devices	4-7.....	4.4.3-12

Figures (Cont'd)

Figure	Title	Release #	Page #
4.4.3-2E	512K to 32M by 40 DRAM Card Using by 8 Devices	4-7	4.4.3-13
4.4.3-2F	1M to 64M by 40 DRAM Card Using by 8 Devices	4-7	4.4.3-14
4.4.4A	32 and 36 Bit 72 Pin DRAM SO-DIMM Pinout, Presence Detect and Configuration Tables	6-7	4.4.4-1
4.4.4B-D	32 and 36 Bit DRAM SO-DIMM Block Diagrams	5-7	4.4.4-2-5
4.4.5A	88 Pin 32 and 36 Bit DRAM SO-DIMM Pinout	6-7	4.4.5-2
4.4.5B	88 Pin 32 and 36 Bit DRAM SO-DIMM PD Truth Tables	6-7	4.4.5-3
4.4.5C-F	88 Pin 32 and 36 Bit DRAM SO-DIMM Block Diagrams	6-7	4.4.5-4⇒7
4.4.6A	112 Pin 32 Bit MPDRAM DIMM Pinout	6-7	4.4.6-2
4.4.6B-C	112 Pin 32 Bit MPDRAM DIMM PD Truth Tables and Block Diagrams	6-7	4.4.6-3, 4
4.4.7A	128K to 8M by 32 EEPROM SIMM, Pinout and PD Tables	4-7	4.4.7-3
4.4.7B	128K to 8M by 32 EEPROM SIMM Block Diagram	4-7	4.4.7-4
4.4.8B-C	32, 36, or 40 Bit 100 Pin Module Pinout	7c8	4.4.8-3, 4
4.4.8D	32, 36, or 40 Bit 100 Pin Module Pin Comparison	7	4.4.8-5
4.4.8E	32, 36, or 40 Bit 100 Pin Module Clock Wiring	7c8	4.4.8-6
4.4.8F-AE	32,36, or 40 Bit 100 Pin Module Block Diagrams	7c8	4.4.8-7⇒32
4.5.1A-B	64, 72, or 80 Bit SIMM Pinout, TOP and Bottom Halves.....	4-7,9	4.5.1-2,3
4.5.1C	64, 72, or 80 Bit SIMM Presence Detect and Configuration Tables	6-7	4.5.1-4
4.5.1D	64, 72, and 80 Bit DRAM SIMM Capacity Table	4-7	4.5.1-5
4.5.1E-AB	64, 72, and 80 Bit Configuration Block Diagrams	4-c7c8	4.5.1-6-29
4.5.2A-B	Pin Assignments, 200 Pin, 8-Byte SDRAM DIMM	5-7,8,11	4.5.2-3,4
4.5.2C	8-Byte SDRAM DIMM Presence Detect and Configuration Tables	5-7	4.5.2-5
4.5.2D-E	8-Byte SDRAM DIMM Mechanical Key and Pin Definitions	5-7	4.5.2-6
4.5.2F-K	8-Byte Buffered SDRAM DIMM Block Diagrams	5-7	4.5.2-7-12
4.5.2L-M	8-Byte Unbuffered SDRAM DIMM Block Diagrams	5-7	4.5.2-13-14
4.5.3A-B	Pin Assignments, 8-Byte Unbuffered DRAM DIMM	5-7,9	4.5.3-2,3
4.5.3D	8-Byte DRAM DIMM Mechanical Key and Pin Definitions	5-7	4.5.3-5
4.5.3E	Pinout comparison, 168 Pin DRAM and SDRAM DIMM	5-7c8	4.5.3-6
4.5.3F	8-Byte Unbuffered DRAM DIMM SPD Assignments	5-7,8-1	4.5.3-7
4.5.3G-U	8-Byte Unbuffered DRAM DIMM Block Diagrams	5-7,8	4.5.3-8-20
4.5.4A-B	Pin Assignment, 8-Byte Unbuffered SDRAM DIMM.....	5-7,9	4.5.4-2,3
4.5.4C	8-Byte Unbuffered SDRAM DIMM SPD Assignments	5-7,8	4.5.4-4
4.5.4D	Comparison of 168 Pin Buffered and Unbuffered DRAM and SDRAM DIMM	7	4.5.4-5
4.5.4E	8-Byte SDRAM DIMM Mechanical Key and Pin Definitions	5-7,8	4.5.4-6
4.5.4G-H	Clock Layout, Unbuffered SDRAM/DRAM DIMM.....	7,8	4.5.4-8,9
4.5.4I-AK	8-Byte SDRAM DIMM Block Diagrams	5-7,8,9	4.5.4-10-38
4.5.5A-B	Pin Assignment, 8-Byte DRAM SO-DIMM	5-7,9	4.5.5-2,3
4.5.5C	Keying Methodology, 8-Byte DRAM SO-DIMM.....	5-7	4.5.5-4
4.5.5D	Comparison of 144 Pin DRAM/SDRAM SO-DIMM	7	4.5.5-5
4.5.5E	8-Byte DRAM SO-DIMM Serial Presence Detect Table.....	5-7	4.5.5-6
4.5.5F-AB	8-Byte DRAM SO-DIMM Block Diagrams	5-7,8	4.5.5-7-16
4.5.6A-B	Pin Assignment, 8 Byte SDRAM SO-DIMM	5-7,9	4.5.6-2,3
4.5.6C	8-Byte SDRAM SO-DIMM Presence Detect Information	5-7	4.5.6-4
4.5.6D	8-Byte SDRAM DIMM Mechanical Key and Pin Definitions	5-7	4.5.6-5
4.5.6E	Comparison of 144 Pin DRAM/SDRAM SO-DIMM	7	4.5.6-6
4.5.6F	Clock Layout, SDRAM SO-DIMM.....	7	4.5.6-7

Figures (Cont'd)

Figure	Title	Release #	Page #
4.5.6G-P	8-Byte Registered SDRAM DIMM Block Diagrams	5-7	4.5.6-8-17
4.5.7A-B	Pin Assignment, 8-Byte Registered SDRAM DIMM.....	8,9	4.5.7-2,3
4.5.7C	8-Byte Registered SDRAM DIMM SPD Assignments.....	8	4.5.7-4
4.5.7D	Keying Methodology, 8-Byte Registered SDRAM DIMM	8	4.5.7-5
4.5.7E	Comparison of 168 Pin Unbuffered DRAM/Registered SDRAM DIMM	9	4.5.7-6
4.5.7F	Register Loading, Unbuffered SDRAM DIMM	8	4.5.7-7
4.5.7G-H	Clock Layout, Registered SDRAM DIMM	8	4.5.7-7-8
4.5.7I-X	8-Byte Registered SDRAM DIMM Block Diagrams	8c9,10,11	4.5.7-9-24
4.5.8A-B	Pin Assignments, 8-Byte SGRAM SO-DIMM.....	8,9,10	4.5.8-2,3
4.5.8C	8-Byte SGRAM/SDRAM SO-DIMM Output Measurement.....	8	4.5.8-4
4.5.8D-F	8-Byte SGRAM/SDRAM SO-DIMM Layout Considerations	8	4.5.8-5-9
4.5.8G-J	8-Byte SGRAM/SDRAM SO-DIMM Block Diagrams	8,10	4.5.8-10-13
4.5.9A-B	Pin Assignments, DDR SGRAM SO-DIMM	9	4.5.9-2, 3
4.5.9C	Clock Net Routing, DDR SGRAM SO-DIMM	9	4.5.9-6
4.5.9D-G	Block Diagrams, DDR SGRAM SO-DIMM.....	9	4.5.9-7-10
4.5.10A-B	Pin Assignments, DDR SDRAM, Top Half and Bottom Half	9,12	4.5.10-2,3
4.5.10C	Summary of Features and Pin Description, DDR SDRAM	9	4.5.10-4
4.5.10D	SPD Table and Information, DDR SDRAM.....	9	4.5.10-5
4.5.10E	Comparison of 184 Pin Unbuffered SDR SDRAM and DDR SDRAM DIMM	9	4.5.10-6
4.5.10F	Keying Methodology, DDR SDRAM.....	9	4.5.10-7
4.5.10G-H	VDDID Definition, DDR SDRAM	9	4.5.10-8, 9
4.5.10I-P	Configuration Block Diagram, DDR SDRAM	9	4.5.10-10-17
4.5.11A-B	Pin Assignments, SDR SDRAM, Top Half and Bottom Half	10	4.5.11-2, 3
4.5.11C	Summary of Features and Pin Description, SDR SDRAM.....	10	4.5.11-4
4.5.11D	SPD Table and Information, SDR SDRAM.....	10	4.5.11-5
4.5.11E	Comparison of 184 Pin Unbuffered SDR SDRAM and DDR SDRAM DIMM	10	4.5.11-6
4.5.11F	Keying Methodology, SDR SDRAM.....	10	4.5.11-7
4.5.11G-H	VDDID Definition, SDR SDRAM	10	4.5.11-8,9
4.5.11I-J	Clock Layout, SDR SDRAM.....	10	4.5.11-10-11
4.5.11K	FET Switch Structure, SDR SDRAM	10	4.5.11-12
4.5.11L-U	Configuration Block Diagram, SDR Unbuffered SDRAM.....	10	4.5.11-13-23
4.5.12A-Q	Configuration Block Diagram, SDR Registered SDRAM	10	4.5.12-3-19
4.5.12R	184 Pin DDR Registered DIMM Clock Network.....	10	4.5.12-21
4.5.12Sa-Sb	Clock Layout, DDR Unbuffered DIMM	10	4.5.12-22-23
4.5.12Ta-Tb	184 Pin DDR Registered SDRAM DIMM Pin Assignments	1	4.5.12-24-26
4.5.14A-B	Pin Assignments, DDR2 SDRAM, Top Half and Bottom Half	12	4.5.14-2,3
4.5.14C	Pin Description, DDR2 SDRAM	12	4.5.14-4
4.5.14D	Pin Summary, DDR2 SDRAM.....	12	4.5.14-5
4.6.1A-C	144 Bit SIMM Pinout, Top, Middle, and Bottom Parts	7c8	4.6.1-2,3,4
4.6.1D	144 Bit SIMM Presence Detect and Configuration Tables	7	4.6.1-5
4.6.1E-F	144 Bit SDRAM DIMM Mechanical Key and Pin Definitions.....	5-7	4.6.1-6
4.6.1G-H	144 Bit SDRAM Configuration Block Diagrams	7	4.6.1-7
5-1	20 Pin DIP to 20 Terminal CC PLD Conversion	1	5-3
5-2	24 and 28 Pin DIP to 27 Terminal CC Conversion	2	5-4
5-3	Power Pin Placement for ECL PLD	1	5-5

5-4	40 Pin DIP PLD Power Pin Placement.....	1	5-6
5-5	44 Terminal CC Power Pin Placement	1	5-7
5-6	48 and 64 Pin DIP ASIC Power Pin Placement	1	5-8
5-7	52, 68, and 84 Terminal CC ASIC Power Pin Placement	1	5-9
5-8A	PLD Standard Loads, Definitions	5	5-11
5-8B	PLD Standard Load Circuit.....	5	5-12
5-8C	PLD Output Load Calculations	5	5-13
5-8D	PLD AC Load Lines.....	5	5-14
5-9	24 Pin PLD Functions in 28 Pin DIP and SCC	3	5-15
5-10	132 Pin PQFP Power Pin Locations.....	3	5-16
5-11	High Speed Pinout for 20 Pin PLD Functions	4	5-17