

4.20.21 - 204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM
72b-S0-DIMM Design Specification

DDR3 SDRAM 72b-SO-DIMM Design Specification

Revision 0.05

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1 Product Description

This specification defines the electrical and mechanical requirements for 204-pin, 1.5 Volt, EP3-6400/EP3-8500/EP3-10600/EP3-12800, 72 bit-wide, Double Data Rate Synchronous DRAM Small Outline Dual In-Line Memory Modules (DDR3 SDRAM 72b-SO-DIMMs). These 72b-SO-DIMMs are intended for use as main memory when installed in embedded systems such as telecommunications I/O cards. EP3-6400/EP3-8500/EP3-10600/EP3-12800 refers to the JEDEC standard DIMM naming convention in which EP3-6400/EP3-8500/EP3-10600/EP3-12800 indicates a 204-pin DIMM running at 400/533/666/800 MHz clock speed and offering 6400/8500/10600/12800 MB/s bandwidth on the primary data bus.

Reference design examples are included which provide an initial basis for 72b-SO-DIMM designs which may be unbuffered (72b-SO-DIMM), registered (72b-SO-RDIMM), or clocked (72b-SO-CDIMM). Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC3-6400/PC3-8500/PC3-10600/PC3-12800 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

Table 1 — Product Family Attributes

DIMM organization	x72 ECC
DIMM dimensions : height (nom.) x width (nom.) x thickness (max.) / MO-number, Variation	30.0 mm x 67.6 mm x 3.80 mm / MO-268, Variation xA 30.0 mm x 67.6 mm x 6.75 mm / MO-268, Variation TBD 30.0 mm x 67.6 mm x 7.55 mm / MO-268, Variation TBD
Pin count	204
SDRAMs supported	512 Mb, 1 Gb, 2 Gb, 4 Gb, 8 Gb
Ranks supported per DIMM	1, 2, 4
Capacity	256 MB, 512 MB, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB, 32 GB
Serial PD	Consistent with JC 45
Voltage options	1.5 volt (V_{DD}), 3.3 volt (V_{DDSPD})
Interface	1.5 volt signal switching based on reference voltage at $V_{DD}/2$. See DRAM specification for more detail.

2 Environmental Requirements

DDR3 SDRAM 72b-SO-DIMMs are intended for use in telecommunications environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating temperature	See Note		3
H _{OPR}	Operating humidity (relative)	10 to 90	%	Note
T _{STG}	Storage temperature	-50 to +100	°C	Note
H _{STG}	Storage humidity (without condensation)	5 to 95	%	Note
P _{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	Note, Note

Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2 Up to 9850 ft.

Note 3 The designer must meet the case temperature specifications for individual module components.

3 Pinout and Description

Table 3 — Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0_t	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
CK0_c	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CK1_t	Clock Input, positive line	1	CB[7:0]	Data check bits Input/Output	8
CK1_c	Clock Input, negative line	1	DQS_t[8:0]	Data strobes	9
CKE[1:0]	Clock Enables	2	DQS_c[8:0]	Data strobes, negative line	9
RAS_n	Row Address Strobe	1	DM[8:0]	Data Masks / Data strobes, Termination data strobes	9
CAS_n	Column Address Strobe	1			
WE_n	Write Enable	1			
S_n[3:0]	Chip Selects	4	EVENT_n	Reserved for optional hardware temperature sensing	1
A[9:0],A11, A[15:13]	Address Inputs	14			
A10/AP	Address Input/Autoprecharge	1	RESET_n	Register and SDRAM control pin	1
A12/BC_n	Address Input/Burst chop	1	V _{DD}	Power Supply	xx
BA[2:0]	SDRAM Bank Addresses	3	V _{SS}	Ground	xx
SCL	Serial Presence Detect (SPD) Clock Input	1	V _{REFDQ}	Reference Voltage for DQ	1
SDA	SPD Data Input/Output	1	V _{REFCA}	Reference Voltage for CA	1
SA[1:0]	SPD Address Inputs	2	V _{TT}	Termination Voltage	2
Par_In	Parity bit for the Address and Control bus	1	V _{DDSPD}	SPD Power	1
Err_Out_n	Parity error found on the Address and Control bus	1	Total		204

Table 4 — Registered DIMM Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0_t	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAMs on rank 0 (72b-SO-DIMM).
CK0_c	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAMs on rank 0 (72b-SO-DIMM).
CK1_t	IN	Positive Edge	Positive line of a secondary differential pair of system clock inputs. Terminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 of 72b-SO-DIMMs.
CK1_c	IN	Negative Edge	Negative line of a secondary differential pair of system clock inputs. Terminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 of 72b-SO-DIMMs.

Table 4 — Registered DIMM Input/Output Functional Description (Cont'd)

Symbol	Type	Polarity	Function
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). Connected to the registering clock driver on 72b-SO-RDIMMs, connected to DRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs.
S_n[3:0]	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs. For 72b-SO-RDIMMs, other combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2] operate similarly to S[1:0] for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
RAS_n, CAS_n, WE_n	IN	Active Low	When sampled at the positive rising edge of the clock, CAS_n, RAS_n, and WE_n define the operation to be executed by the SDRAM. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
V _{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V _{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, RAS_n, CAS_n, WE_n, S0_n, S1_n, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
A[15:13, 12/BC_n,11, 10/AP,9:0]	IN	—	Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS command. The address inputs also provide the op-code during Mode Register Set commands. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
DQ[63:0], CB[7:0]	I/O	—	Data and Check Bit Input/Output pins
DM[8:0]	IN	Active High	Masks write data when high, issued concurrently with input data.
V _{DD} , V _{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic.
V _{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS_t[17:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data.
DQS_c[17:0]	I/O	Negative Edge	Negative line of the differential data strobe for input and output data.
SA[1:0]	IN	—	These signals are tied at the system planar to either V _{SS} or V _{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V _{DDSPD} on the system planar to act as a pullup.

Table 4 — Registered DIMM Input/Output Functional Description (Cont'd)

Symbol	Type	Polarity	Function
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus to V_{DDSPD} on the system planar to act as a pullup.
EVENT_n	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on TS/SPD part.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET_n	IN		The RESET_n pin is connected to the RESET_n pin on the register (72b-SO-RDIMM) and to the RESET_n pin on the SDRAMs (all modules). When low, all register outputs will be driven low and the Clock Driver clocks to the DRAMs and register(s) will be set to low level (the Clock Driver will remain synchronized with the input clock).
Par_In	IN		Parity bit for the Address and Control bus. ("1 ": Odd, "0 ": Even). Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.
Err_Out_n	OUT (open drain)		Parity error detected on the Address and Control bus. A resistor may be connected from Err_Out_n bus line to V_{DD} on the system planar to act as a pull up. Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.

Table 5 — DDR3 204-pin 72b-SO-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREFDQ	2	VSS	53	VSS	54	DQ28	103	A3	104	A4	155	VSS	156	DQS5_t
3	VSS	4	DQ4	55	DQ24	56	DQ29	105	A1	106	A2	157	DM5	158	VSS
5	DQ0	6	DQ5	57	DQ25	58	VSS	107	A0	108	BA1	159	DQ42	160	DQ46
7	DQ1	8	VSS	59	DM3	60	DQS3_c	109	VDD	110	VDD	161	DQ43	162	DQ47
9	VSS	10	DQS0_c	61	VSS	62	DQS3_t	111	CK0_t	112	Par_In, NC, CK1_t	163	VSS	164	VSS
11	DM0	12	DQS0_t	63	DQ26	64	VSS	113	CK0_c	114	Err_Out_n, NC, CK1_c	165	DQ48	166	DQ52
13	DQ2	14	VSS	65	DQ27	66	DQ30	115	VDD	116	VDD	167	DQ49	168	DQ53
15	DQ3	16	DQ6	67	VSS	68	DQ31	117	A10/AP	118	S3_n	169	VSS	170	VSS
17	VSS	18	DQ7	69	CB0	70	VSS	119	BA0	120	S2_n	171	DQS6_c	172	DM6
19	DQ8	20	VSS	71	CB1	72	CB4	121	WE_n	122	RAS_n	173	DQS6_t	174	DQ54
21	DQ9	22	DQ12	Key				123	VDD	124	VDD	175	VSS	176	DQ55
23	VSS	24	DQ13	73	VSS	74	CB5	125	CAS_n	126	ODT0	177	DQ50	178	VSS
25	DQS1_c	26	VSS	75	DQS8_c	76	DM8	127	S0_n	128	ODT1	179	DQ51	180	DQ60
27	DQS1_t	28	DM1	77	DQS8_t	78	VSS	129	S1_n	130	A13	181	VSS	182	DQ61
29	VSS	30	RESET_n	79	VSS	80	CB6	131	VDD	132	VDD	183	DQ56	184	VSS
31	DQ10	32	VSS	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	DQS7_c
33	DQ11	34	DQ14	83	CB3	84	VREFCA	135	DQ33	136	DQ37	187	VSS	188	DQS7_t
35	VSS	36	DQ15	85	VDD	86	VDD	137	VSS	138	VSS	189	DM7	190	VSS
37	DQ16	38	VSS	87	CKE0	88	A15	139	DQS4_c	140	DM4	191	DQ58	192	DQ62
39	DQ17	40	DQ20	89	CKE1	90	A14	141	DQS4_t	142	DQ38	193	DQ59	194	DQ63
41	VSS	42	DQ21	91	BA2	92	A9	143	VSS	144	DQ39	195	VSS	196	VSS
43	DQS2_c	44	DM2	93	VDD	94	VDD	145	DQ34	146	VSS	197	SA0	198	EVENT_n
45	DQS2_t	46	VSS	95	A12/BC_n	96	A11	147	DQ35	148	DQ44	199	VDDSPD	200	SDA
47	VSS	48	DQ22	97	A8	98	A7	149	VSS	150	DQ45	201	SA1	202	SCL
49	DQ18	50	DQ23	99	A5	100	A6	151	DQ40	152	VSS	203	VTT	204	VTT
51	DQ19	52	VSS	101	VDD	102	VDD	153	DQ41	154	DQS5_c				

Terminology:

- * Active low signals are indicated by the suffix “_n”
- * Positive line of differential pairs are indicated by the suffix “_t”
- * Complementary inputs of differential pairs are indicated by the suffix “_c”

See Notes on following page for differences of 72b-SO-RDIMMs, 72b-SO-CDIMMs, and 72b-SO-DIMMs

Table 6 — Pinout Comparison Based on Module Type

Pin #	72b-SO-RDIMM		72B-SO-CDIMM		72B-SO-DIMM	
	Signal	Notes	Signal	Notes	Signal	Notes
89	CK0_c	Connected to CK_t and CK_c inputs on registering clock driver	CK0_c	Connected to CK_t and CK_c inputs on PLL	CK0_c	Connected to rank 0 SDRAMs
87	CK0_t		CK0_t		CK0_t	
88	Par_In	Connected to the registering clock driver	CK1_t	CK1_t and CK1_c are terminated but not used	CK1_t	Connected to rank 1 SDRAMs on 2 rank DIMMs, terminated but not used on 1 rank DIMMs
90	ErrOut_n		CK1_n		CK1_c	
121	S1_n	Connected to the registering clock driver	S1_n	Used for dual-rank 72b-SO-CDIMMs, not connected on single-rank 72b-SO-CDIMMs	S1_n	Used for 2 rank DIMMs, not connected on 1 rank DIMMs
114	ODT1, NC	Connected to the registering clock driver on dual- and quad- rank DIMMs; NC on single-rank DIMMs	ODT1, NC	Used for dual-rank DIMMs, not connected on single-rank DIMMs	ODT1, NC	Used for dual-rank DIMMs, not connected on single-rank DIMMs
126	S2_n, NC	Connected to the register on 4 rank DIMMs, not connected on 1 or 2 rank DIMMs	NC	Not used	NC	Not used
119	CKE1	Connected to the register on 2 and 4 rank DIMMs; NC on 1 rank DIMMs	CKE1, NC	Used for 2 rank DIMMs, not connected on 1 rank DIMMs	CKE1, NC	Used for 2 rank DIMMs, not connected on 1 rank DIMMs
117	A15	Connected to the registering clock driver	A15, NC	Depending on device density, may not be connected to SDRAMs. However, these signals are terminated. A15 not routed on some Raw Cards	A15, NC	Depending on device density, may not be connected to SDRAMs. However, these signals are terminated. A15 not routed on some Raw Cards
130	A14		A14		A14	
101	A13		A13		A13	
125	S3_n, NC	Connected to the register on 4 rank DIMMs, not connected on 1 or 2 rank DIMMs	NC	Not used	NC	Not used

NC = no internal connection

4 Component Details

Table 7 — Supported SDRAM Components Maximum size for 512Mb to 8Gb; DDR3 SDRAM

This table is for reference only. Please see appropriate raw card annex for more information.

Raw Card	Supported DRAM Outline (Width x Length) max.	Package Type	MO-207 variation
A	TBD	Planar	DW-z
B	TBD	Planar	DW-z
C	TBD	Planar	DW-z
D	TBD	Planar	DW-z
E	TBD	Planar	DT-z
F	TBD	Planar	DT-z

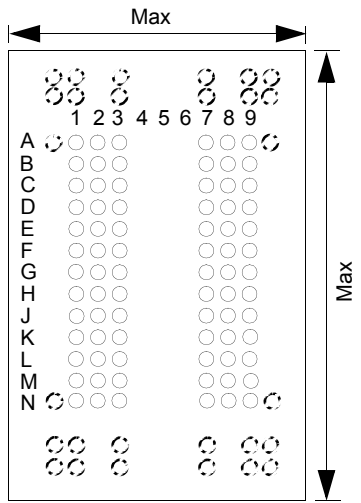
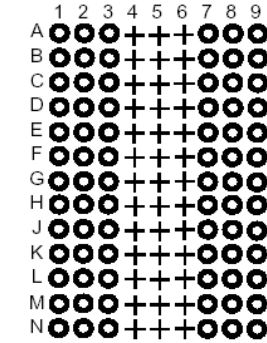


Table 8 — Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM
(MO-207 Variation DT-z/DW-z, 60 Balls FBGA 0.8 mm x 0.8 mm pitch)

x4 Ballout of DDR3 SDRAMs (Top view)

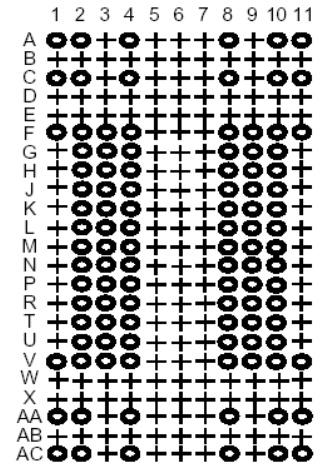
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS_n	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



○ Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



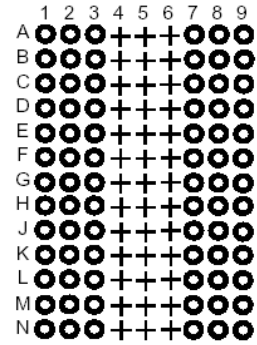
Note 1 Above coordinates of ball out corresponds to footprint on PCB (page 16).
Note 2 "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note 3 NC balls may be mated with any solder pad on PCB.

Table 9 — Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM
(MO-207 Variation DT-z/DW-z, 60 Balls FBGA 0.8 mm x 0.8 mm pitch)

x8 Ballout of DDR3 SDRAMs (Top view)

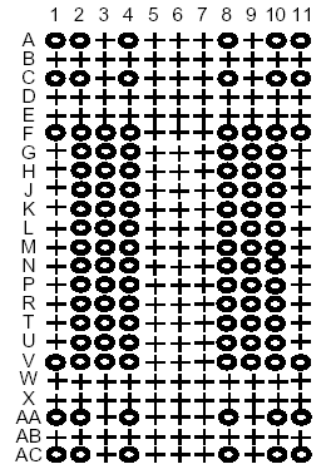
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS_n	CK_t	VSS	NC		F
M		ODT	VDD	CAS_n	CK_c	VDD	CKE		G
N		NC	CS_n	WE_n	A10/AP	ZQ	NC		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



● Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls

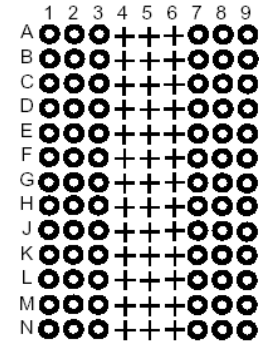


- Note 1** Above coordinates of ball out corresponds to footprint on PCB (page 15).
- Note 2** "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
- Note 3** NC balls may be mated with any solder pad on PCB.
- Note 4** "NU" means that the ball is present and may or may not be electrically connected to an active signal in the SDRAM package.
- Note 5** NU balls may only be mated with NC solder pads on PCB.

Table 10 — Pin Assignments for 512Mb to 8Gb; DDR3 SDRAM
MO-207 Variation DW-z, 60 Balls FBGA 0.8 mm x 0.8 mm pitch)
x4 Ballout of DDR3 SDRAMs for Stacked DIMM (Top view)

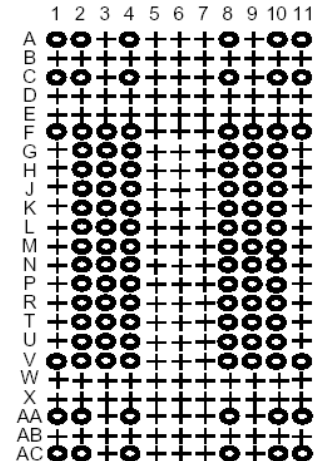
	1	2	3	4	8	9	10	11	
A	NC	NC		NC	NC		NC	NC	
B									
C	NC	NC		NC	NC		NC	NC	
D									
E									
F	NC	VSS	VDD	NC	NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS_c	VDD	VSS	VSSQ		D
K		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ		E
L		ODT1	VSS	RAS_n	CK	VSS	CKE1		F
M		ODT0	VDD	CAS_n	CK	VDD	CKE0		G
N		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2	A15	V _{REFCA}	VSS		J
R		VDD	A3	A0	A12/BC_n	BA1	VDD		K
T		VSS	A5	A2	A1	A4	VSS		L
U		VDD	A7	A9	A11	A6	VDD		M
V	NC	VSS	RESET_n	A13	A14	A8	VSS	NC	N
W									
Y									
AA	NC	NC		NC	NC		NC	NC	
AB									
AC	NC	NC		NC	NC		NC	NC	
		1	2	3	7	8	9		

MO-207 Variation DT-z



○ Populated ball
+ Ball not populated

MO-207 Variation DW-z
with support balls



Note 1 Above coordinates of ball out corresponds to footprint on PCB (page 16).
Note 2 "NC" means that the ball is present and is not connected to any signal in the SDRAM package.
Note 3 NC balls may be mated with any solder pad on PCB.

Table 11 — SDRAM Landing Pattern Assignments on DIMM
x4 footprint on PCB (Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		NC	VSS	RAS_n	CK	VSS	NC	
G		ODT	VDD	CAS_n	CK	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

Note 1 Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note 2 "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note 3 NC solder pads may be mated with any balls of an SDRAM.

Table 12 — SDRAM Landing Pattern Assignments on DIMM
x8 footprint on PCB (Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NU/ TDQS_c	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM/ TDQS_t	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	DQ6	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	DQ4	DQ7	DQ5	VDDQ	
F		NC	VSS	RAS_n	CK_t	VSS	NC	
G		ODT	VDD	CAS_n	CK_c	VDD	CKE	
H		NC	CS_n	WE_n	A10/AP	ZQ	NC	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

- Note 1** Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.
Note 2 "NC" means that a solder pad is present and is not connected to any signal on the PCB.
Note 3 NC solder pads may be mated with any balls of an SDRAM.

Table 13 — SDRAM Landing Pattern Assignments on DIMM
x4 footprint on PCB for Stacked DIMM (Top view)

		1	2	3	7	8	9	
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC
A	NC	VSS	VDD	NC	NC	VSS	VDD	NC
B		VSS	VSSQ	DQ0	DM	VSSQ	VDDQ	
C		VDDQ	DQ2	DQS_t	DQ1	DQ3	VSSQ	
D		VSSQ	NC	DQS_c	VDD	VSS	VSSQ	
E		V _{REFDQ}	VDDQ	NC	NC	NC	VDDQ	
F		ODT1	VSS	RAS_n	CK_t	VSS	CKE1	
G		ODT0	VDD	CAS_n	CK_c	VDD	CKE0	
H		CS1_n	CS0_n	WE_n	A10/AP	ZQ0	ZQ1	
J		VSS	BA0	BA2	A15	V _{REFCA}	VSS	
K		VDD	A3	A0	A12/BC_n	BA1	VDD	
L		VSS	A5	A2	A1	A4	VSS	
M		VDD	A7	A9	A11	A6	VDD	
N	NC	VSS	RESET_n	A13	A14	A8	VSS	NC
	NC	NC		NC	NC		NC	NC
	NC	NC		NC	NC		NC	NC

Note 1 Above coordinates of footprint corresponds to previous ballout of DDR3 SDRAMs.

Note 2 "NC" means that a solder pad is present and is not connected to any signal on the PCB.

Note 3 NC solder pads may be mated with any balls of an SDRAM.

Table 14 — Pin Assignments for Registering Clock Driver (SSTE32882)

1:2 Register with Address and Command Parity Function (Top View)

176-Ball TFBGA 0.65 x 0.65 mm pitch [MO-246 Variation E]

Front Configuration (MIRROR = 0)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	RSVD	VSS	RESET_n	MIRROR	ERROUT_n	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1_n	VDD		VDD	VDD	VDD		VDD	QBCS1_n	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWEn	QACS0_n	VDD		VDD	VDD	VDD		VDD	QBCS0_n	QBWE_n
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS_n	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS_n
P	QARAS_n	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	QBRAS_n
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DOT1
T	DCKE0	DCS0_n								DCS1_n	DOT0
U	DA12	DBA2		Y1_c	PVSS	VDD	PVDD	Y0_c		DA13	DCAS_n
V	DA9	DA11		Y1_t	PVSS	VSS	PVDD	Y0_t		DRAS_n	DWE_n
W	DA8	DA6	FBIN_c	Y3_c	AVSS	CLK_c	RSVD	Y2_c	FBOUOut_c	DA0	DBA0
Y	DA7	RSVD	FBIN_t	Y3_t	AVDD	CLK_t	VREFCa	Y2_t	FBOUOut_t	PAR_IN	DBA1

Note 1 RSVD indicates ball positions reserved for future functions. These balls must not be connected electrically to any signal on the system or to the device die. However, a ball on the device and a connecting pad on the module are required in those locations.

Note 2 This figure is valid for Revision TBD of the register specification. Refer to the register specification TBD for any later revisions.

Table 15 — Pin Assignments for Registering Clock Driver (SSTE32882)

1:2 Register with Address and Command Parity Function (Top View)

176-Ball TFBGA 0.65 x 0.65 mm pitch [MO-246 Variation E]

Back configuration (MIRROR = 1)

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	RSVD	VSS	RESET_n	MIRROR	ERROUT_n	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	QACS1_n	VDD		VDD	VDD	VDD		VDD	QBCS1_n	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	QAWEn	QACS0_n	VDD		VDD	VDD	VDD		VDD	QBCS0_n	QBWE_n
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	QACAS_n	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	QBCAS_n
P	QARAS_n	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	QBRAS_n
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	DCS1_n								DCS0_n	DCKE0
U	DCAS_n	DA13		Y1_c	PVSS	VDD	PVDD	Y0_c		DBA2	DA12
V	DWE_n	DRAS_n		Y1_t	PVSS	VSS	PVDD	Y0_t		DA11	DA9
W	DBA0	DA0	FBIN_c	Y3_c	AVSS	CLK_c	RSVD	Y2_c	FBOUOut_c	DA6	DA8
Y	DBA1	PAR_IN	FBIN_t	Y3_t	AVDD	CLK_t	VREFCA	Y2_t	FBOUOut_t	RSVD	DA7

Note 1 RSVD indicates ball positions reserved for future functions. These balls must not be connected electrically to any signal on the system or to the device die. However, a ball on the device and a connecting pad on the module are required in those locations.

Note 2 This figure is valid for Revision TBD of the register specification. Refer to the register specification TBD for any later revisions.

Table 16 — Critical Registering Clock Driver Specifications for PC3-10600

Register	Symbol	Parameter	Conditions	T _C = TBD V _{DD} = 1.5 V ± 0.075 V		Units	Notes
				Min	Max		
1:2 28-bit	f _{clock}	Input Clock Frequency	application frequency	300	670	MHz	
	t _{CH/tCL}	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	t _{CK}	
	t _{ACT}	Inputs active time before RESET_n is taken HIGH	DCKE0/1=LOW and DCS0/1_n=HIGH	8	-	t _{CK}	
	t _{SU}	Setup time	Input valid before CK_t/CK_c	100	-	ps	
	t _H	Hold time	Input to remain valid after CK_t/CK_c	175	-	ps	
	t _{PDM}	Propagation delay, single-bit switching	CK_t/CK_c to output	-	1.0	ns	
	t _{DIS}	output disable time	CK_t/CK_c to output float	0	TBD	ns	
	t _{EM}	output enable time	CK_t/CK_c to output driving	-	1.1	ns	
	C _{IN(DATA)}	Data Input Capacitance		2	3		
	C _{IN(CLOCK)}	Clock Input Capacitance		2	3		
C _{IN(RST)}	Reset Input Capacitance		TBD	TBD			

Table 17 — Critical Clock Driver Specifications for PC3-10600

Clock driver Characteristics at application frequency

Device	Symbol	Parameter	Conditions	T _C = TBD V _{DD} = 1.5V ± 0.075V		Units	Notes
				Min	Max		
1:2, 1.5 Volt	t _{jit(cc)}	Cycle-to-cycle period jitter		0	40	ps	
	t _{STAB}	Stabilization time		-	6	us	
	t _{fdyn}	Dynamic phase offset		-50	50	ps	
	t _{CKsk}	Clock Output skew			50	ps	
	t _{jit(per)}	Yn Clock Period jitter		-40	40	ps	
	t _{jit(hper)}	Half period jitter		-50	50	ps	
	t _{Qsk1}	Qn Output to clock tolerance (Standard 1/2-Clock Pre-Launch)		-100	200	ps	
	t _{Qsk2}	Output clock tolerance (3/4 Clock Pre-Launch)		-100	200	ps	
t _{dynoff}	Maximum re-driven dynamic clock off-set		-80	80	ps		

Note 1 The value in this table are valid for revision xx of Register specification TBD.

Note 2 Refer to the register specification for any later revision

5 DDR3 Registered DIMM Wiring Details

5.1 Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into six groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group
Clock Driver Input / Unused Clocks	CK0_t, CK0_c, CK1_t, CK1_c
Clock Driver Output	FBOUT_t, FBOUT_c, PCK[3:0]
Data, DQS_t, DQS_c, DM	DQ[63:0], CB[7:0], DQS_t[8:0], DQS_c[8:0], DM[8:0]
Address and Control Chip Select, Clock Enable, ODT	A[15:0], BA[2:0], RAS_n, CAS_n, WE_n S_n[3:0], CKE[1:0], Par_In, ODT[1:0]
Address and Command Parity	Err_Out_n
RESET_n	RESET_n

5.2 General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing guidelines are as follows

- Route all signal traces except clocks using 0.1/0.1 rules, i.e., 0.1 mm traces and 0.1 mm minimum spacing between adjacent traces. But spacing should be as wide as possible to prevent crosstalk.
- Route clocks using 0.1 mm lines and 0.1 mm spaces between differential clock pairs and differential DQS_t, DQS_c.
- Route clocks using at least 90% of the total trace length in the inner layers. Maximize use of internal layers for routing clocks. Surface routing should be minimized and limited to what is necessary to connect to component.
- Signals are referenced to Vss or Vdd on adjacent layers. Data signals (DQ, DQS_t, DQS_c, and DM) are referenced to Vss. Address and Command signals are referenced to VDD.
- The registering clock driver feedback path must meet the desired flight time from FBOUT to FBIN of 95±15ps. Any change in stackup impedance, or use of vias, must be taken into account in this calculation.

5.3 Signal referencing information

Signal groups	Referencing	Signal groups	Referencing
DQ/DQS pair /DM	Ground layer	Pre-register address and command net	Vdd shape
Clock nets	Vdd shape	Post-register address and command net	Vdd shape

5.4 Differential Clock Net Structures

CK0_t, CK0_c

DDR3 SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54 mm total) between clocks of the same function

Clock Driver input net segment length is newly defined and optimized for high speed DDR3 Registered DIMMs.

5.5 Test Points

Test points are provided on the DIMMs for probing purposes where signals can not be probed using existing vias or components. These test points vary by DIMM design. The test point signals are summarized in the corresponding appendices and are documented in the schematics as well as in an assembly drawing showing the location of the test points.

5.6 Test Point location

All DDR3 components are in BGA packages which makes the package pads inaccessible for probing during system development. The DDR3 Registered DIMMs have test points identified to make initial evaluation easier. In some cases test pads have been added and in other cases existing vias are used as test points. An effort has been made to provide testability on some signals in all signal groups but 100% coverage is not possible. All test points must have a power and/or ground via within 500 mils. Test point location and /or availability are indicated for each raw card in the corresponding annexes.

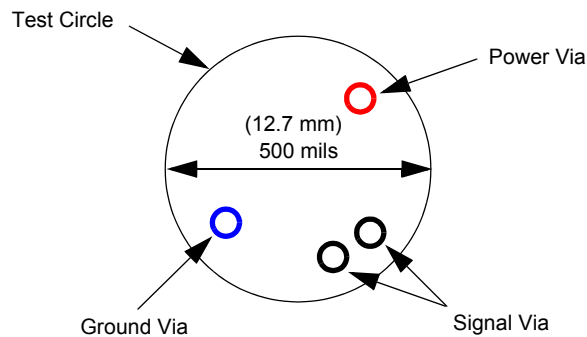


Figure 1 — Test Point Location

5.7 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

5.8 Net Structure Example

A 1 GB double-sided x72 DIMM using 512 Mbit, 64Mx8 SDRAM devices would have a data net structure as shown in Figure 2.

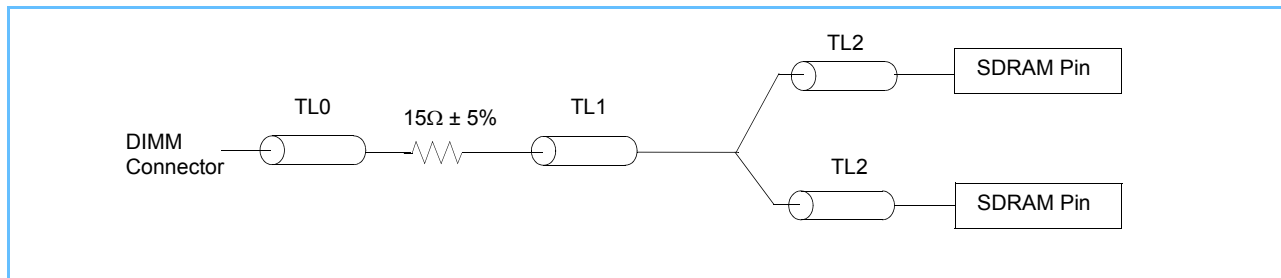


Figure 2 — Data net structure

6 Timing Budget (TBD)

7 On DIMM Thermal Sensor

The following schematics illustrate the possible wiring choices for the SPD and TS.

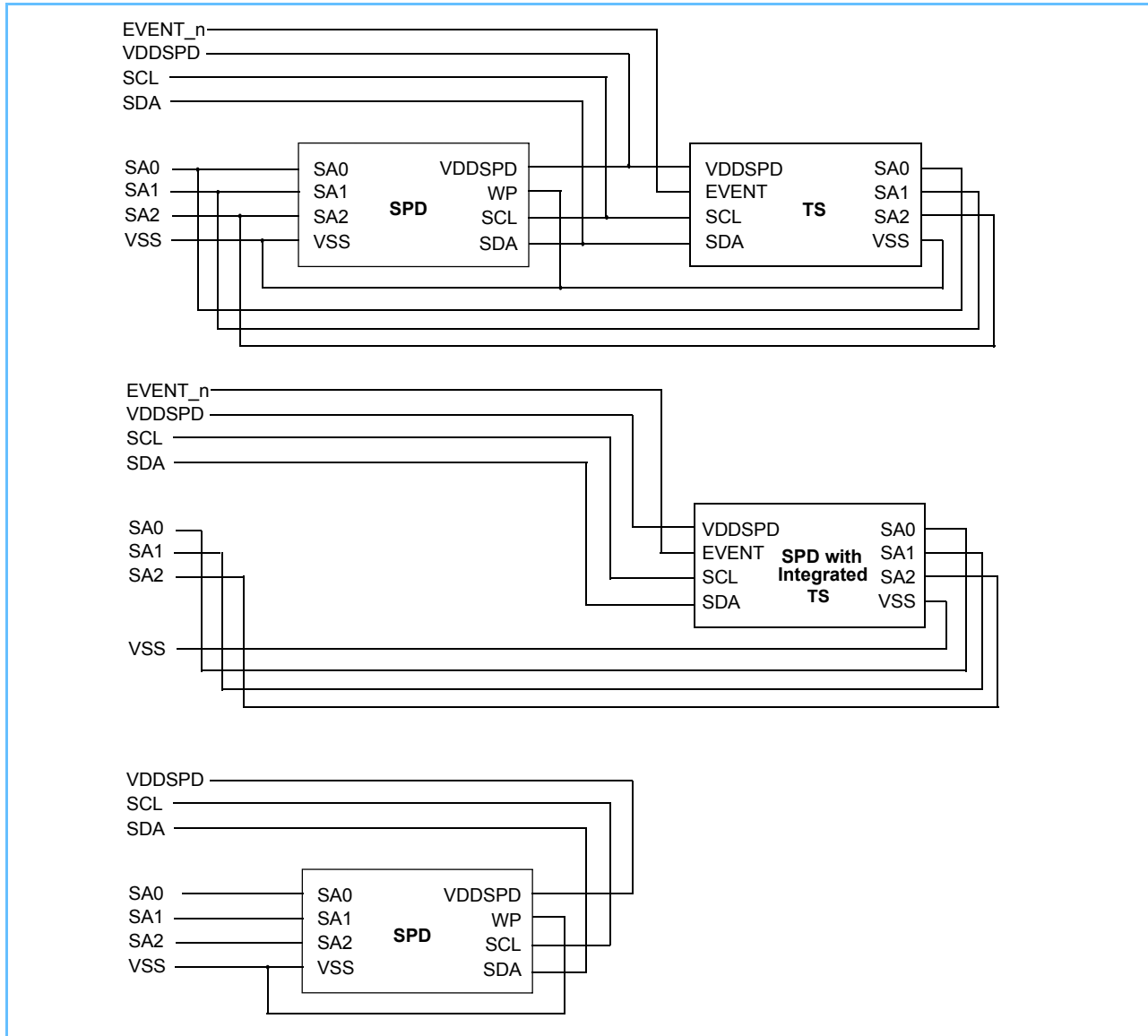


Figure 3 — Schematic connection of Thermal Sensor (TS) and SPD

Optional on DIMM thermal sensor will provide DRAM temperature readout through discrete or integrated thermal sensor.

On LP (low profile, 30 mm) DIMMs the TS and SPD footprint will be placed above the register on DIMM front and back. Refer to MO-269 for placement requirements. TDFN packages are used for TS and SPD. MO-229 variation VCED-3 or VEED-7 will be referenced for TS and SPD part.

8 Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC3-6400 DDR3 SDRAM R-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR3 SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices.

The following table is intended to be an **example** of a typical PC3-8500 72b-SO-RDIMM. SPD values indicating different DIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or DIMMs. This example assumes:

- Module Organization: 512MB (64Mx72)
- Device Composition: 64Mx8
- Device Package: FBGA
- Module Physical Ranks: 1
- CAS latency: 6 (DDR3-1066)

Table 18 — Typical PC3-8500 72b-SO-RDIMM. SPD values

Byte #	Function Described	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial Bytes Written / SPD Device Size / CRC Coverage	Bytes 0-116/256/176	92	1, 2
1	SPD revision	Rev 1.0	10	
2	Key Byte / DRAM device type	DDR3 SDRAM	0B	
3	Key Byte / Module type	RDIMM	01	
4	SDRAM Density and Banks	512Mb, 8 banks	01	3
5	SDRAM Addressing	13 rows, 10 columns	09	3
6	Reserved	None	00	
7	Module Organization	1 Rank, x8 DQs	01	3
8	Module Memory Bus Width	ECC, 64-bit Bus	0B	
9	Fine Timebase (FTB) Dividend / Divisor	5/2 = 2.5ps	52	
10	Medium Timebase (MTB) Dividend	1ns	01	
11	Medium Timebase (MTB) Divisor	8ns	08	
12	SDRAM Minimum Cycle Time (tCK _{min})	1.875ns	0F	3
13	Reserved	None	00	
14	CAS Latencies Supported, Least Significant Byte	CL 6	04	3
15	CAS Latencies Supported, Most Significant Byte	None	00	3
16	Minimum CAS Latency Time (tA _{min})	11.25ns	5A	3
17	Minimum Write Recovery Time (tWR _{min})	15ns	78	3
18	Minimum RAS _n to CAS _n Delay Time (tRCD _{min})	11.25ns	5A	3
19	Minimum Row Active to Row Active Delay Time (tRRD _{min})	9ns	48	3
20	Minimum Row Precharge Delay Time (tRP _{min})	11.25ns	5A	3
21	Upper nibble for tRAS and tRC	1(2C) and 1(A4)	11	3
22	Minimum Active to Precharge Delay Time (tRAS _{min}), LSB	37.5ns	2C	3

Table 18 — Typical PC3-8500 72b-SO-RDIMM. SPD values (Cont'd)

Byte #	Function Described	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
23	Minimum Active to Active / Refresh Delay Time (t_{RCmin}), LSB	48.75ns	86	3
24	Minimum Refresh Recovery Delay Time (t_{RFCmin}) LSB	(combo bytes 24, 25)	D0	3
25	Minimum Refresh Recovery Delay Time (t_{RFCmin}) MSB	90ns	02	3
26	Minimum Internal Write to Read Command Delay Time (t_{WTRmin})	7.5ns	3C	3
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTPmin})	7.5ns	3C	3
28	Upper Nibble for t_{FAW}	(combo bytes 28, 29)	01	3
29	Minimum Four Active Window Delay Time (t_{FAWmin})	37.5ns	2C	3
30	SDRAM Optional Features	RZQ/6 supported	01	3
31	SDRAM Thermal and Refresh Options	ASR, extended temperature	05	3
32-59	Reserved, General Section	None	00000000	
60-116	Module Type Specific Section, Indexed by Key Byte 3			
117-118	Module ID: Module Manufacturer's JEDEC ID Code	Variable Data		
119	Module ID: Module Manufacturing Location	Variable Data		
120-121	Module ID: Module Manufacturing Date	Variable Data		
122-125	Module ID: Module Serial Number	Variable Data		
126-127	Cyclical Redundancy Code	Variable Data		
128-145	Module Part Number	Variable Data		4
146-147	Module Revision Code	Variable Data		4
148-149	DRAM Manufacturer's JEDEC ID Code	Variable Data		4
150-175	Manufacturer's Specific Data	Variable Data		4
176-225	Open for customer use	Variable Data		

Note 1 Number of SPD bytes written will typically be programmed as 128 or 176 bytes.
Note 2 Size of SPD device will typically be programmed as 256 bytes.
Note 3 From DDR3 SDRAM data sheet.
Note 4 These are optional, in accordance with the JEDEC spec.

9 DDR3 DIMM Label Format

This material is provided as reference only.

DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

ggggg eRxff EP3-wwwwm-aa-bb-ccd

Where:

- ggggg = Module total capacity, in bytes
256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed
1R = 1 rank of DDR3 SDRAM installed
2R = 2 ranks
4R = 4 ranks
- xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization
- wwwww = Module bandwidth in MB/s
6400 = 6.40 GB/s (PC3-800 SDRAMs, 8 byte primary data bus)
8500 = 8.53 GB/s (PC3-1066 SDRAMs, 8 byte primary data bus)
10600 = 10.66 GB/s (PC3-1333 SDRAMs, 8 byte primary data bus)
12800 = 12.80 GB/s (PC3-1600 SDRAMs, 8 byte primary data bus)
- m = Module Type
C = Small Outline Clocked DIMM ("72b-SO-CDIMM"), with PLL, no registering clock driver
R = Small Outline Registered DIMM ("72b-SO-RDIMM") with registering clock driver, no PLL
U = Small Outline Unbuffered DIMM ("72b-SO-DIMM"), with no registering clock driver or PLL
- aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency
- bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
- cc = Reference design file used for this design (if applicable)
A = Reference design for raw card 'A' is used for this assembly
B = Reference design for raw card 'B' is used for this assembly
AC = Reference design for raw card 'AC' is used for this assembly
ZZ = None of the reference designs were used for this assembly
- d = Revision number of the reference design used
0 = Initial release
1 = First revision
2 = Second revision
P = Pre-release or Engineering sample
Z = To be used when field cc = ZZ

Examples:

1GB 2Rx8 PC3-12800U-10-10-BP

is a 2 GB DDR3 unbuffered 72b-SO-DIMM using 2 ranks of x8 SDRAMs operational to DDR3-1600 performance with CAS Latency = 10 using JEDEC DDR3 SPD revision 1.0, raw card reference design file B pre-release revision used for the assembly

4GB 2Rx8 PC3-8500R-8-10-ZZZ

is a 4 GB DDR3 registered 72b-SO-RDIMM using 2 ranks of x8 SDRAMs operational to DDR3-1066 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, no JEDEC standard raw card reference design file used for the assembly

10 DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This material is included as reference and may be out of date. Download the latest version of MO-269 for any later updates. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; <http://www.jedec.org>.
2. Click on 'Free Standards' and enter the free download area.
3. Search by document number: 'MO-269' and download the PDF for this product family.
4. Or search by 'JEP95'; 'JEDEC Publication 95.' and open entire document, scroll down and select 'MO-269' to download the PDF for this product family.

Within MO-269, several DIMM thickness variations are defined. These variations are summarized in the table below, in conjunction with examples of the types of RDIMM components and assemblies that may be associated with each DIMM thickness range:

Table 19 — DIMM thickness variations

Maximum RDIMM Thickness	Comments
Less than or equal to 4.00 mm	Generally associated with DIMMs produced with devices that are 1.35 mm thick or less
> 4.00 mm and less than or equal to 6.75 mm	Generally associated with DIMMs produced with devices that are greater than 1.35 mm and less than or equal to 2.70 mm thick
> 6.75 mm and less than or equal to 7.55 mm	Generally associated with DIMMs produced with devices that are greater than 2.70 mm and less than or equal to 3.10 mm thick
> 7.55 mm	Intended to cover DIMMs produced with non-standard package thicknesses, card-on-card structures or alternate solutions

Note Maximum DIMM thickness can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.