

## Appendix Y - Raw Card Y

### DDR3 Registered Dimm Design File

Specification Revision	Applicable Design File	Applicable BOM
0.81	PC3-RDIMM_V080_RC_Y0_20090113.zip	PC3-RDIMM_V080_RC_Y0_20090113_BOM.txt

Note: "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

### Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
2GB	256Mx72	512Mbit	64Mx8	36	4	13/10/3	AB*
4GB	512Mx72	1Gbit	128Mx8	36	4	14/10/3	AB*
8GB	1Gx72	2Gbit	256Mx8	36	4	15/10/3	AB*
16GB	2Gx72	4Gbit	512Mx8	36	4	16/10/3	AB*
32GB	4Gx72	8Gbit	1Gx8	36	4	16/11/3	AB*

\*Note: without heatspreader; variations with heatspreader are TBD

### SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	Package Type	MO-207 variation
10.5 x 11.5	8	106 Ball FBGA	x8 planar, double row	DW-z

### Supported Speeds

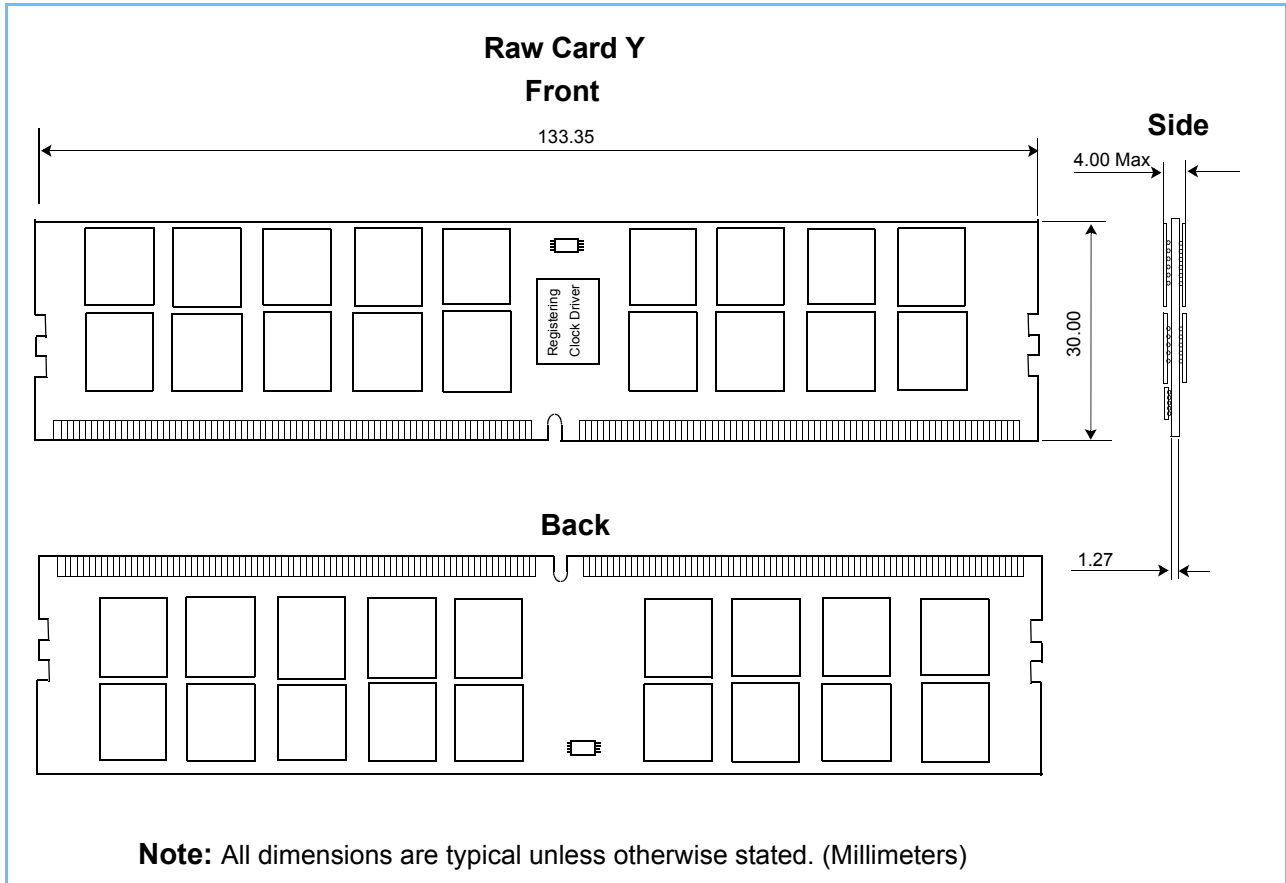
PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
X	X	X		1

1: X will reflect passed committee ballot at the time when specification is issued at BOD ballot.

### Design Rules and Deviations

0.075 mm trace width is used in this card.
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## General Layout



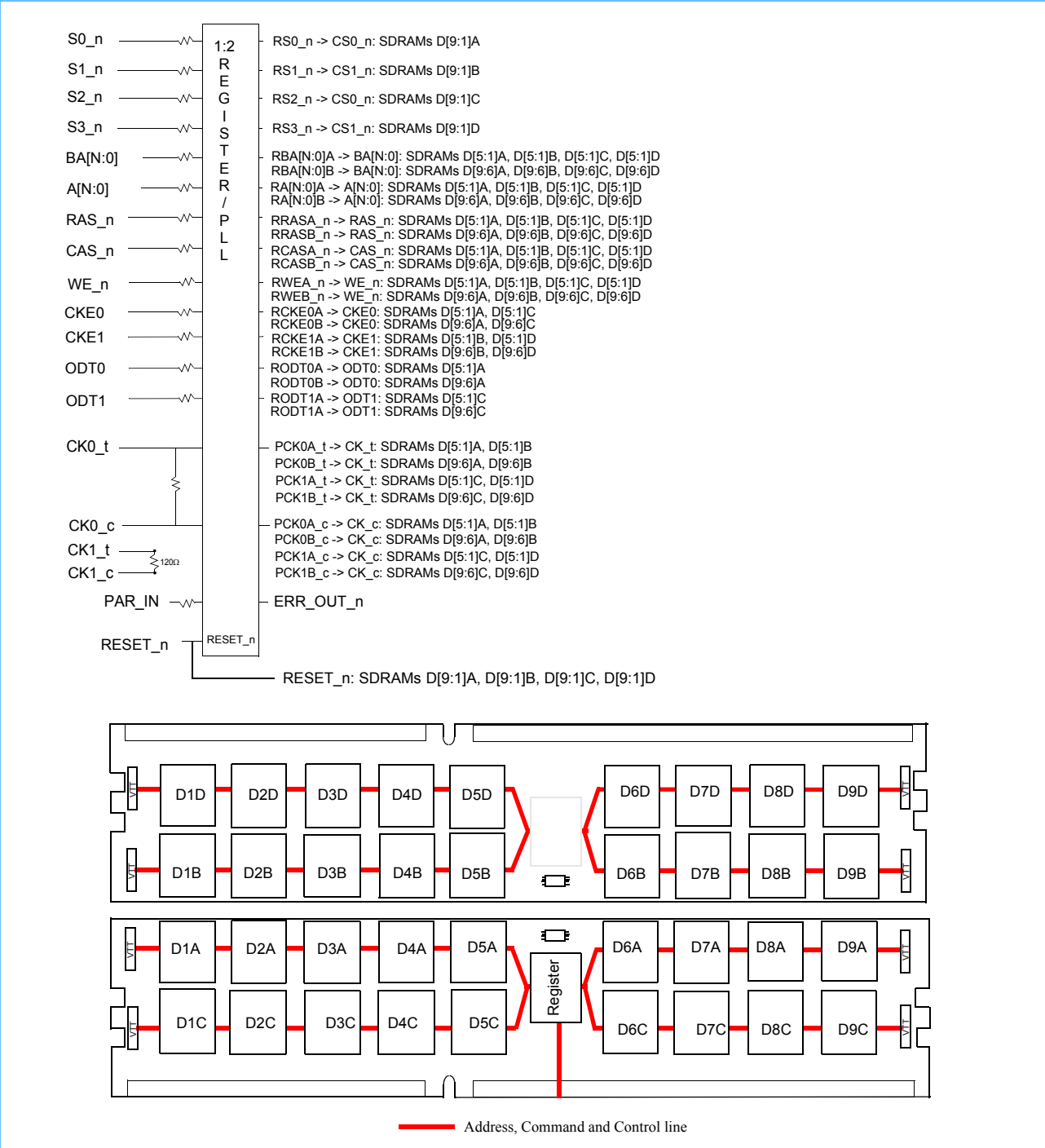
Note 1: Implementation and dimensions without heatspreader.

Note 2: Thermal sensor is placed within the Thermal Sensor Placement Area as defined in MO-269.

Note 3: In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heatspreader attached.

# Functional Block Diagram

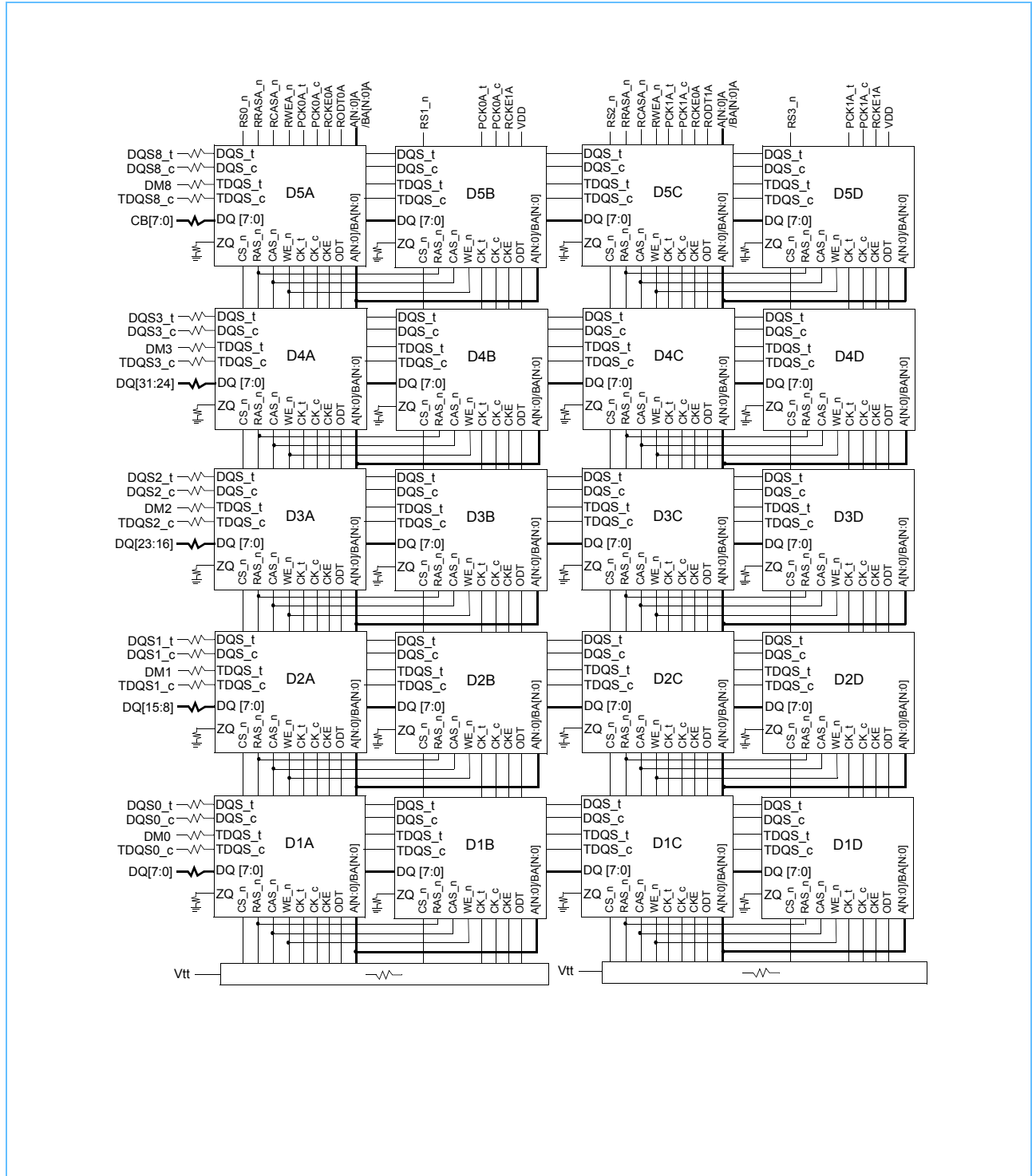
(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs, part 1 of 3)



1. CK0\_t and CK0\_c are differentially terminated with single 120Ω ±5% resistor.
2. CK1\_t and CK1\_c are differentially terminated with single 120Ω ±5% resistor but is not used.

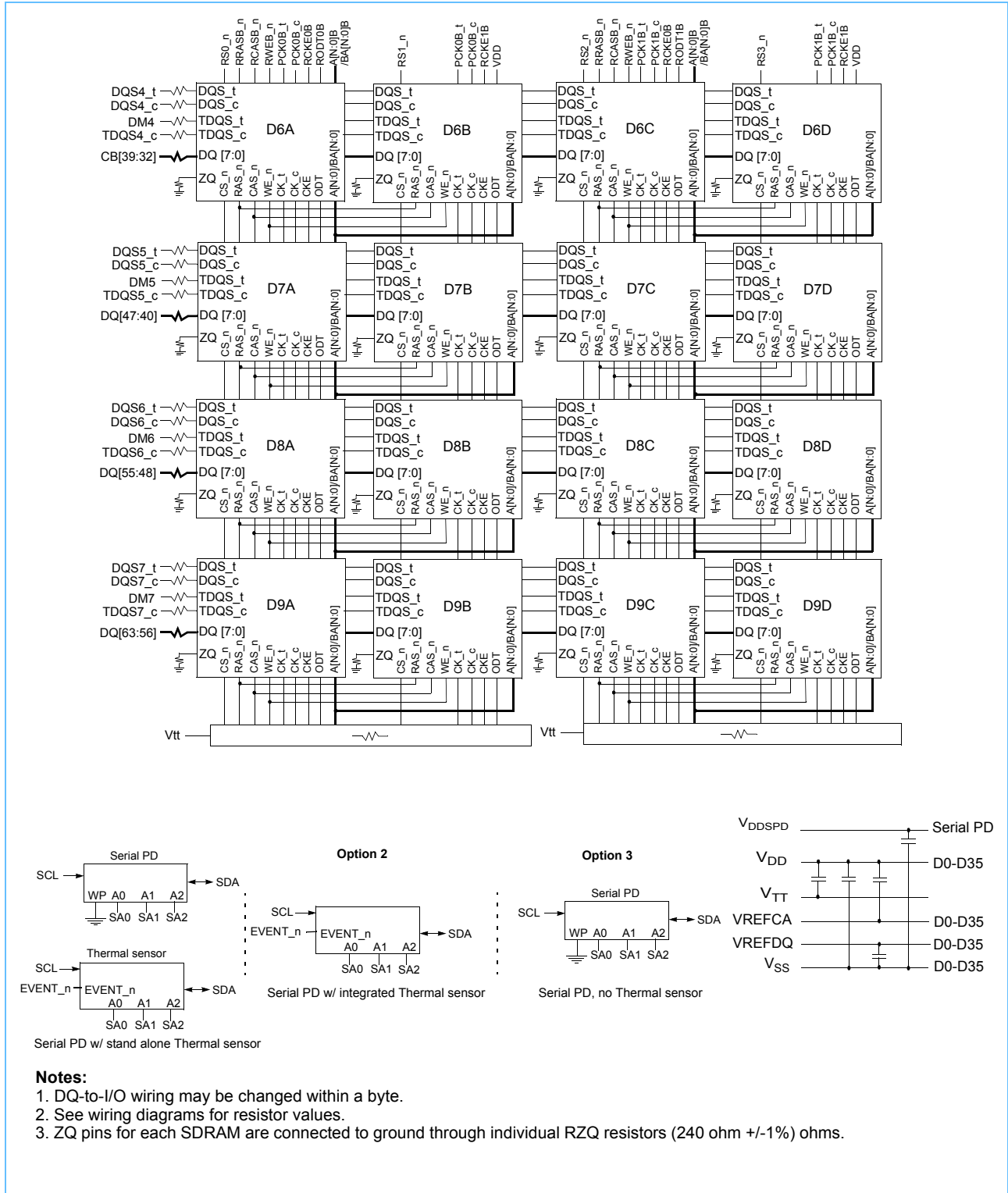
# Functional Block Diagram

(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs, part 2 of 3)



# Functional Block Diagram

(x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs, part 3 of 3)



## Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

### Component Specification.

DRAMs per output	Register Type	RegisterSpeedGrade PC3-6400	RegisterSpeedGrade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
20 / 16	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	1

## Register Control Bit Settings

### Types of Control Bits:

1. Reserved for future use (RFU):

These control register bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These control register bits are used by Register, DIMM or System vendors for test and characterization purposes only.

They must be programmed to zero for normal operation.

3. Card type specific (Card):

These values were used during validation of this reference design. It is recommended that systems program these register bits as defined here to ensure operation as validated. Any change from these values to match-module implementation must be verified in simulation and testing.

4. Application specific bits (A/S):

These control register bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.

## Register Control Word Setting for Raw Card Y

Register Control Word	Bit	Function	Type	Register Setting
RC0	DBA1	B outputs disabled	Card	0
	DBA0	A outputs disabled	Card	0
	DA4	Float outputs	A/S	0 or 1
	DA3	Output Inversion	Card	0
RC1	DBA1	Disable Y3_t/Y3_c clock	Card	0
	DBA0	Disable Y2_t/Y2_c clock	Card	0
	DA4	Disable Y1_t/Y1_c clock	Card	0
	DA3	Disable Y0_t/Y0_c clock	Card	0
RC2	DBA1	Frequency Band Select	Test	0
	DBA0	Input Bus Termination	A/S	0 or 1
	DA4	1T/3T Output timing	A/S	0 or 1
	DA3	Address- and command-nets prelaunch (Control Signals QxCKE, QxCS, QxODT do not apply)	Card	0
RC3	DBA1	Driver Characteristics: Command/Address Driver-B Outputs	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Command/Address Driver-A Outputs	Card	0
	DA3		Card	1
RC4	DBA1	Driver Characteristics: Control Driver-B Outputs	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Control Driver-A Outputs	Card	0
	DA3		Card	1
RC5	DBA1	Driver Characteristics: Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers	Card	0
	DA3		Card	1
RC6	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0

## Register Control Word Setting for Raw Card Y

Register Control Word	Bit	Function	Type	Register Setting
RC7	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC8	DBA1	Extended IBT settings	Card	0
	DBA0		A/S	0 or 1
	DA4		A/S	0 or 1
	DA3		A/S	0 or 1
RC9	DBA1	CKE Power Down Mode Enable	A/S	0 or 1
	DBA0	CKE Power Down Mode	A/S	0 or 1
	DA4	Reserved for Future Use	RFU	0
	DA3	Reduced Drive Mode	A/S	0 or 1
RC10	DBA1	RDIMM Operating Speed	A/S	0 or 1
	DBA0		A/S	0 or 1
	DA4		A/S	0 or 1
	DA3		A/S	0 or 1
RC11 ... RC15	DBA1	Reserved for Future Use	RFU	0
	DBA0		RFU	0
	DA4		RFU	0
	DA3		RFU	0

## Input Loading Matrix

Signal Names	Input Device	Loads
CK0_t, CK0_c	Registering Clock Driver	1
CK1_t, CK1_c	Termination Resistor	1
RESET_n	Registering Clock Driver + DDR SDRAM	1 + 36
CKE0, ODT0	Registering Clock Driver	1
CKE1, ODT1	Registering Clock Driver	1
Addr, BA, RAS_n, CAS_n, WE_n, Par_In	Registering Clock Driver	1
S0_n	Registering Clock Driver	1
S1_n	Registering Clock Driver	1
S2_n	Registering Clock Driver	1
S3_n	Registering Clock Driver	1
DQ, CB, DQS_t, DQS_c	DDR3 SDRAM	4
DM, TDQS_t, TDQS_c	DDR3 SDRAM	4
SCL, SDA, SA	EEPROM	1*
EVENT_n	Thermal sensor	1**
* When optional discrete thermal sensor is present, loading is 2.		
** When thermal sensor is not present, loading is 0.		

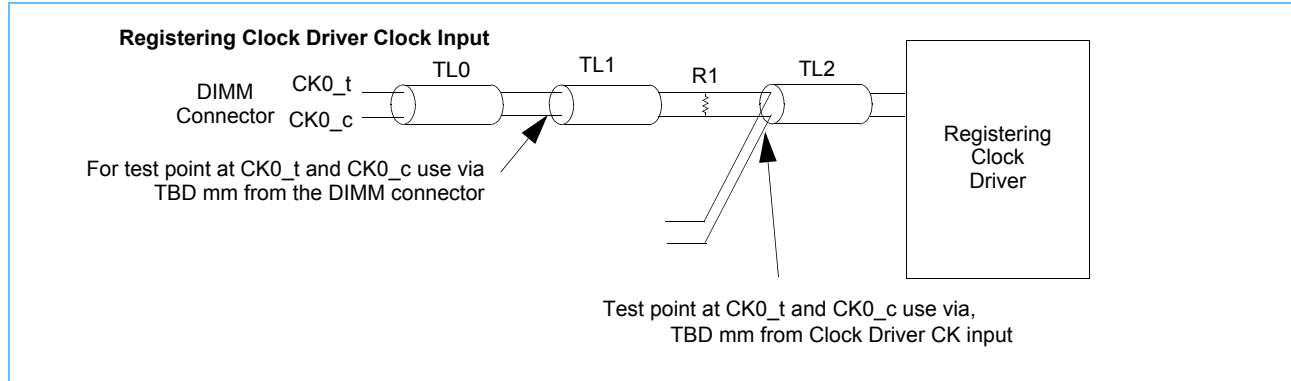
## Test Points

General test point information is defined on page 22

Signal Group	Signal Location	Available on:
Address / Command	Pre register	22 Ohm series resistors
	Post register	Termination resistors
DQ,CB		15 Ohm resistors
DQS_t, DQS_c		15 Ohm resistors
DM/TDQS_t, TDQS_c		Not valid on this raw card
Clock	Pre Clock Driver	Termination resistor near registering clock driver
	Post Clock Driver (at SDRAMs, at Register)	Termination resistors
Notes:		

## Registering Clock Driver Net Structures

### Net Structure Routing for Registering Clock Driver Input

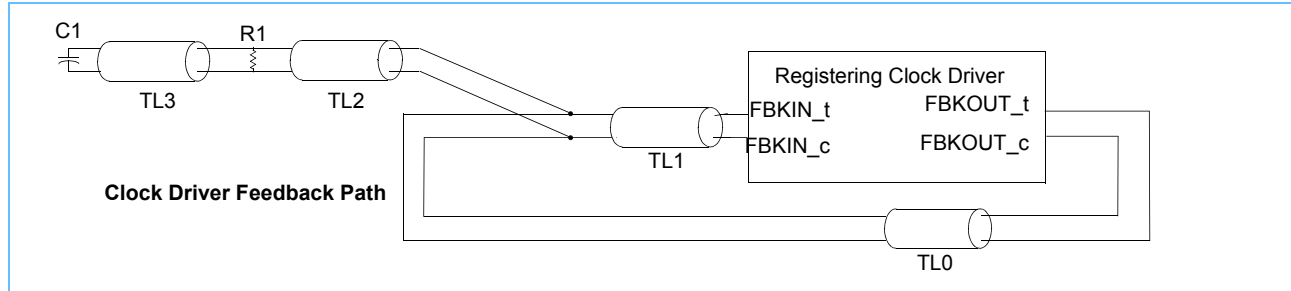


### Clock Net Lengths for Registering Clock Driver Input Net Structures

TL0		TL1		TL2		R1 (Ohms)	Notes
Min	Max	Min	Max	Min	Max		
2.4	2.5	18.8	18.9	2.4	2.5	120	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.
2.  $TL0 + TL1 + TL2 = 24.6$  to  $24.8$

### Net Structure Routing for Registering Clock Driver Feedback Path

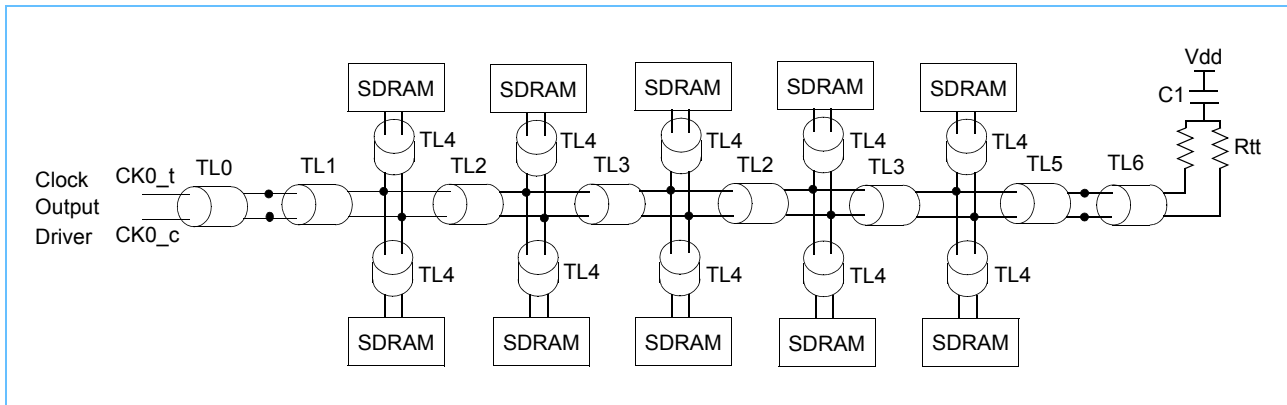


### Trace Lengths for Registering Clock Driver Feedback Path Net Structure

TL0		TL1		TL2	TL3	R1 (Ohms)	C1 (pF)	Notes
Min	Max	Min	Max					
13.4	13.6	1.5	1.7	0.8	1.0	$75 \pm 5\%$	0	1, 2, 3, 4

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.
2.  $TL0 + TL1 = 15.0 \pm 0.1$
3. All capacitances are given in pF and must be kept within a tolerance of  $\pm 10\%$ .
4. The termination resistor and loading capacitor are both placed as close to the pin of the Clock Driver as possible.

### Net Structure Routing for Clock Driver Output to SDRAM Load - DIMM Left Side

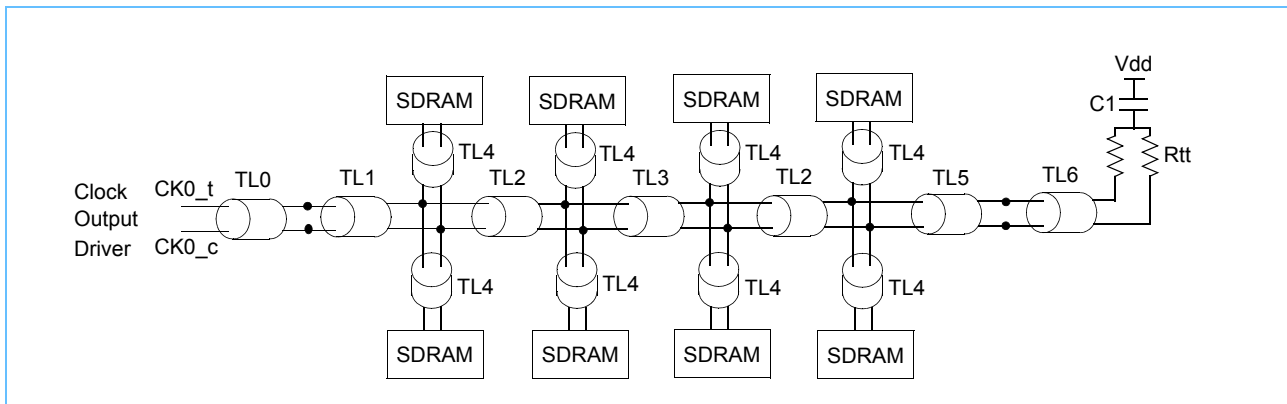


### Trace Lengths for Clock Driver Output to SDRAM load Net Structures

TL0		TL1		TL2		TL3		TL4		TL5 + TL6		Rtt (Ohms)	C1(uF)	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
0.7	3.1	19.1	21.7	12.4	12.6	12.4	12.6	2.9	3.0	11.8	12.0	27 ± 5%	0.1	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL0 + TL1 = 22.2 to 22.4

### Net Structure Routing for Clock Driver Output to SDRAM Load - DIMM Right Side

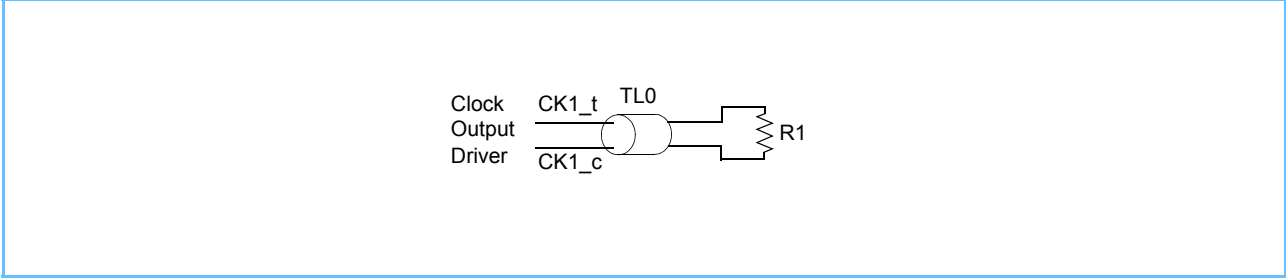


### Trace Lengths for Clock Driver Output to SDRAM load Net Structures

TL0		TL1		TL2		TL3		TL4		TL5 + TL6		Rtt (Ohms)	C1(uF)	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
0.7	3.9	18.3	21.7	12.4	12.6	12.4	12.6	2.9	3.0	11.8	12.0	27 ± 5%	0.1	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL0 + TL1 = 22.2 to 22.4

**Net Structure Routing for Clock Driver Output to DIMM Termination**



**Trace Lengths for Clock Driver Output to DIMM Termination Net Structures**

TL0		R1 (Ohms)	Notes
Min	Max		
4.0	4.1	120 ± 5%	1

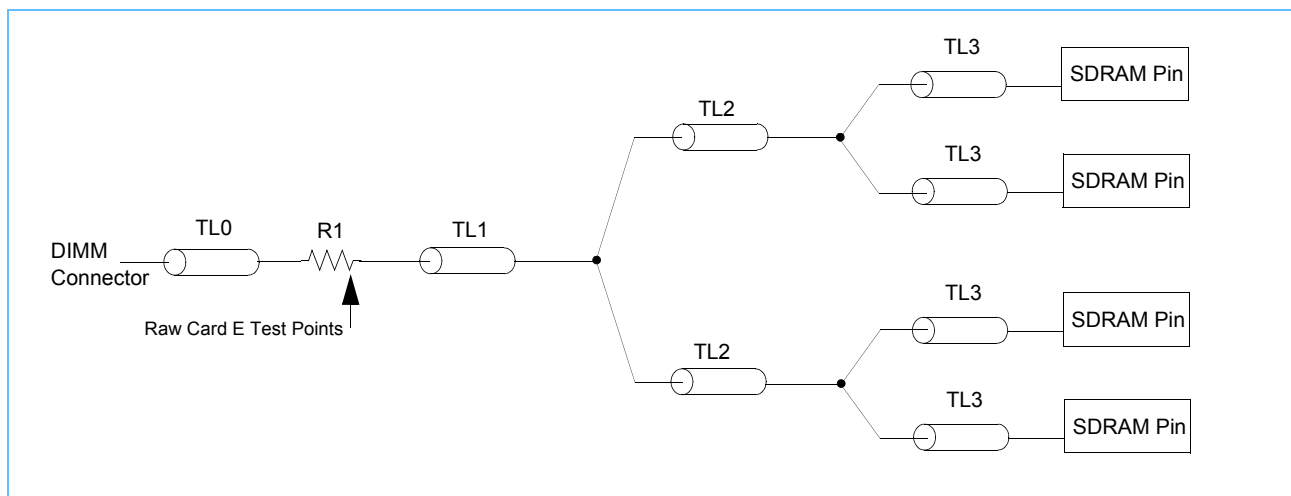
1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

## Data Net Structures

### DQ[63:0], CB[7:0], DQS[8:0]\_t, DQS[8:0]\_c, DM[8:0]/TDQS[17:9]\_t, TDQS[17:9]\_c

Special attention has been paid to balancing data nets (including Check Bits) within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend delays for all nets, as described in the following tables.

### Net Structure Routing for DQ[63:0], CB[7:0], DQS[17:0]\_t, DQS[17:0]\_c, DM[8:0]/TDQS[17:9]\_t, TDQS[17:9]\_c



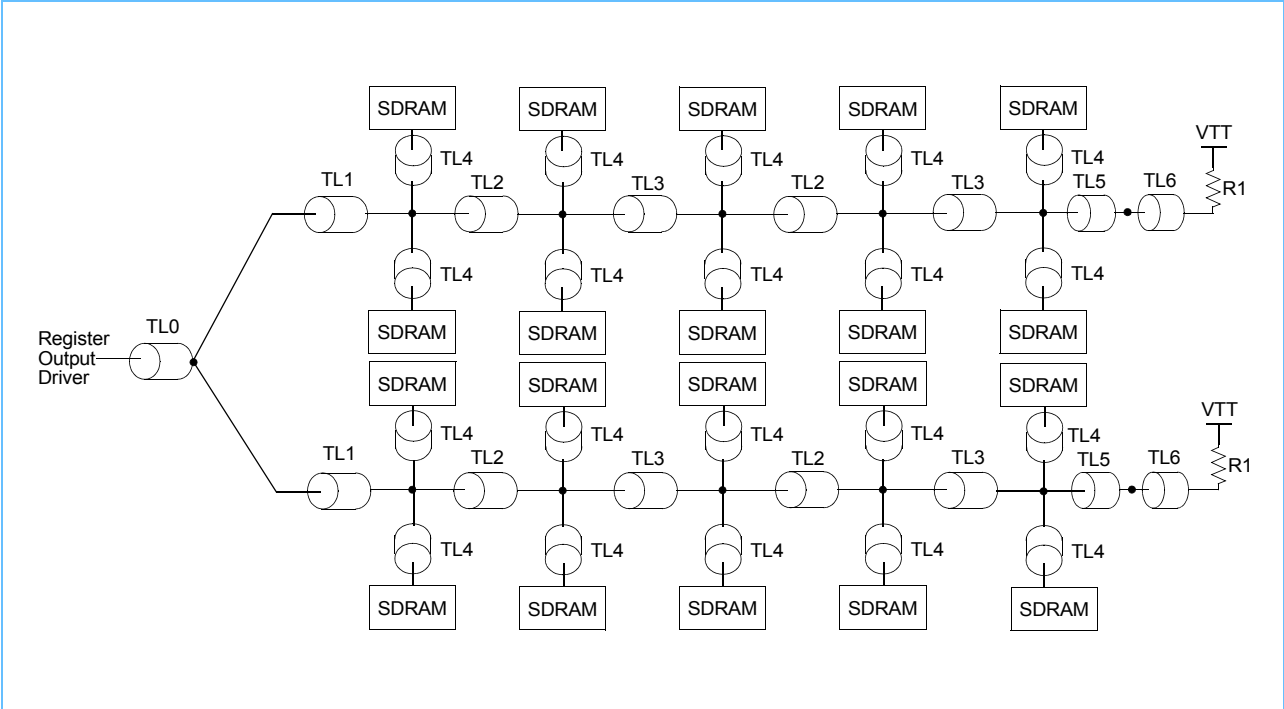
### Trace Lengths of DQ[63:0], CB[7:0], DQS[17:0]\_t, DQS[17:0]\_c, DM[8:0]/TDQS[17:9]\_t, TDQS[17:9]\_c for R/C Y0

	TL0		TL1		TL2		TL3		TL0 + TL1 + TL2 + TL3		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQ0-7, DQS0_t, DQS0_c, DM0/TDQS9, DQS9_c	3.7	6.6	12.7	15.8	2.6	4.6	0.5	2.6	25.2	25.6	15 ± 5%	1
DQ8-15, DQS1_t, DQS1_c, DM1/TDQS10, DQS10_c	3.3	5.4	12.4	14.7	2.6	4.6	0.5	2.6	24.1	24.3	15 ± 5%	1
DQ16-23, DQS2_t, DQS2_c, DM2/TDQS11, DQS11_c	3.3	4.7	15.1	16.5	2.6	4.6	0.5	2.6	25.9	26.1	5 ± 5%	1
DQ24-31, DQS3_t, DQS3_c, DM3/TDQS12, DQS12_c	3.3	4.2	20.0	20.9	2.6	4.6	0.5	2.6	30.1	30.3	5 ± 5%	1
CB0-CB7, DQS8_t, DQS8_c, DM8/TDQS17, DQS17_c	3.3	4.9	20.0	21.4	2.6	4.6	0.5	2.6	30.6	30.9	15 ± 5%	1
DQ32-39, DQS4_t, DQS4_c, DM4/TDQS13, DQS13_c	3.3	5.0	18.1	19.6	2.6	4.6	0.5	2.6	29.0	29.2	15 ± 5%	1
DQ40-47, DQS5_t, DQS5_c, DM5/TDQS14, DQS14_c	3.2	5.1	15.8	17.7	2.6	4.6	0.5	2.6	26.8	26.9	15 ± 5%	1
DQ48-55, DQS6_t, DQS6_c, DM6/TDQS15, DQS15_c	3.2	4.3	13.8	15.0	2.6	4.6	0.5	2.6	24.1	24.3	5 ± 5%	1
DQ56-63, DQS7_t, DQS7_c, DM7/TDQS16, DQS16_c	3.2	4.7	13.4	15.2	2.6	4.6	0.5	2.6	24.2	24.6	5 ± 5%	1

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

# Post Register Address and Command Net Structure Routing - DIMM Left Side

A[15:0], BA[2:0], RAS\_n, CAS\_n, WE\_n



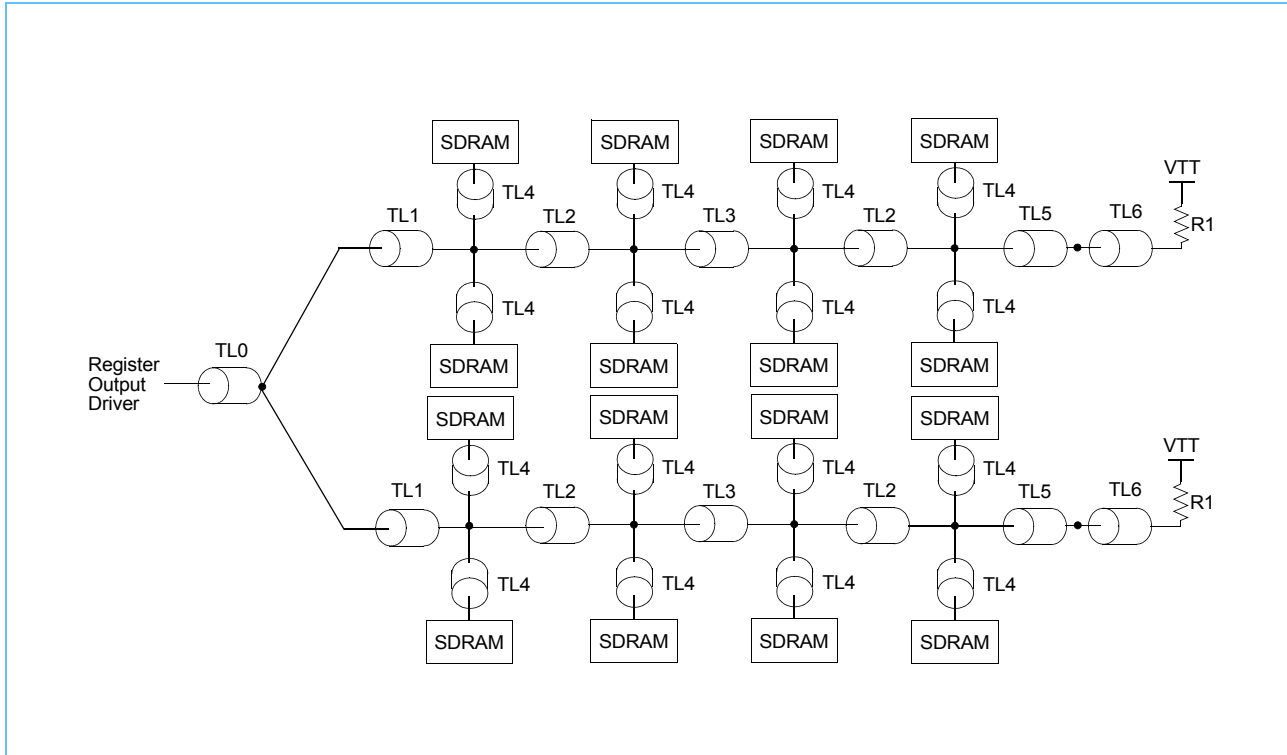
## Trace Lengths for Post Register of Address and Command Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 (Ohms)	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
0.9	5.5	16.7	21.5	12.4	12.6	12.4	12.6	1.5	3.0	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.  
2. TL0 + TL1 = 22.2 to 22.4

## Post Register Address and Command Net Structure Routing - DIMM Right Side

A[15:0], BA[2:0], RAS<sub>n</sub>, CAS<sub>n</sub>, WE<sub>n</sub>



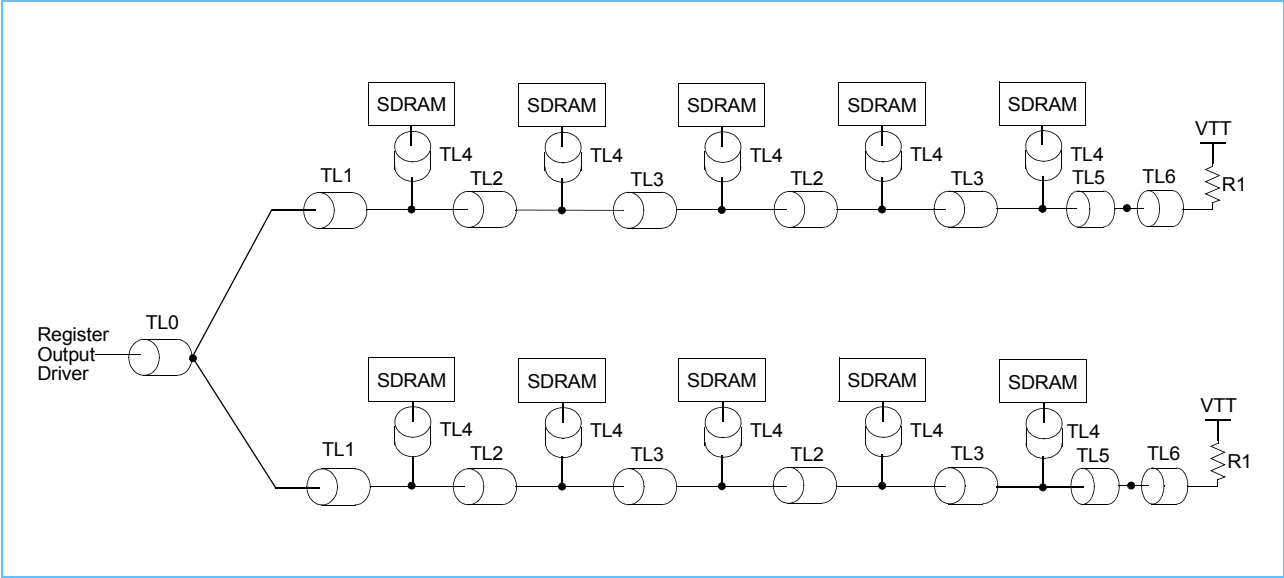
### Trace Lengths for Post Register of Address and Command Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 (Ohms)	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
0.9	5.7	16.5	21.5	12.4	12.6	12.4	12.6	1.5	3.0	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.  
2. TL0 + TL1 = 22.2 to 22.4

### Post Register Control Net Structure Routing - DIMM Left Side

CKE[1:0]



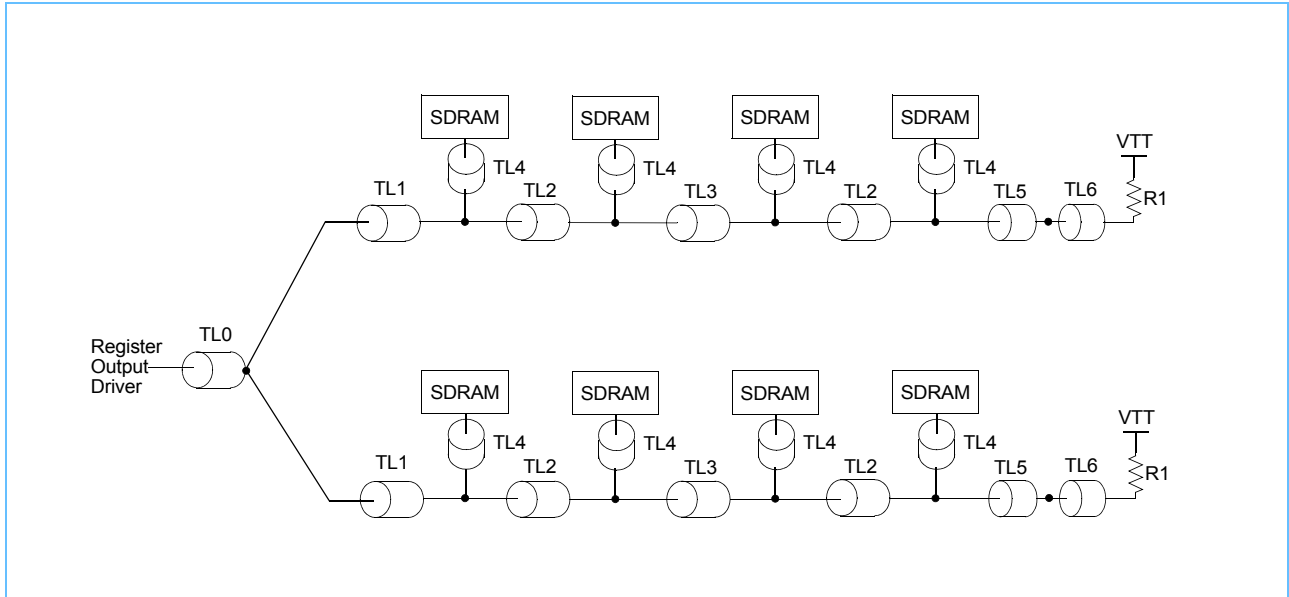
### Trace Lengths for Post Register of Control Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
4.0	5.8	16.4	18.4	17.9	18.1	17.9	18.1	2.8	3.0	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL0 + TL1 = 22.2 mm to 22.4 mm

## Post Register Control Net Structure Routing - DIMM Right Side

CKE[1:0]



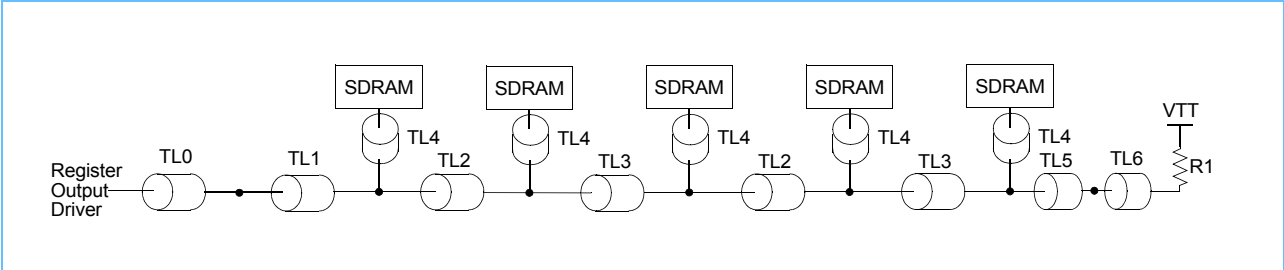
### Trace Lengths for Post Register of Control Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
4.7	5.1	17.1	17.7	17.9	18.1	17.9	18.1	2.8	3.0	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.
2.  $TL0 + TL1 = 22.2$  mm to  $22.4$  mm

## Post Register Control Net Structure Routing - DIMM Left Side

ODT[1:0]



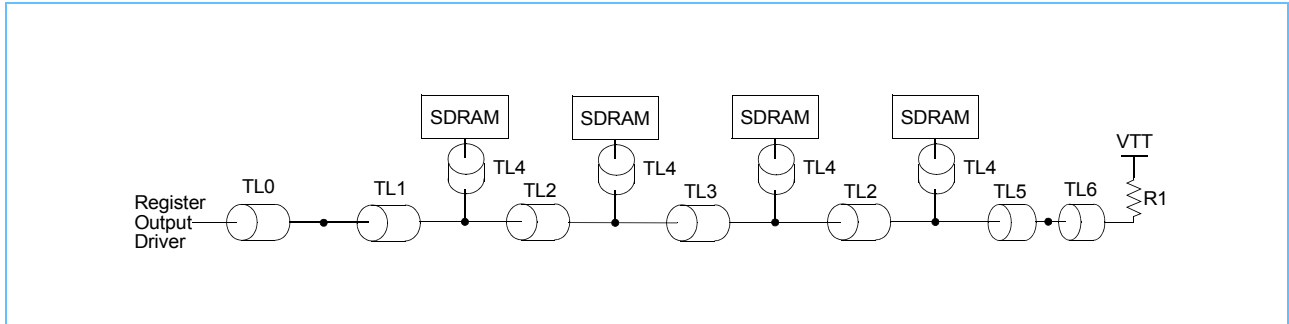
### Trace Lengths for Post Register of Control Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
5.5	6.0	16.2	16.9	16.9	17.1	16.9	17.1	2.3	2.4	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.  
2. TL0 + TL1 = 22.2 mm to 22.4 mm

## Post Register Control Net Structure Routing - DIMM Right Side

ODT[1:0]



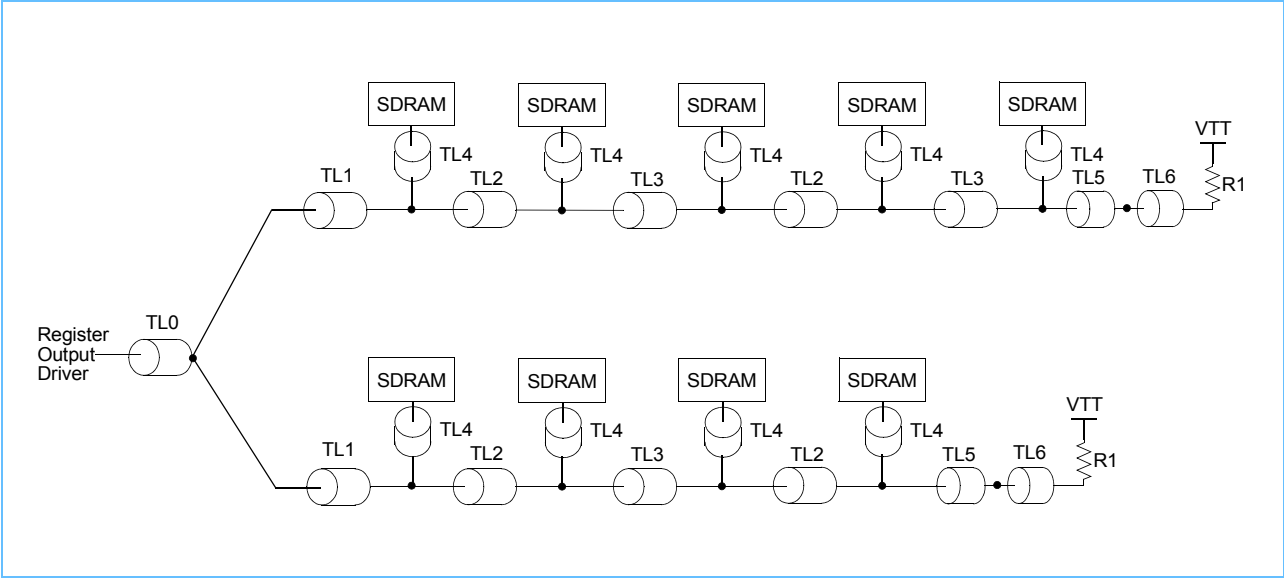
### Trace Lengths for Post Register of Control Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
5.6	5.7	16.5	16.8	16.9	17.1	16.9	17.1	2.4	3.0	9.9	10.1	36 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.
2.  $TL0 + TL1 = 22.2$  mm to  $22.4$  mm

# Post Register Control Net Structure Routing

CS3:0]



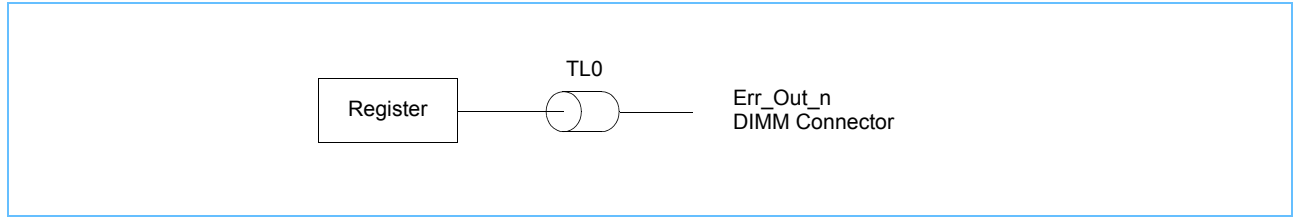
## Trace Lengths for Post Register of Control Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1.2	1.4	24.0	24.4	15.4	15.6	15.4	15.6	1.6	2.8	9.9	10.1	27 ± 5%	1, 2

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL0 + TL1 = 25.4 mm to 25.6 mm

## Address and Command Parity Net Structures

### Net Structure Routing for Address and Command Parity



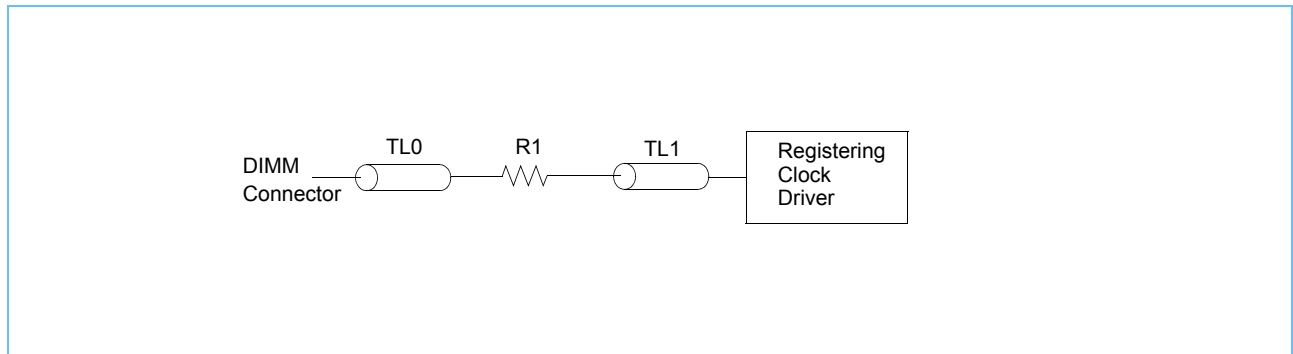
### Trace Lengths for Address and Command Parity Net Structure

TL0		Notes
Min	Max	
31.5	31.5	1

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.

## Net Structure Routing for Pre Register of Address, Command, Control and Address/Command Parity

A[15:0], BA[2:0], RAS\_n, CAS\_n, WE\_n, S[3:0]\_n, CKE[1:0], ODT[1:0], Par\_in



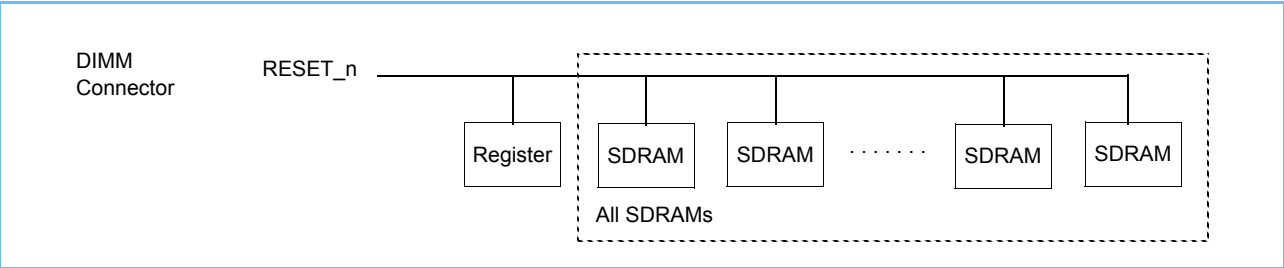
### Trace Lengths for Pre Register of Address, Command, Control and Address/Command Parity

A[15:0], BA[2:0], RAS\_n, CAS\_n, WE\_n, S[1:0]\_n, CKE[1:0], ODT[1:0], Par\_in

TL0		TL1		TL0 + TL1		R1 (Ohms)	Notes
Min	Max	Min	Max	Min	Max		
2.3	4.0	20.2	22.5	24.6	24.8	22 $\pm$ 5%	1

1. All distances are given in millimeters and must be kept within a tolerance of  $\pm 0.8$  millimeter.

## RESET\_n Net Structures



## RESET\_n Net Total Length

Total Net Length
377 mm

Note: Net is wired with 0.1 mm width; only the total length all traces together (in millimeters) is specified and must be kept within a tolerance of  $\pm 10\%$

## Cross Section Recommendations

Most DIMM printed circuit board designs use six layers of glass epoxy material. PCBs should contain solid ground plane and power plane layers as far as possible..

Any exceptions to these design rules will be indentified in the appendix for that raw card.

**Note:** The PCB edge connector contacts shall be gold-plated.

## PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers, 0.075 mm wide single trace)	5.5	6.7	ps/mm
Trace velocity: S0 (inner layers, 0.075 mm wide single trace)	6.5	7.6	ps/mm
Trace impedance: $Z_0$ (all layers, 0.075 mm wide single trace)	54	66	Ohms

## Example Twelve Layer Stackup

