

Annex AB - Raw Card AB

DDR3 Registered DIMM Design File

Specification Revision	Applicable Design File	Applicable BOM
0.10	PC3-RDIMM_V010_RC-AB0_20081201.brd	PC3-RDIMM_V010_RC-AB0_20081201_BOM.txt
0.83	PC3-RDIMM_V083_RC_AB1_20100329.brd	PC3-RDIMM_V083_RC_AB1_20090623_BOM.txt

NOTE "Reference" design file updates will be released as needed. This Registered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated.

Module Configuration

DIMM		SDRAM		# of SDRAMs	# of Physical Ranks	# of Address bits row/col/Bank	MO-269 variation
Capacity	Organization	Density	Organization				
4GB	512Mx72	512Mbit	128Mx4	72	4	13/11/3	AB
8GB	1Gx72	1Gbit	256Mx4	72	4	14/11/3	AB
16GB	2Gx72	2Gbit	512Mx4	72	4	15/11/3	AB
32GB	4Gx72	4Gbit	1Gx4	72	4	16/11/3	AB
64GB	8GX72	8Gbit	2Gx4	72	4	16/12/3	AB

SDRAM Configuration

Supported DRAM Outline (Width x Length) max.	# of Banks in SDRAM	SDRAM Package Type	SDRAM Organization	MO-207 variation
11.0 mm x 11.5 mm	8	78 Ball stacked FBGA	x4, stacked, double row	DT-z

Supported Speeds

Registration	Voltage	PC3-6400	PC3-8500	PC3-10600	PC3-12800	Notes
AB0	DDR3	X	X			2, 3
	DDR3L					2, 3
	DDR3U					2, 3
AB1	DDR3	X	X	X		1, 2, 3
	DDR3L					
	DDR3U					

NOTE 1 50% Recessed GND

NOTE 2 X will reflect passed committee ballot at the time when specification is issued at BOD ballot

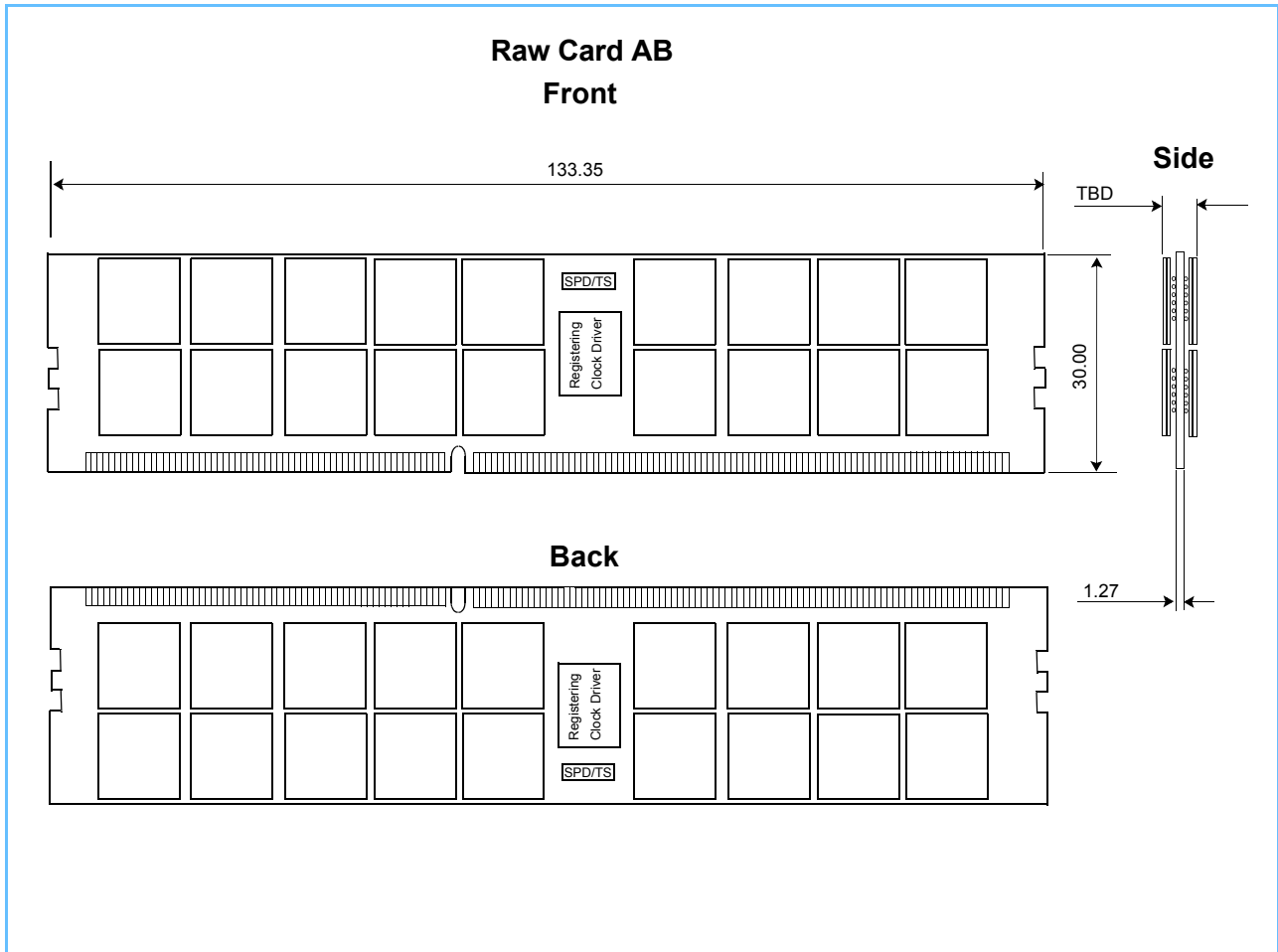
NOTE 3 P means the proposed speed for committee ballot

Design Rules and Deviations

1. 0201 capacitors and resistors are used in this design.
2. Blind vias are used in this design.

General Layout

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs)



NOTE 1 All dimensions are typical unless otherwise stated. (Millimeters)

NOTE 2 Thermal sensor is placed within the thermal sensor placement area as defined in MO-269.

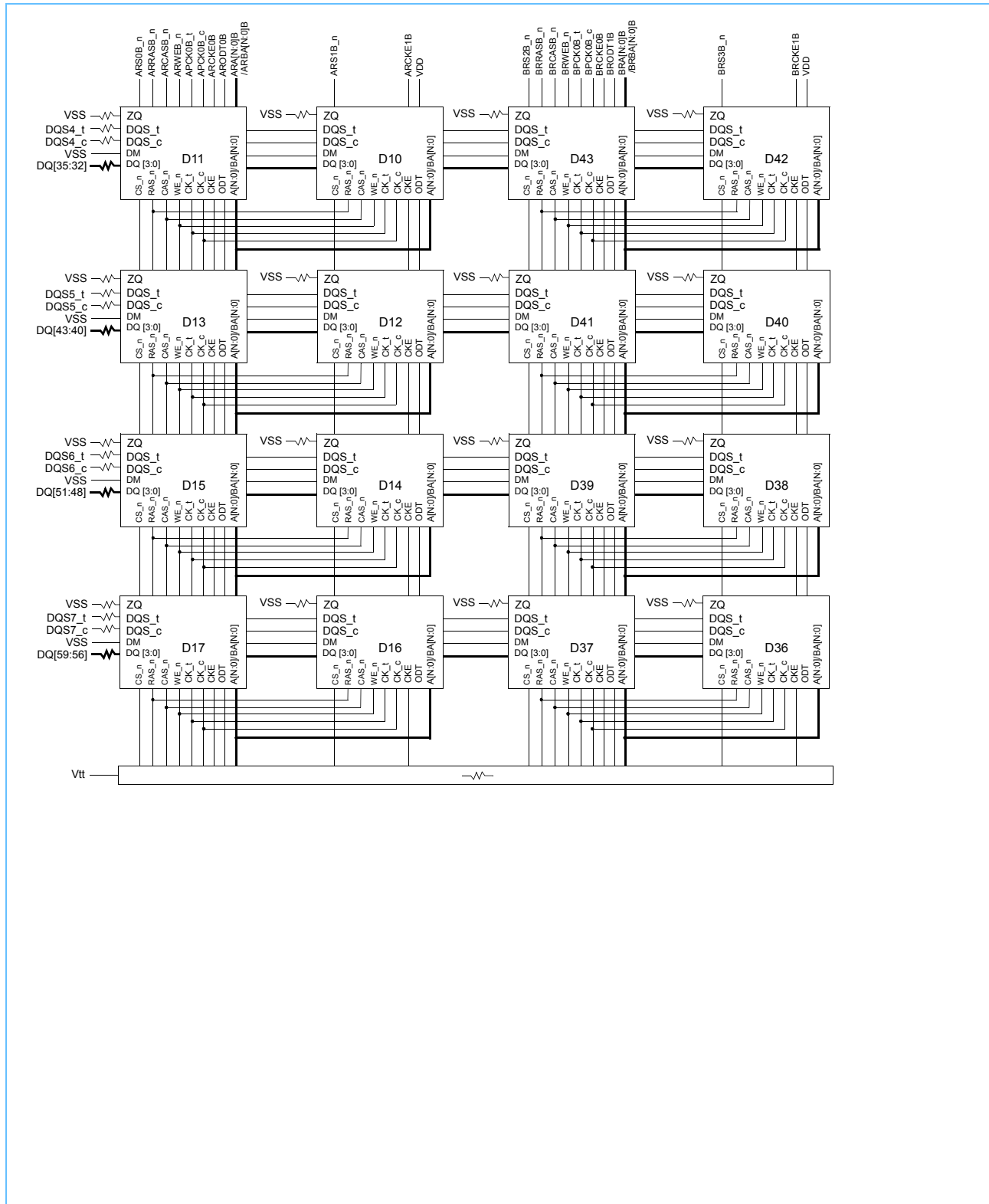
NOTE 3 Registering clock driver is placed within the Register Placement Area as defined in MO-269.

NOTE 4 Implementation and dimensions shown without heat spreader.

NOTE 5 In the event that a heat spreader is added to this module, module thickness would increase. Please refer to MO-269 for dimensions of specific variations with heat spreader attached.

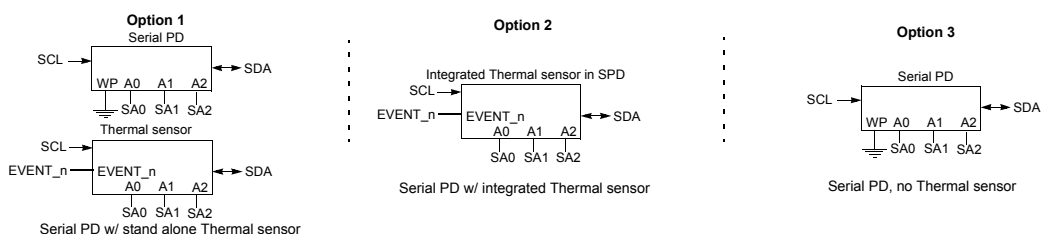
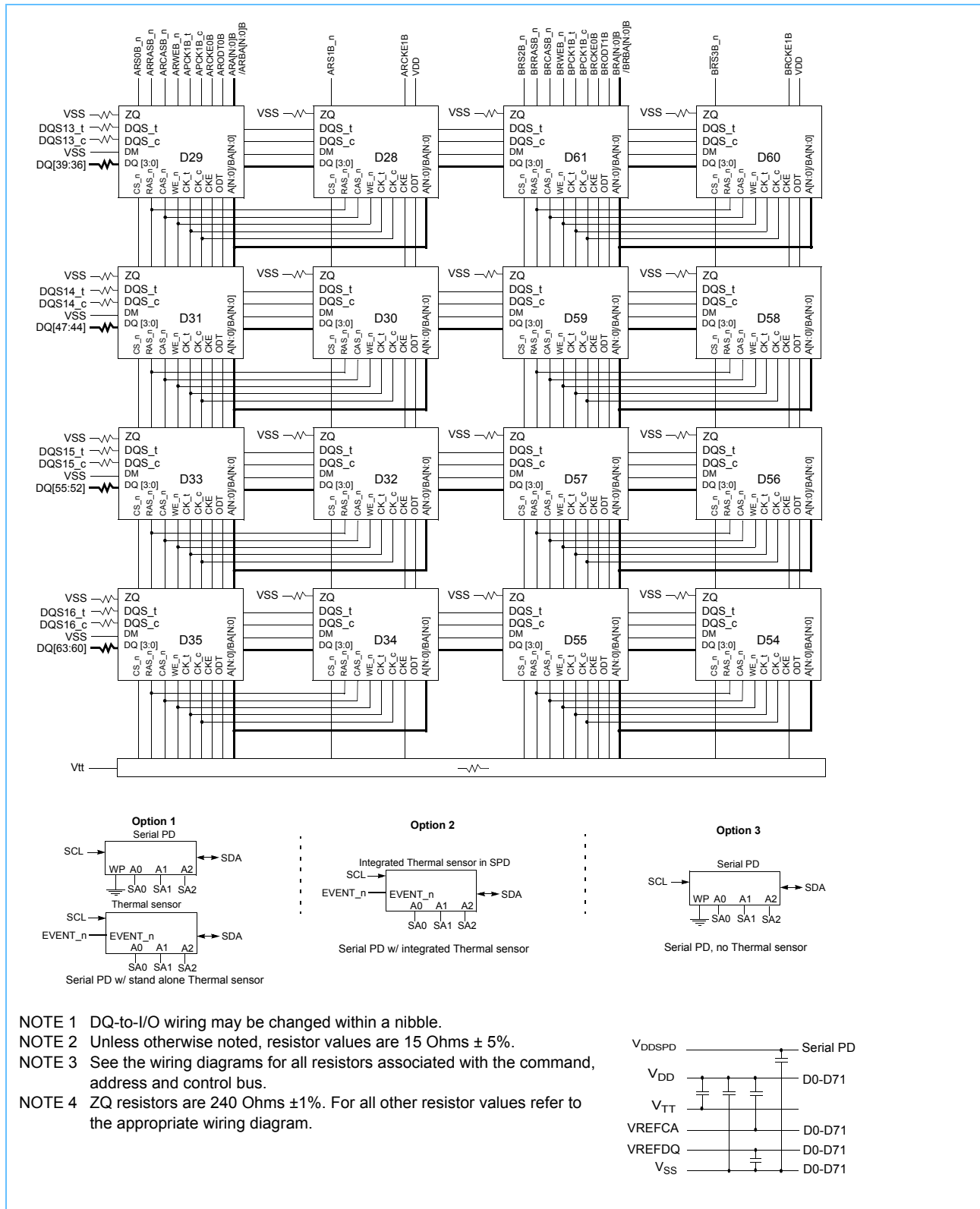
Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 4 of 5)

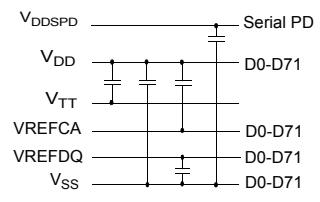


Block Diagram

x72 DIMM, populated as four physical ranks of x4 stacked DDR3 SDRAMs (part 5 of 5)



- NOTE 1 DQ-to-I/O wiring may be changed within a nibble.
- NOTE 2 Unless otherwise noted, resistor values are 15 Ohms \pm 5%.
- NOTE 3 See the wiring diagrams for all resistors associated with the command, address and control bus.
- NOTE 4 ZQ resistors are 240 Ohms \pm 1%. For all other resistor values refer to the appropriate wiring diagram.



Registering Clock Driver

Please refer to the register vendor data sheets for all technical specifications and requirements.

Component Specifications

DRAMs per output	Register Type	RegisterSpeedGrade PC3-6400	RegisterSpeedGrade PC3-8500	Register Speed Grade PC3-10600	Register Speed Grade PC3-12800	Quantity
20 / 16	1:2 28-bit 1.5V	SSTE32882	SSTE32882	SSTE32882	SSTE32882	2

Register Control Bit Settings

Types of Control Bits:

1. Reserved for future use (RFU):

These bits must be programmed to zero for all raw cards that have been developed/manufactured before this “future use” was defined.

2. Test bits (Test):

These bits are used by Register, DIMM or System vendors for test and characterization purposes only. They must be programmed to zero for normal operation

3. Card type specific (Card):

These bits have to be programmed to a certain value based on the raw card. The values are given in the table. These bits will be defined and balloted during the raw card development. DIMM is only guaranteed to work with those bits set appropriately. (highlighted in green)

4. Application specific bits (A/S):

These bits are freely programmable by the user based on the actual system configuration in which this DIMM is used.

Register Control Word	Bit	Function	Type	Register Settings
RC0	DBA1	B outputs disabled	Card	0
	DBA0	A outputs disabled	Card	0
	DA4	Float outputs	A/S	0 or 1
	DA3	Output Inversion	Card	0
RC1	DBA1	Disable Y3_t/Y3_c clock	Card	0
	DBA0	Disable Y2_t/Y2_c clock	Card	0
	DA4	Disable Y1_t/Y1_c clock	Card	0
	DA3	Disable Y0_t/Y0_c clock	Card	0
RC2	DBA1	Frequency Band Select	Test	0
	DBA0	Input Bus Termination	A/S	“0” or “1”
	DA4	1T/3T Output timing	A/S	“0” or “1”
	DA3	Address- and command-nets prelaunch (Control Signals QxCKE, QxCS, QxODT do not apply)	Card	0

Register Control Word	Bit	Function	Type	Register Settings
RC3	DBA1	Driver Characteristics: Command/Address Driver-B Outputs	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Command/Address Driver-A Outputs	Card	0
	DA3		Card	1
RC4	DBA1	Driver Characteristics: Control Driver-B Outputs	Card	0
	DBA0		Card	0
	DA4	Driver Characteristics: Control Driver-A Outputs	Card	0
	DA3		Card	0
RC5	DBA1	Driver Characteristics: Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers	Card	0
	DBA0		Card	1
	DA4	Driver Characteristics: Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers	Card	0
	DA3		Card	1
RC6	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC7	DBA1	Reserved, free to use by register vendor	Test	0
	DBA0		Test	0
	DA4		Test	0
	DA3		Test	0
RC8	DBA1	Extended IBT settings	Card	1
	DBA0		A/S	0 or 1
	DA4		A/S	0 or 1
	DA3		A/S	0 or 1
RC9	DBA1	CKE Power Down Mode Enable	A/S	0 or 1
	DBA0	CKE Power Down Mode	A/S	0 or 1
	DA4	Reserved for Future Use	RFU	0
	DA3	Reduced Drive Mode	A/S	0 or 1
RC10	DBA1	RDIMM Operating Speed	A/S	0 or 1
	DBA0		A/S	0 or 1
	DA4		A/S	0 or 1
	DA3		A/S	0 or 1

Register Control Word	Bit	Function	Type	Register Settings
RC11 ... RC15	DBA1	Reserved for Future Use	RFU	0
	DBA0		RFU	0
	DA4		RFU	0
	DA3		RFU	0

Input Loading Matrix

Signal Names	Input Device	Loads
CK0_t, CK0_c	Registering Clock Driver	2
CK1_t, CK1_c	Termination Resistor	1
RESET_n	Registering Clock Driver + DDR3 SDRAM	2 + 72
CKE0	Registering Clock Driver	2
ODT0	Registering Clock Driver	1
CKE1	Registering Clock Driver	2
ODT1	Registering Clock Driver	1
Addr, BA, RAS_n, CAS_n, WE_n, Par_In	Registering Clock Driver	2
S0_n	Registering Clock Driver	1
S1_n	Registering Clock Driver	1
S2_n	Registering Clock Driver	1
S3_n	Registering Clock Driver	1
DQ, CB, DQS_t, DQS_c	DDR3 SDRAM	4
DM, TDQS_t, TDQS_c	DDR3 SDRAM	N/A
SCL,SDA,SA	EEPROM	1*
EVENT_n	Thermal sensor	1**
*When optional discrete thermal sensor is present the load is 2.		
**When optional discrete thermal sensor is not present the load is 0.		

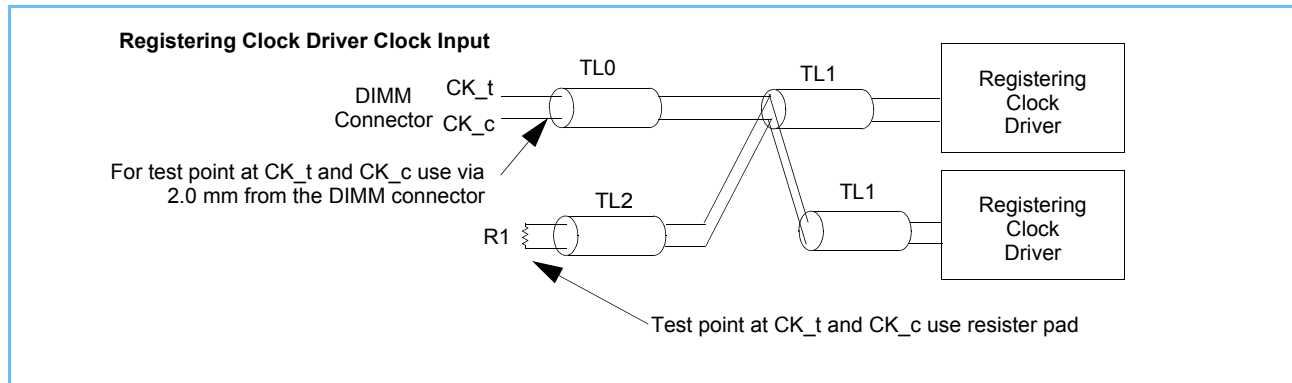
Test Points

General test point information is defined on page 4.20.20-28.

Signal Group	Signal Location	Available on
Address / Command	Pre register	22 Ohm series resistors
	Post register	Termination resistors
DQ,CB		15 Ohm resistors
DQS_t, DQS_c		15 Ohm resistors
DM		Not valid on this raw card
Clock	Pre Clock Driver	Termination resistor near registering clock driver
	Post Clock Driver (at SDRAMs, at Register)	Termination resistors
Notes:		

Registering Clock Driver Net Structures

Net Structure Routing of Registering Clock Driver Input

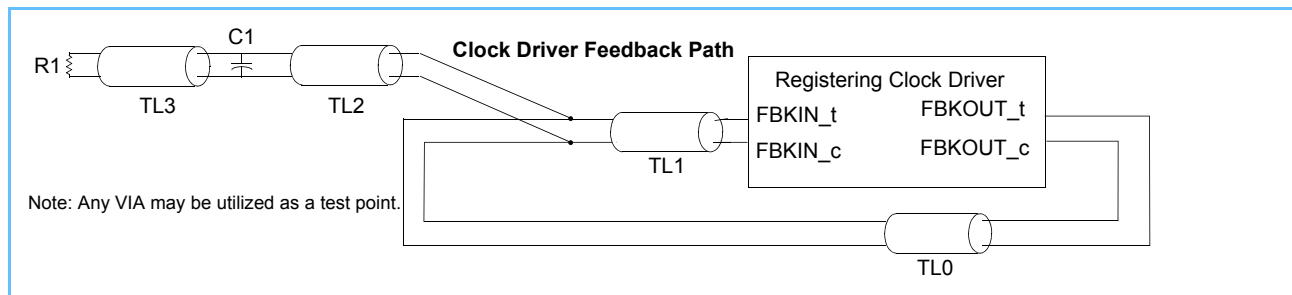


Clock Net Lengths of Registering Clock Driver Input Net Structures

TL0		TL1		TL2		R1 (Ohms)	Notes
Min	Max	Min	Max	Min	Max		
21.5	21.6	1.5	1.6	1.1	1.2	120 ± 5%	1

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Net Structure Routing of Registering Clock Driver Feedback Path



Trace Lengths of Registering Clock Driver Feedback Path Net Structure

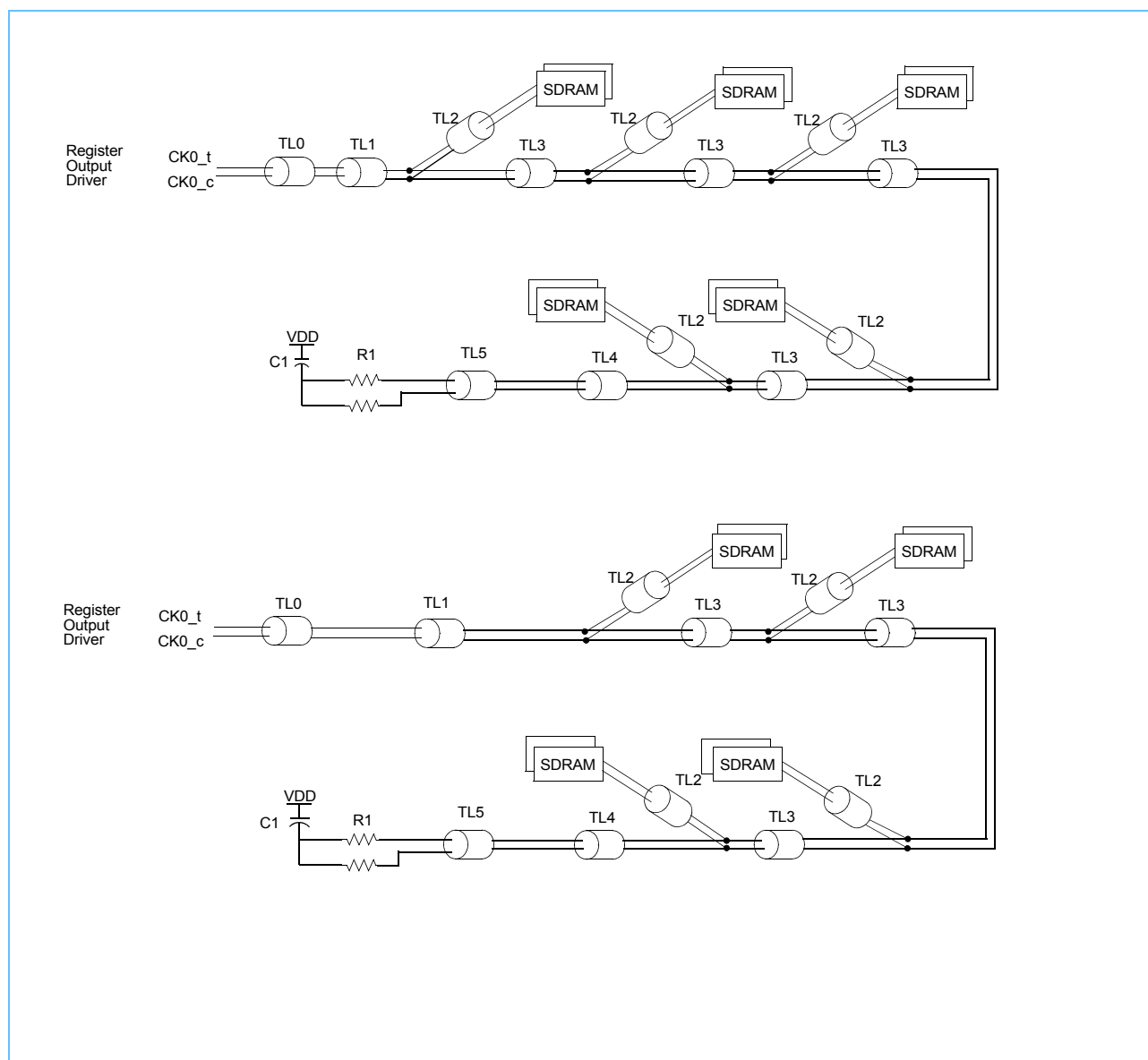
TL0		TL1		TL2		TL3	R1 (Ohms)	C1 (pF)	Notes
Min	Max	Min	Max	Min	Max				
13.4	13.5	1.5	1.6	2.3	2.8	1.0	75 ± 5%	0	1, 2, 3

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

NOTE 2 TL0 + TL1 = 15.0 mm ± 0.1 mm

NOTE 3 All capacitances are given in pF and must be kept within a tolerance of ± 10%.

Net Structure Routing of Clock Driver Output to SDRAM Load



Trace Lengths of Clock Driver Output to SDRAM load Net Structures

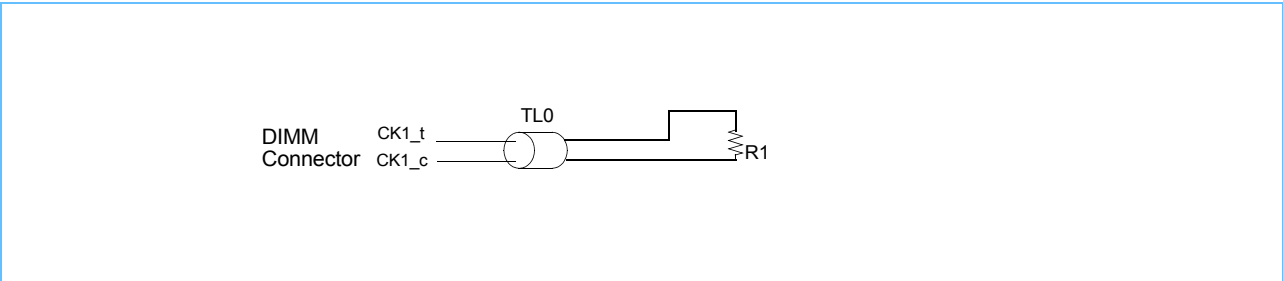
TL0		TL1		TL2		TL3		TL4		TL5		First DRAM		Last DRAM		R1 (Ohms)	C1 (uF)	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
0.7	1.5	18.3	18.3	3.2	3.2	12.8	14.0	7.3	8.1	0.7	0.7	22.2	23.0	74.6	75.4	30 ± 5%	0.1	1, 2, 3

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

NOTE 2 $TL0 + TL1 = 19.4 \text{ mm} \pm 0.4 \text{ mm}$

NOTE 3 First DRAM = $TL0 + TL1 + TL2$, Last DRAM = $TL0 + TL1 + TL2 + 4 \times TL3$

Net Structure Routing for Unused Clock Termination on DIMM



Trace Lengths of Unused Clock Termination on DIMM Net Structures

TL0		R1 Ohms	Notes
Min	Max		
3.3	3.5	120 ± 5%	1

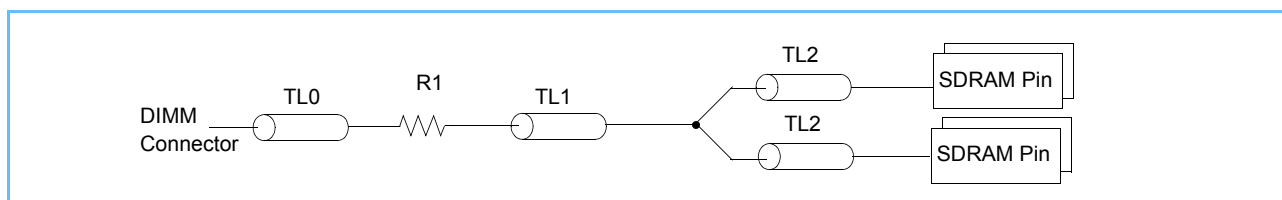
NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Data Net Structures

DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c

Special attention has been paid to balancing data nets (including Check Bits) within a DDR3 SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend delays for all nets, as described in the following tables.

Net Structure Routing of DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c



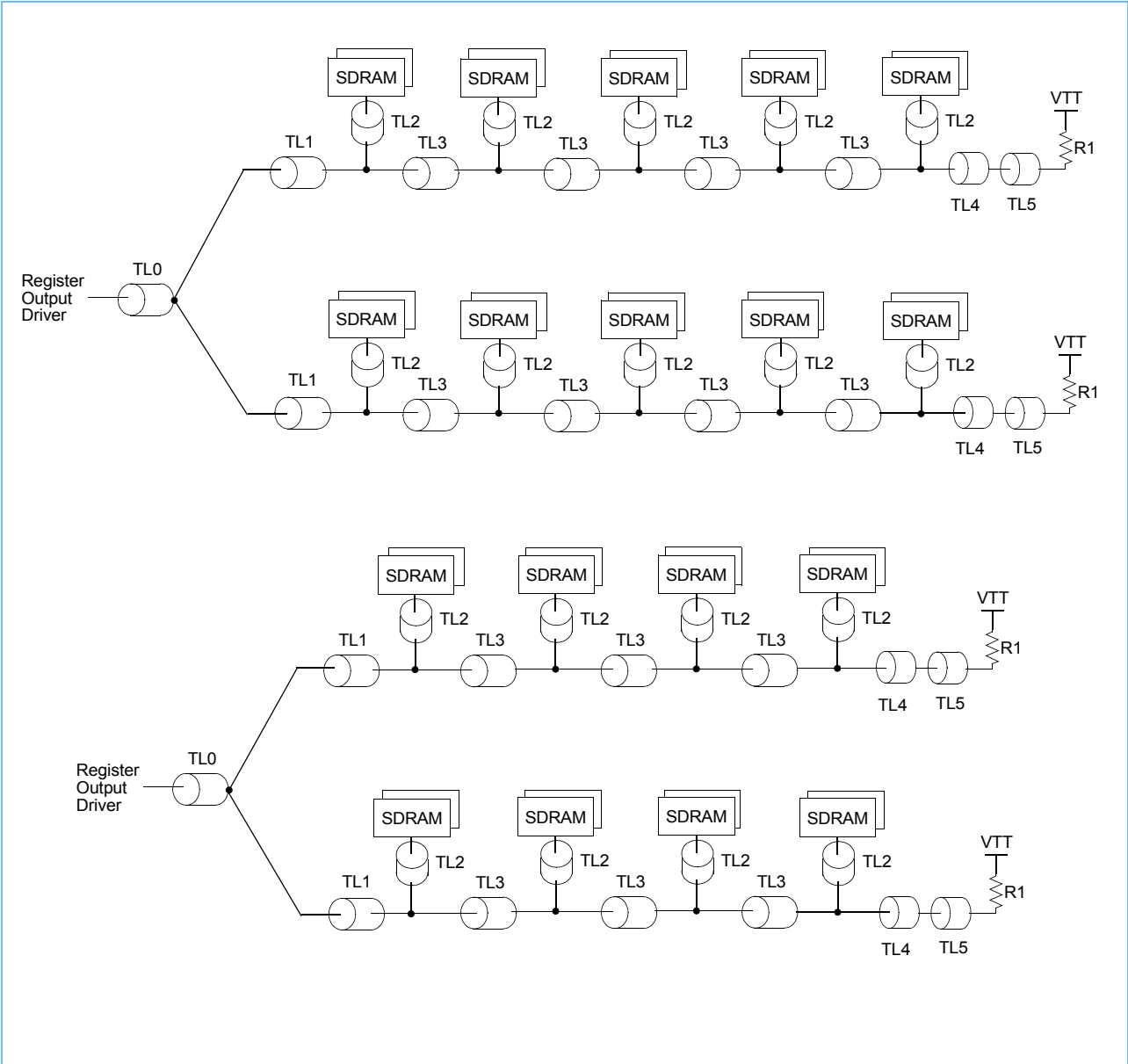
Trace Lengths of DQ[63:0], CB[7:0], DQS[17:0]_t, DQS[17:0]_c

	TL0		TL1		TL2		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max		
DQ0-7, DQS0_t, DQS0_c, DQS9_t, DQS9_c	2.8	3.5	18.3	20.0	0.5	2.3	15 ± 5 %	1
DQ8-15, DQS1_t, DQS1_c, DQS10_t, DQS10_c	2.8	3.5	18.7	20.4	0.5	2.3	15 ± 5 %	1
DQ16-23, DQS2_t, DQS2_c, DQS11_t, DQS11_c	2.8	3.5	20.4	22.1	0.5	2.3	15 ± 5 %	1
DQ24-31, DQS3_t, DQS3_c, DQS12_t, DQS12_c	2.8	3.5	21.6	23.4	0.5	2.3	15 ± 5 %	1
DQ32-39, DQS4_t, DQS4_c, DQS13_t, DQS13_c	2.8	3.5	22.1	23.9	0.5	2.3	15 ± 5 %	1
DQ40-47, DQS5_t, DQS5_c, DQS14_t, DQS14_c	2.8	3.5	20.3	22.1	0.5	2.3	15 ± 5 %	1
DQ48-55, DQS6_t, DQS6_c, DQS15_t, DQS15_c	2.8	3.5	20.5	22.3	0.5	2.3	15 ± 5 %	1
DQ56-63, DQS7_t, DQS7_c, DQS16_t, DQS16_c	2.8	3.5	21.0	22.9	0.5	2.3	15 ± 5 %	1
CB0-7, DQS8_t, DQS8_c, DQS17_t, DQS17_c	2.8	3.5	24.2	25.9	0.5	2.3	15 ± 5 %	1

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Post Register Address and Command Net Structures

A[15:0], BA[2:0], RAS_n, CAS_n, WE_n



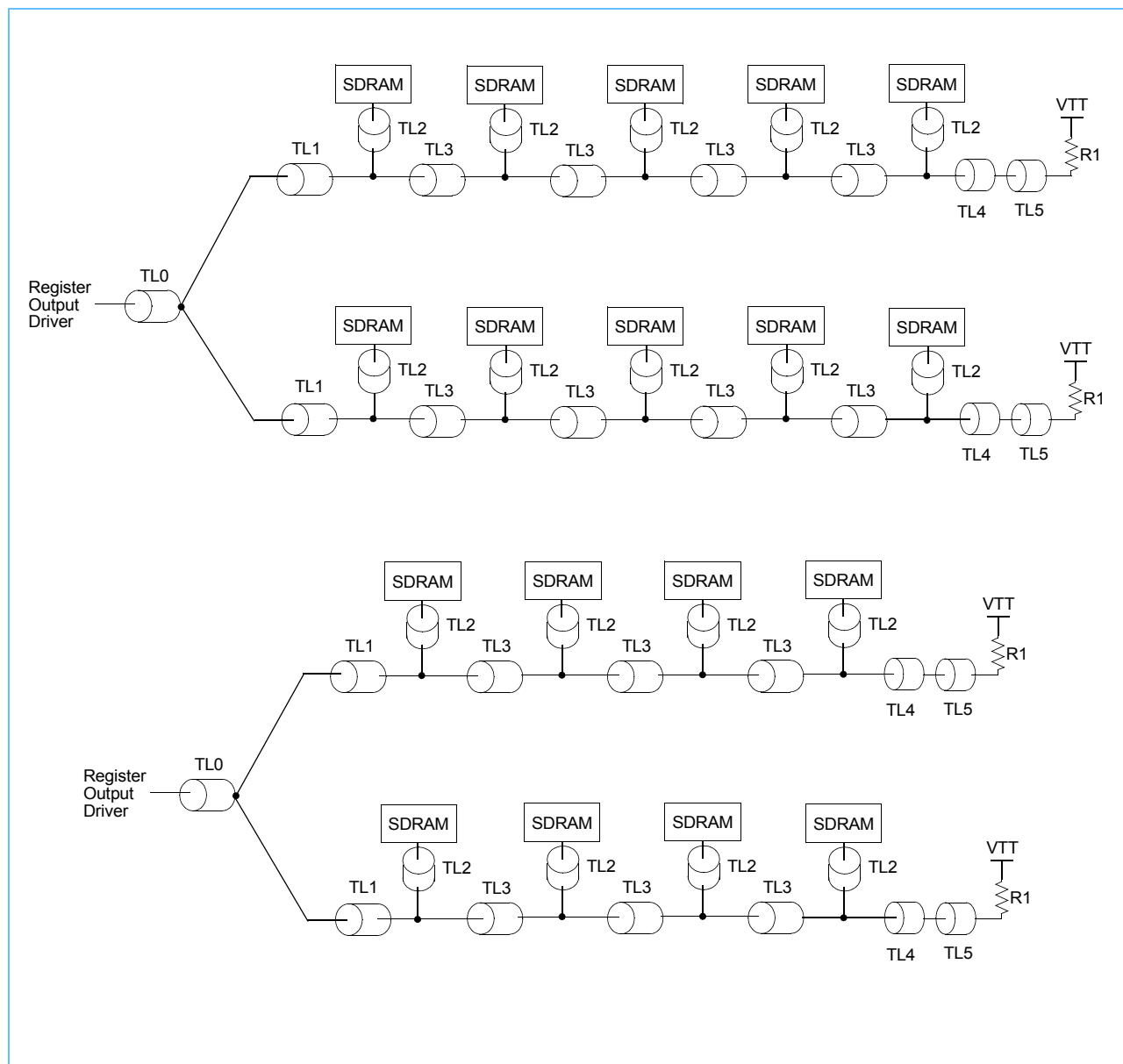
Trace Lengths for Post Register of Address and Command Net Structures

TL0		TL1		TL2		TL3		TL4		TL5		First DRAM		Last DRAM		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1.6	3.1	15.5	15.5	0.6	2.4	13.0	14.2	4.4	14.4	0.8	1.2	17.7	21.6	70.9	74.2	36 ± 5%	1, 2, 3

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
 NOTE 2 TL0 + TL1 = 17.85 mm ± 0.75 mm
 NOTE 3 First DRAM = TL0 + TL1 + TL2 , Last DRAM = TL0 + TL1 + TL2 + 4 x TL3

Post Register Control Net Structures

S[3:0]_n, CKE[1:0], ODT[1:0]



Trace Lengths for Post Register of Control Net Structures

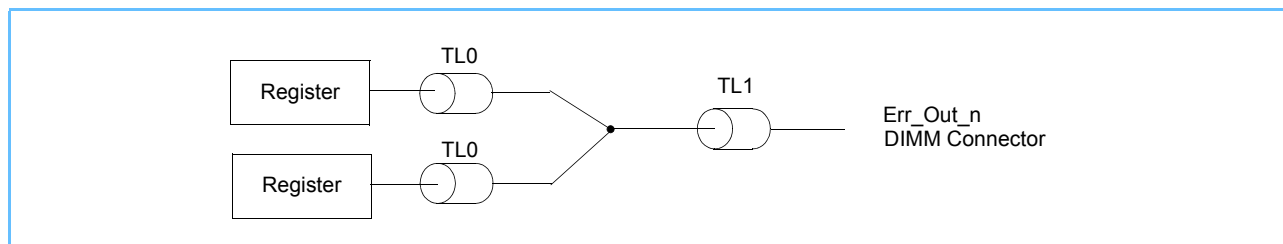
TL0		TL1		TL2		TL3		TL4		TL5		First DRAM		Last DRAM		R1 Ohms	Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
1.6	2.1	18.5	18.5	0.6	2.0	14.0	15.0	2.6	16.5	0.7	1.2	20.7	22.6	77.7	79.2	36 ± 5%	1, 2, 3

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

NOTE 2 $TL0 + TL1 = 20.35 \text{ mm} \pm 0.25 \text{ mm}$

NOTE 3 First DRAM = $TL0 + TL1 + TL2$, Last DRAM = $TL0 + TL1 + TL2 + 4 \times TL3$

Error Out Net Structure



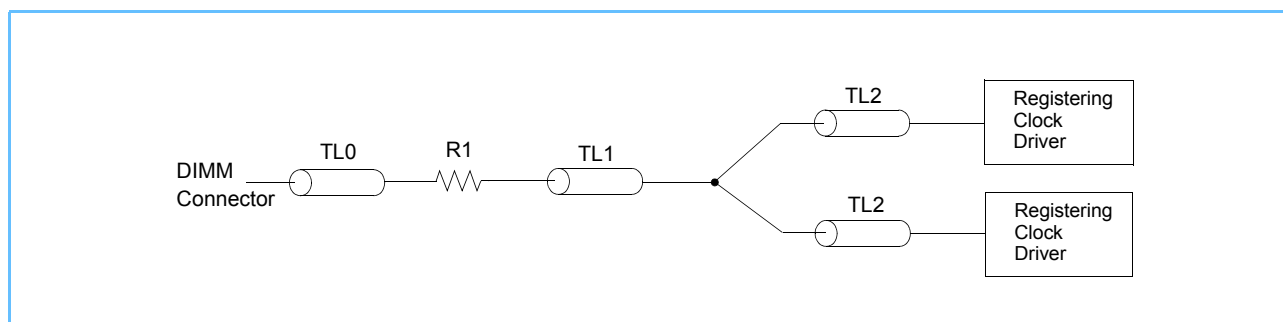
Trace Lengths of Error Out Net Structure

TL0	TL1	Notes
0.9	37.4	1

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Net Structure Routing of Pre Register Address, Command, Control and Address/Command Parity

A[15:0], BA[2:0], RAS_n, CAS_n, WE_n, CKE[1:0], Par_in



Trace Lengths of Pre Register Address, Command, Control and Address/Command Parity

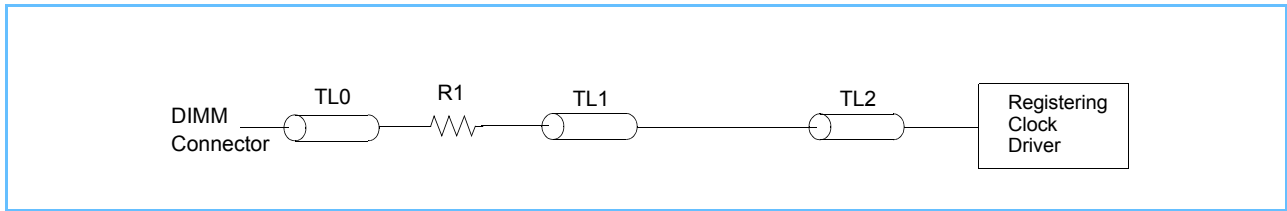
A[15:0], BA[2:0], RAS_n, CAS_n, WE_n, CKE[1:0], Par_in

	TL0		TL1		TL2		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max		
A[15:0], BA[2:0], RAS_n, CAS_n, WE_n, Par_in	2.9	3.5	15.5	17.9	0.7	3.0	22 \pm 5 %	1
CKE[1:0]	3.2	3.2	15.7	15.8	2.7	2.8	22 \pm 5 %	1

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

Net Structure Routing of Pre Register Control

S[3:0]_n, ODT[1:0]



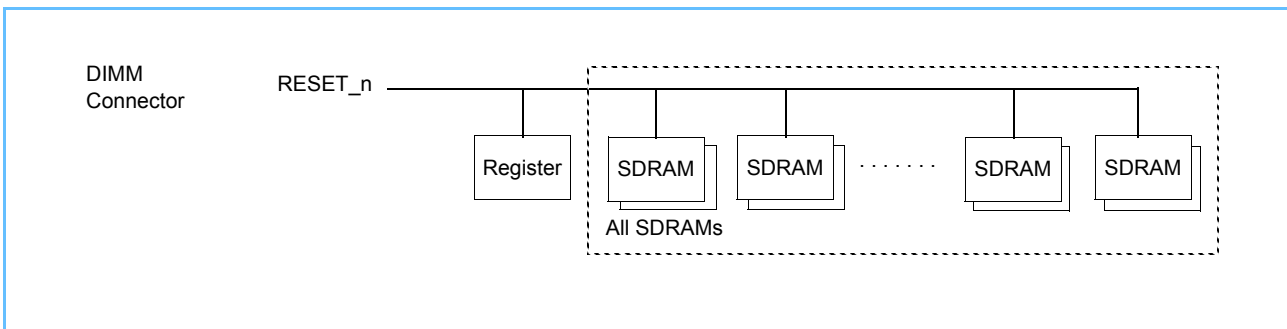
Trace Lengths of Pre Register Control

S[3:0]_n, ODT[1:0]

	TL0		TL1		TL2		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max		
S[3:0]_n, ODT[1:0]	2.9	3.6	21.3	21.4	2.7	2.8	22 ± 5 %	1

NOTE 1 All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.

RESET_n Net Structures



RESET_n Net Total Length

Total Net Length
575.4

NOTE Net is wired with 100um width; only the total length all traces together (in millimeters) is specified and must be kept within a tolerance of ± 10%

Cross Section Recommendations

Most DIMM printed circuit board designs use six layers of glass epoxy material. PCBs should contain solid ground plane and power plane layers as far as possible. The PCB stackup must be designed with 0.10 mm wide traces.

Any exceptions to these design rules will be identified earlier in the Design Rules and Deviations section of this annex.

NOTE The PCB edge connector contacts shall be gold-plated.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers, 0.10 mm wide single trace)	5.5	6.7	ps/mm
Trace velocity: S0 (inner layers, 0.10 mm wide single trace)	6.5	7.6	ps/mm
Trace impedance: Z ₀ (all layers, 0.10 mm wide single trace)	54	66	Ohms

Example Ten Layer Stackup

