

4.20.19 - 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000  
DDR3 SDRAM Unbuffered DIMM Design Specification

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## **DDR3 SDRAM Unbuffered DIMM Design Specification**

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## 1 Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 1.5 Volt ( $V_{DD}$ )/1.5 Volt ( $V_{DDQ}$ ), Unbuffered, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These DDR3 DIMMs are intended for use as main memory when installed in PCs.

Reference design examples are included which provide an initial basis for Unbuffered DDR3 DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC3-6400, PC3-8500, PC3-10600, PC3-12800, PC3-14900 and PC3-17000 support. All Unbuffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification follows the JEDEC standard DDR3 component specification (refer to JEDEC standard JESD79-3, at [www.jedec.org](http://www.jedec.org)).

**Table 1 — Product Family Attributes**

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (NOM)	133.35 mm x 30.00 mm x 4 mm	Refer to MO 269
Pin Count	240	
DDR3 SDRAMs Supported	512Mb, 1Gb, 2Gb, 4Gb, 8Gb	78/106-ball FBGA package for x8 and 96/112-ball FBGA for x16 devices.
Capacity	256MB–16GB	
Serial PD	Consistent with JEDEC JC 45 SPD publication	
Voltage Options	1.5 Volt $V_{DD}/V_{DDQ}$	All DDR3 modules use a common $V_{DD}-V_{DDQ}$ power plane. They are tied together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements.
	3.0 Volt to 3.6 Volt $V_{DDSPD}$	This supply is separate from the $V_{DD}/V_{DDQ}$ power plane. EEPROM supply is operable from 3.0V to 3.6V.
Interface	1.5V signaling	
Note 1 $V_{DDSPD}$ is not tied to $V_{DD}$ or $V_{DDQ}$ on the DDR3 DIMM.		

## 2 Environmental Requirements

240-pin Unbuffered DDR3 SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

**Table 2 — Environmental Parameters**

Symbol	Parameter	Rating	Units	Notes
T <sub>OPR</sub>	Operating Temperature (ambient)	0 to +55	°C	3
H <sub>OPR</sub>	Operating Humidity (relative)	10 to 90	%	
T <sub>STG</sub>	Storage Temperature	-50 to +100	°C	1
H <sub>STG</sub>	Storage Humidity (without condensation)	5 to 95	%	1
P <sub>BAR</sub>	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note 1 Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2 Up to 9850 ft.

Note 3 The component maximum case temperature (T<sub>CASE</sub>) shall not exceed the value specified in the DDR3 DRAM component specification.

### 3 Architecture

**Table 3 — Pin Definition**

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I <sup>2</sup> C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I <sup>2</sup> C serial bus data line for EEPROM
RAS <sub>n</sub>	SDRAM row address strobe	SA0–SA2	I <sup>2</sup> C slave address select for EEPROM
CAS <sub>n</sub>	SDRAM column address strobe	V <sub>DD</sub> *	SDRAM core power supply
WE <sub>n</sub>	SDRAM write enable	V <sub>DDQ</sub> *	SDRAM I/O Driver power supply
S0 <sub>n</sub> –S1 <sub>n</sub>	DIMM Rank Select Lines	V <sub>REFDQ</sub>	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	V <sub>REFCA</sub>	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V <sub>SS</sub>	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits	NC	Spare pins (no connect)
DQS0 <sub>t</sub> –DQS8 <sub>t</sub>	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
DQS0 <sub>c</sub> –DQS8 <sub>c</sub>	SDRAM data strobes (negative line of differential pair)	RESET <sub>n</sub>	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	EVENT <sub>n</sub>	Reserved for optional temperature-sensing hardware
CK0 <sub>t</sub> –CK1 <sub>t</sub>	SDRAM clocks (positive line of differential pair)	V <sub>TT</sub>	SDRAM I/O termination supply
CK0 <sub>c</sub> –CK1 <sub>c</sub>	SDRAM clocks (negative line of differential pair)	RSVD	Reserved for future use

\*The V<sub>DD</sub> and V<sub>DDQ</sub> pins are tied common to a single power-plane on these designs.

3 Architecture (Cont'd)

Table 4 — Input/Output Functional Description

Symbol	Type	Polarity	Function
A0–A15	1.5V	—	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC_n) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
BA0–BA2	1.5V	—	Selects which SDRAM bank of eight is activated.
CK0_t–CK1_t CK0_c–CK1_c	1.5V	Differential crossing	CK_t and CK_c are differential clock inputs. All the DDR3 SDRAM addr/ctl inputs are sampled on the crossing of positive edge of CK_t and negative edge of CK_c. Output (read) data is referenced to the crossing of CK_t and CK_c (Both directions of crossing).
CKE0–CKE1	1.5V	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
DM0–DM8	1.5V	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
DQ0–DQ63, CB0–CB7	1.5V	—	Data and Check Bit Input/Output pins.
DQS0_t–DQS8_t DQS0_c–DQS8_c	1.5V	Differential crossing	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are associated with the LDQS_t and LDQS_c pins and Pins DQ8–DQ15 are associated with UDQS_t and UDQS_c pins.
ODT0–ODT1	1.5V	Active High	When high, termination resistance is enabled for all DQ, DQS_t, DQS_c and DM pins, assuming this function is enabled on the DRAM.
RAS_n, CAS_n, WE_n	1.5V	Active Low	RAS_n, CAS_n, and WE_n (along with S_n) define the command being entered.
RESET_n	1.5V		The RESET_n pin is connected to the RESET_n pin on each DRAM. When low, all DRAMs are set to a known state.
S0_n–S1_n	1.5V	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
V <sub>DD</sub> , V <sub>SS</sub>	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. V <sub>DD</sub> and V <sub>DDQ</sub> pins are tied to V <sub>DD</sub> /V <sub>DDQ</sub> planes on these modules.
V <sub>DDQ</sub>	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V <sub>DDQ</sub> shares the same power plane as V <sub>DD</sub> pins.
V <sub>DDSPD</sub>	Supply		Power supply for SPD EEPROM. This supply is separate from the V <sub>DD</sub> /V <sub>DDQ</sub> power plane. EEPROM supply is operable from 3.0V to 3.6V.
V <sub>REFDQ</sub>	Supply		Reference voltage for I/O inputs.
V <sub>REFCA</sub>	Supply		Reference voltage for command/address inputs.
SA0–SA2		—	These signals are tied at the system planar to either V <sub>SS</sub> or V <sub>DDSPD</sub> to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V <sub>DDSPD</sub> to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V <sub>DDSPD</sub> to act as a pullup on the system board.
EVENT_n	Output (Open Drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on the TS/SPD part.

3 Architecture (Cont'd)

Table 5 — 240-Pin DDR3 SDRAM Pin Assignment (Part 1 of 2)

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A2	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DM3, DQS12_t, TDQS12_t	62	VDD	182	VDD	92	VSS	212	DM5, DQS14_t, TDQS14_t
3	DQ0	123	DQ5	33	DQS3_c	153	NC, DQS12_c, TDQS12_c	63	NC, CK1_t	183	VDD	93	DQS5_c	213	NC, DQS14_c, TDQS14_c
4	DQ1	124	VSS	34	DQS3_t	154	VSS	64	NC, CK1_c	184	CK0_t	94	DQS5_t	214	VSS
5	VSS	125	DM0, DQS9_t, TDQS9_t	35	VSS	155	DQ30	65	VDD	185	CK0_c	95	VSS	215	DQ46
6	DQS0_c	126	NC, DQS9_c, TDQS9_c	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0_t	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	EVENT_n, NC	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	CB4, NC	68	PAR_IN, NC	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	CB0, NC	159	CB5, NC	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	CB1, NC	160	VSS	70	A10/AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DM8, DQS17_t, TDQS17_t, NC	71	BA0	191	VDD	101	VSS	221	DM6, DQS15_t, TDQS15_t
12	DQ8	132	DQ13	42	DQS8_c	162	NC, DQS17_c, TDQS17_c	72	VDD	192	RAS_n	102	DQS6_c	222	NC, DQS15_c, TDQS15_c
13	DQ9	133	VSS	43	DQS8_t	163	VSS	73	WE_n	193	S0_n	103	DQS6_t	223	VSS
14	VSS	134	DM1, DQS10_t, TDQS10_t	44	VSS	164	CB6, NC	74	CAS_n	194	VDD	104	VSS	224	DQ54
15	DQS1_c	135	NC, DQS10_c, TDQS10_c	45	CB2, NC	165	CB7, NC	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1_t	136	VSS	46	CB3, NC	166	VSS	76	S1_n, NC	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC (TEST)	77	ODT1, NC	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	VTT, NC	168	RESET_n	78	VDD	198	S3_n, NC	108	DQ56	228	DQ61
19	DQ11	139	VSS	KEY				79	S2_n, NC	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	49	VTT, NC	169	CKE1, NC	80	VSS	200	DQ36	110	VSS	230	DM7, DQS16_t, TDQS16_t
21	DQ16	141	DQ21	50	CKE0	170	VDD	81	DQ32	201	DQ37	111	DQS7_c	231	NC, DQS16_c, TDQS16_c
22	DQ17	142	VSS	51	VDD	171	A15, NC	82	DQ33	202	VSS	112	DQS7_t	232	VSS

### 3 Architecture (Cont'd)

**Table 5 — 240-Pin DDR3 SDRAM Pin Assignment (Part 2 of 2)**

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
23	V <sub>SS</sub>	143	DM2, DQS11_t, TDQS11_t	52	BA2	172	A14	83	V <sub>SS</sub>	203	DM4, DQS13_t, TDQS13_t	113	V <sub>SS</sub>	233	DQ62
24	DQS2_c	144	NC, DQS11_c, TDQS11_c	53	ERR_OUT_n, NC	173	V <sub>DD</sub>	84	DQS4_c	204	NC, DQS13_c, TDQS13_c	114	DQ58	234	DQ63
25	DQS2_t	145	V <sub>SS</sub>	54	V <sub>DD</sub>	174	A12/BC_n	85	DQS4_t	205	V <sub>SS</sub>	115	DQ59	235	V <sub>SS</sub>
26	V <sub>SS</sub>	146	DQ22	55	A11	175	A9	86	V <sub>SS</sub>	206	DQ38	116	V <sub>SS</sub>	236	V <sub>DDSPD</sub>
27	DQ18	147	DQ23	56	A7	176	V <sub>DD</sub>	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V <sub>SS</sub>	57	V <sub>DD</sub>	177	A8	88	DQ35	208	V <sub>SS</sub>	118	SCL	238	SDA
29	V <sub>SS</sub>	149	DQ28	58	A5	178	A6	89	V <sub>SS</sub>	209	DQ44	119	SA2	239	V <sub>SS</sub>
30	DQ24	150	DQ29	59	A4	179	V <sub>DD</sub>	90	DQ40	210	DQ45	120	V <sub>TT</sub>	240	V <sub>TT</sub>
				60	V <sub>DD</sub>	180	A3								

**Table 6 — Pinout Comparison Between RDIMM Type and UDIMM Type**

Pin	RDIMM		UDIMM	
	Signal	Notes	Signal	Notes
48, 49	V <sub>TT</sub>	Additional connection for termination voltage for address/command/control/clock nets	NC	Not used on DIMMs
120, 240	V <sub>TT</sub>	Termination voltage for address/command/control/clock nets	V <sub>TT</sub>	Termination voltage for address/command/control/clock nets
53	ERR_OUT_n	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
63	NC, CK1_t	CK1 terminated but not used on RDIMMs	CK1_t	Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
64	NC, CK1_c		CK1_c	
68	Par_In	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
76	S1_n	Connected to the register on all RDIMMs	S1_n	Used for dual-rank UDIMMs; NC on single-rank UDIMMs
77	ODT1, NC	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	ODT1, NC	Used for dual-rank UDIMMs; NC on single-rank UDIMMs
79	S2_n, NC	Connected to the register on quad-rank RDIMMs; NC on single- or dual-rank RDIMMs	NC	Not used on UDIMMs
167	NC	TEST input used only on bus analysis probes	NC	TEST input used only on bus analysis probes
169	CKE1	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	CKE1, NC	Used for double-rank UDIMMs; NC on single-rank UDIMMs
171	A15	Connected to the register on all DIMMs	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs; however, these signals are terminated on UDIMMs; A15: not routed on some raw cards
172	A14		A14	
196	A13		A13	
198	S3_n, NC	Connected to the register on quad-rank RDIMMs; NC on single- or dual-rank RDIMMs	NC	Not used on UDIMMs

3 Architecture (Cont'd)

**Table 6 — Pinout Comparison Between RDIMM Type and UDIMM Type (Cont'd)**

Pin	RDIMM		UDIMM	
	Signal	Notes	Signal	Notes
39, 40, 45, 46, 158, 159, 164, 165	CB $n$	Used on all RDIMMs ( $n = 0...7$ )	NC, CB $n$	Used on x72 UDIMMs ( $n = 0...7$ ); not used on x64 UDIMMs
125, 134, 143, 152, 161, 203, 212, 221, 230	DQS $n\_t$ , TDQS $n\_t$	Connected to DQS $_t$ on x4 DRAMs; TDQS $_t$ on x8 RDIMM SDRAMs ( $n = 9...17$ )	DM $n$	Connected to DM on x8 DRAMs; UDM or LDM on x16 UDIMM DRAMs ( $n = 0...8$ ); DM8 is not used on x64 UDIMMs
126, 135, 144, 153, 162, 204, 213, 222, 231	DQS $n\_c$ , TDQS $n\_c$	Connected to DQS $_c$ on x4 DRAMs; TDQS $_c$ on x8 RDIMM SDRAMs ( $n = 9...17$ )	NC	DQS9 $_c$ –DQS17 $_c$ and TDQS $n\_c$ are not used on UDIMMs.
187	EVENT $_n$	Connected to thermal sensing component	EVENT $_n$ , NC	Connected to the thermal sensing component on ECC DIMMs. No connection on nonECC DIMMs

**Table 7 — Pinout Comparison Between LRDIMM Type and UDIMM Type**

Pin	LRDIMM		UDIMM	
	Signal	Notes	Signal	Notes
48, 49	V <sub>TT</sub>	Termination Voltage for Address/Command/Control/Clock nets.	NC	Not used on UDIMMs
120, 240	V <sub>TT</sub>	Termination Voltage for Address/Command/Control/Clock nets.	V <sub>TT</sub>	Termination voltage for address/command/control/clock nets.
53	ERR_OUT $_n$	Parity error output of Memory Buffer	NC	Not used on UDIMMs
63	CK1 $_t$	Terminated but not used	CK1 $_t$	Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
64	CK1 $_c$		CK1 $_c$	
68	Par_In	Parity input to Memory Buffer (MB). This signal is required for MB functionality.	NC	Not used on UDIMMs
76	S1 $_n$	Chip select for the second logical rank. Required for programming the Memory Buffer. SMBus can be used for programming the MB.	S1 $_n$	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs
77	ODT1, CKE3	Provides 4th CKE signal. Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs. Connected to MB.	ODT1, NC	Used for dual-rank UDIMMs, not connected on single-rank UDIMMs
79	S2 $_n$ , A16	May be used as third chip select or address A16. Use is system dependent. MB can be programmed to use it as chip select 2 or address A16.	NC	Not used on UDIMMs
167	CKE2	Not used on JEDEC standard LRDIMMs but may be used on custom LRDIMMs.	NC	TEST input used only on bus analysis probes
169	CKE1	2nd CKE.	CKE1, NC	Used for double-rank UDIMMs, not connected on single-rank UDIMMs

### 3 Architecture (Cont'd)

**Table 7 — Pinout Comparison Between LRDIMM Type and UDIMM Type (Cont'd)**

Pin	LRDIMM		UDIMM	
	Signal	Notes	Signal	Notes
171	A15	Always used on LRDIMMs	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs, however, these signals are terminated on UDIMMs. A15. not routed on some RCs
172	A14		A14	
196	A13		A13	
198	S3_n, A17	May be used as either a 4th chip select or address A17. Use is system dependent. MB can be programmed to use it as chip select 3 or address A17.	NC	Not used on UDIMMs
39, 40, 45, 46, 158, 159, 164, 165	CB <sub>n</sub>	ECC byte. Always used on LRDIMM.	NC, CB <sub>n</sub>	Used on x72 UDIMMs ( <i>n</i> = 0...7); not used on x64 UDIMMs
125, 134, 143, 152, 161, 203, 212, 221, 230	DQS[9:17] <sub>t</sub>	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.	DM <sub>n</sub>	Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; ( <i>n</i> = 0...8)
126, 135, 144, 153, 162, 204, 213, 222, 231	DQS[9:17] <sub>c</sub>	Always connected to MB. Typically used for LRDIMMs with x4 SDRAMs. Not used for LRDIMMs with x8 SDRAMs.	NC	not used on UDIMMs
187	EVENT_n	Connected to the thermal sensing component and MB.	EVENT_n, NC	Connected to the thermal sensing component on ECC DIMMs. No connection on non-ECC DIMMs.
NC = no internal connection				

### 3.1 Address Mirroring Feature

There is a via grid located under the SDRAMs for wiring the CA signals (address, bank address, command, and control lines) to the SDRAM pins. The length of the traces from the vias to the SDRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.

The pins on the SDRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 SDRAM pins are wired straight, with no mismatch between the connector pin assignment and the SDRAM pin assignment. Some of the Rank 1 SDRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

**Table 8 — SDRAM Pin Wiring for Mirroring**

Connector Pin	SDRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5

3 Architecture (Cont'd)

Table 8 — SDRAM Pin Wiring for Mirroring (Cont'd)

Connector Pin	SDRAM Pin	
	Rank 0	Rank 1
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

Figure 1 illustrates the wiring in both the mirrored and non-mirrored case. The lengths of the traces to the SDRAM pins, is obviously shorter. The via grid is smaller as well.

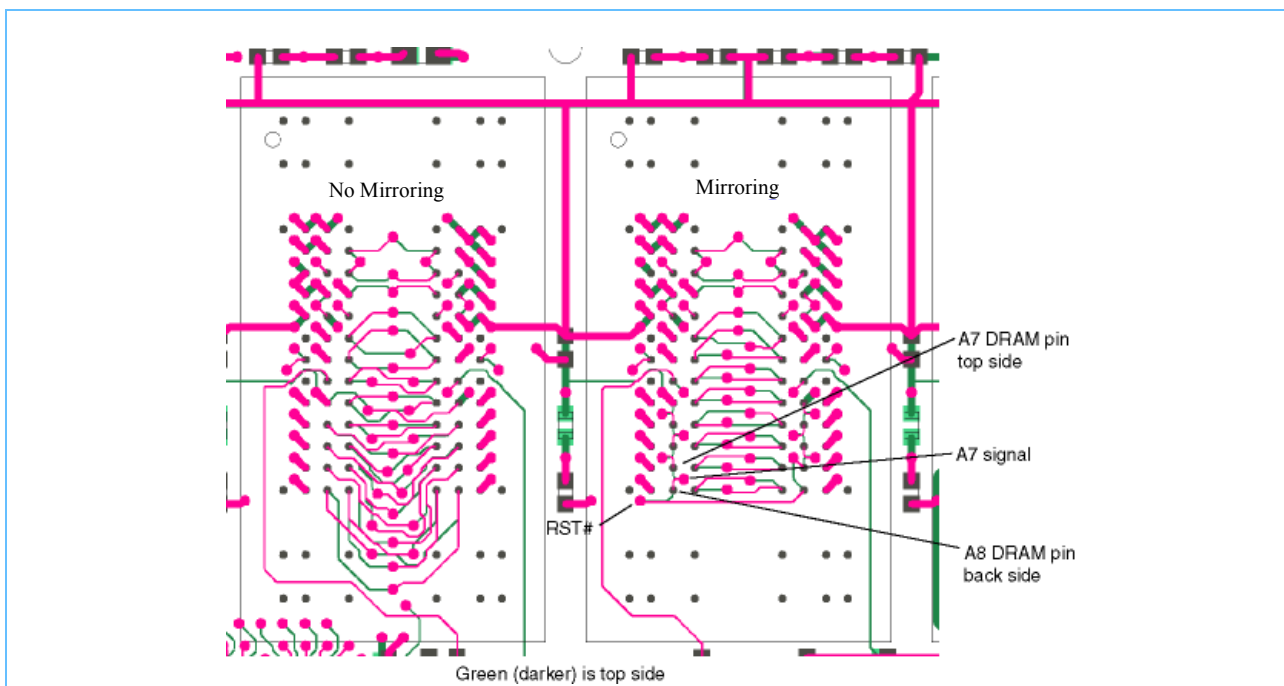


Figure 1 — Wiring Differences for Mirrored and Non-Mirrored Addresses

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a few rules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 SPD specification, UDIMM Annex, for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

3 Architecture (Cont'd)

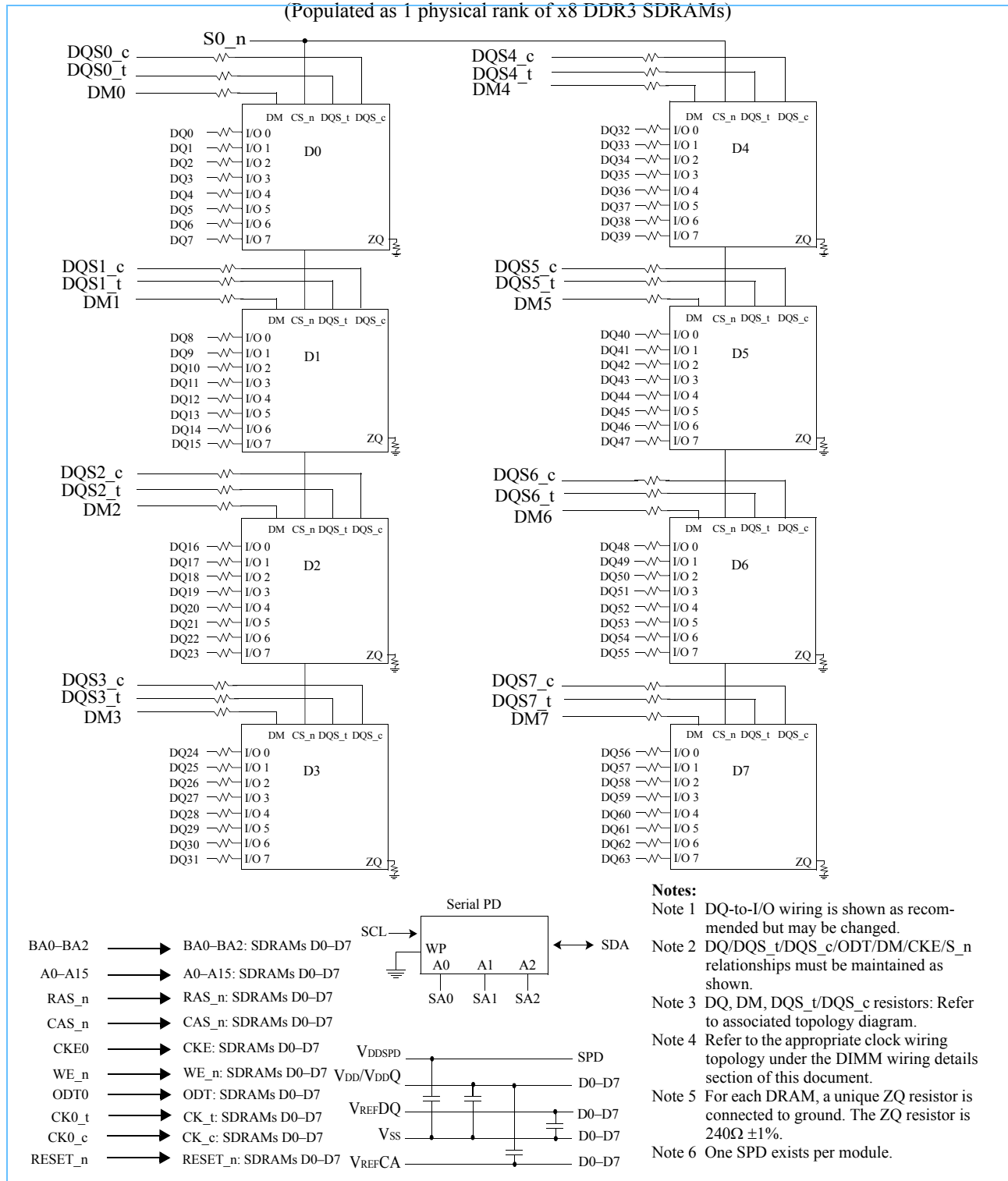


Figure 2 — Block Diagram: Raw Card Version A, x64

3 Architecture (Cont'd)

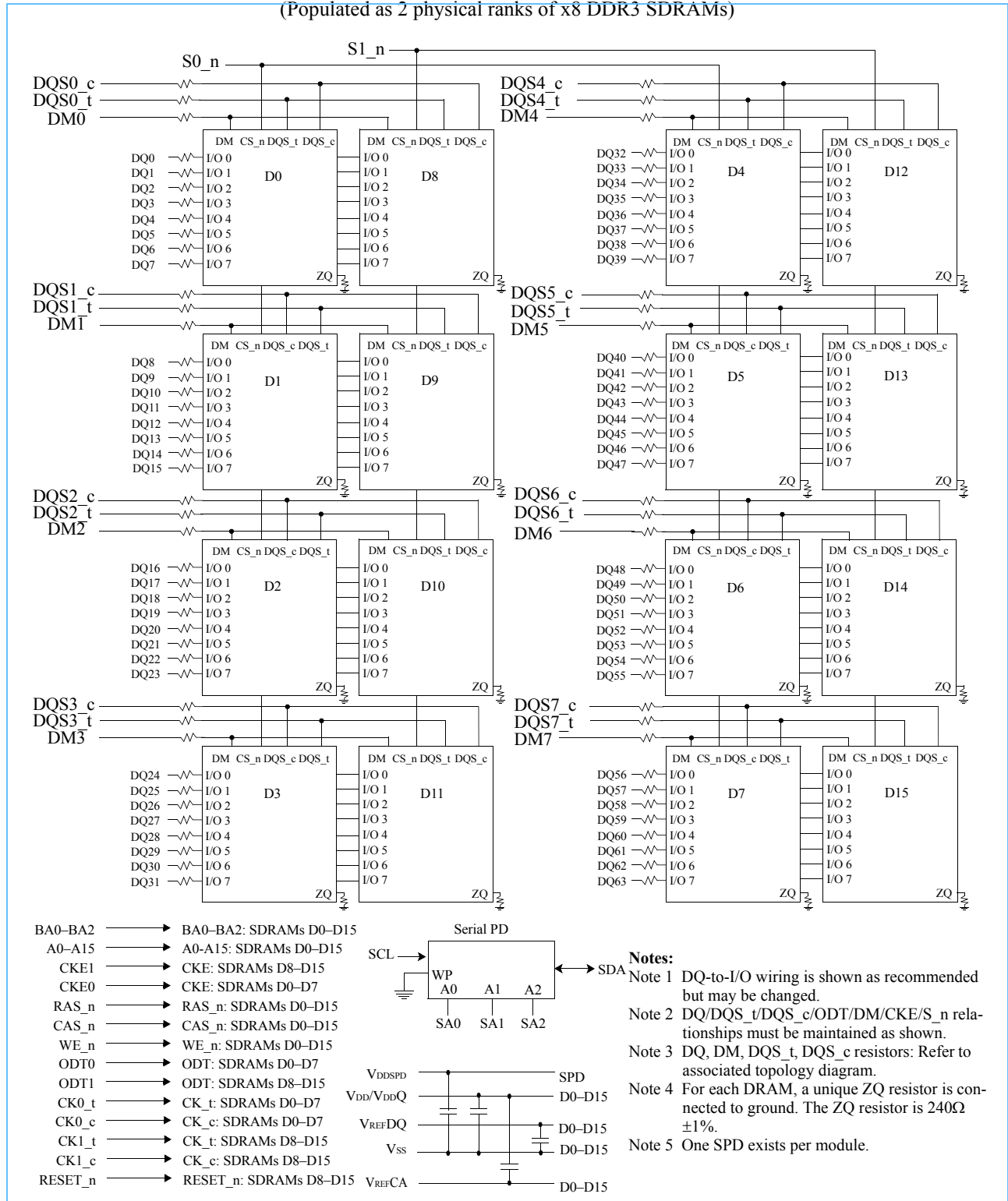


Figure 3 — Block Diagram: Raw Card Version B, x64

3 Architecture (Cont'd)

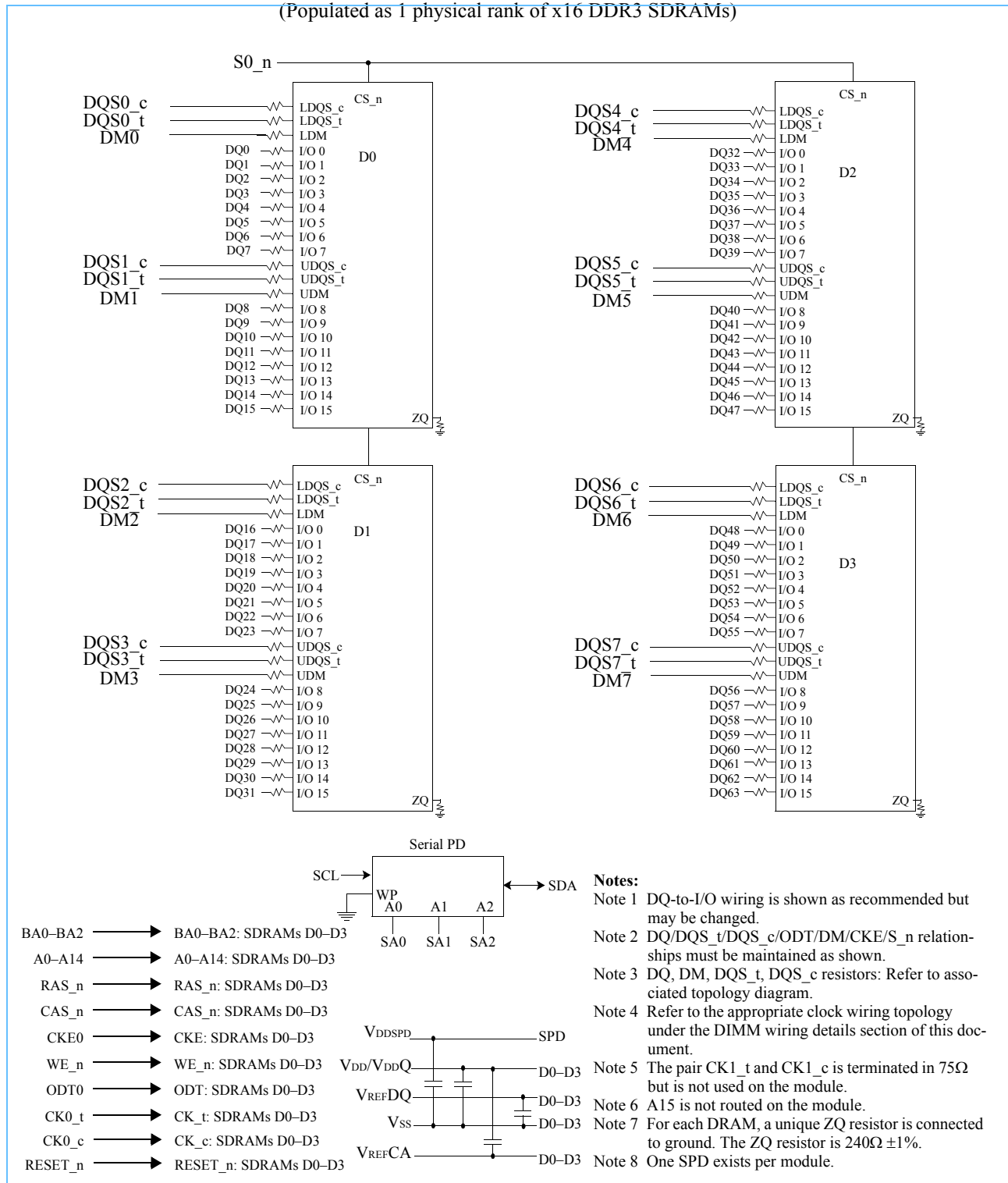


Figure 4 — Block Diagram: Raw Card Version C, x64

3 Architecture (Cont'd)

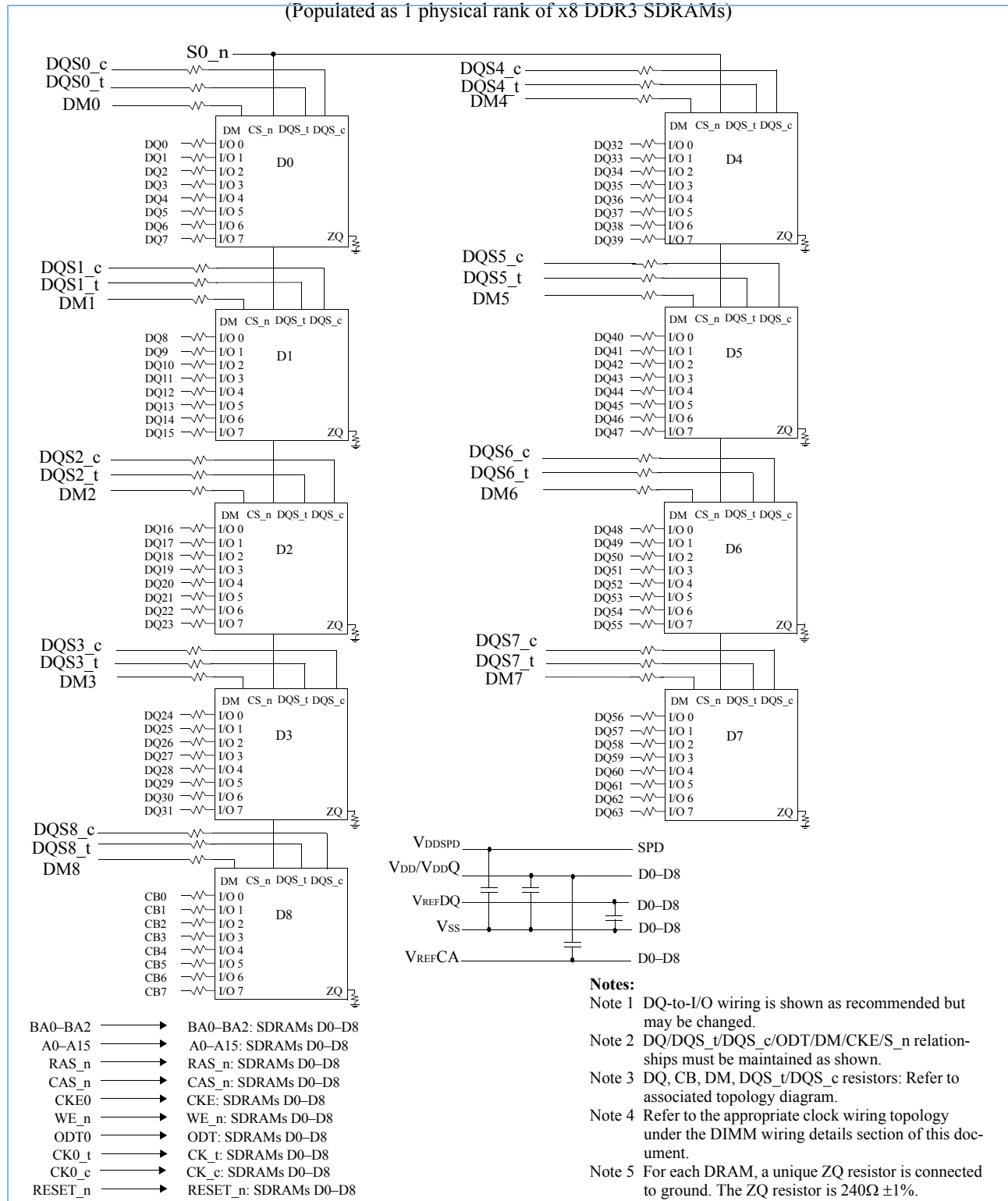


Figure 5 — Block Diagram: Raw Card Version D, x72

3 Architecture (Cont'd)

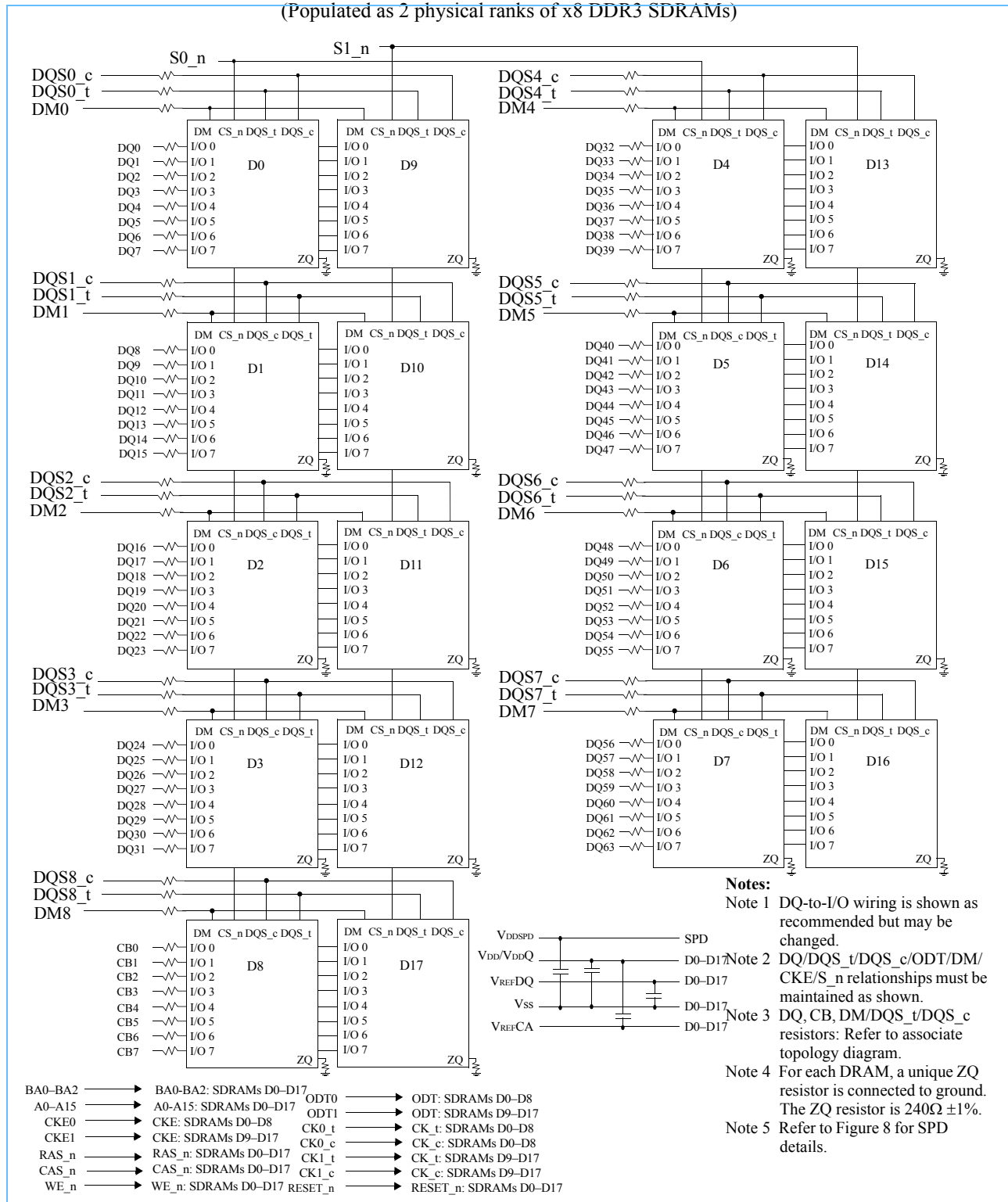


Figure 6 — Block Diagram: Raw Card Version E, x72

3 Architecture (Cont'd)

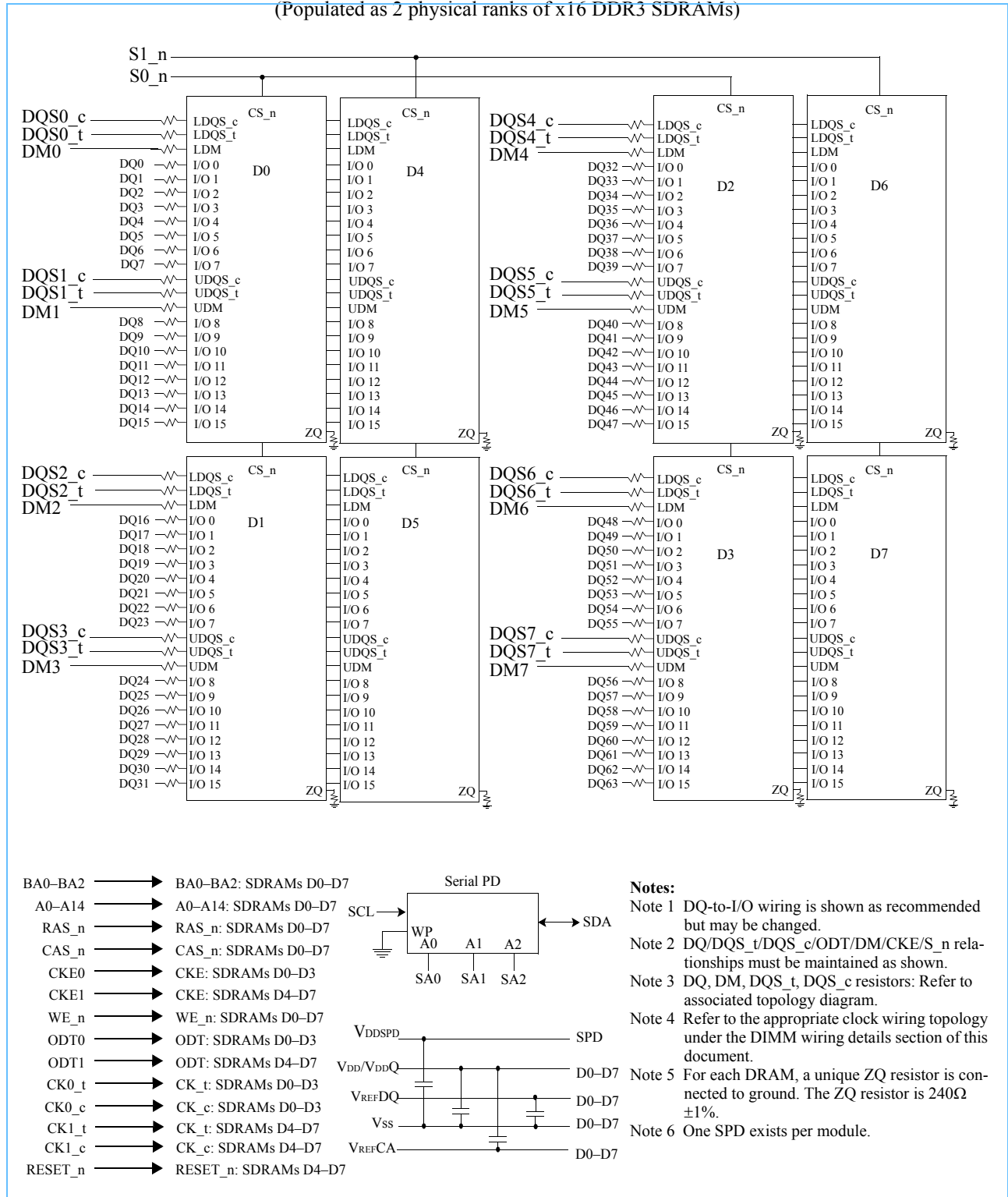
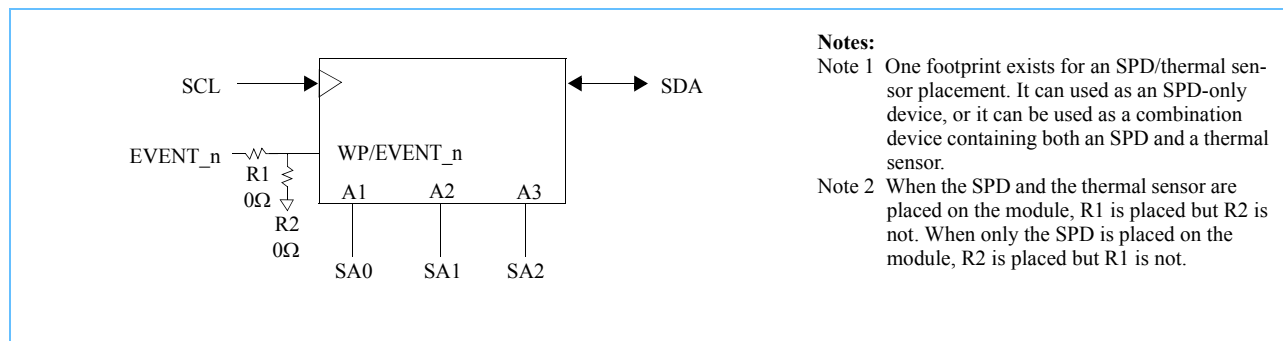


Figure 7 — Block Diagram: Raw Card Version F, x64

### 3 Architecture (Cont'd)

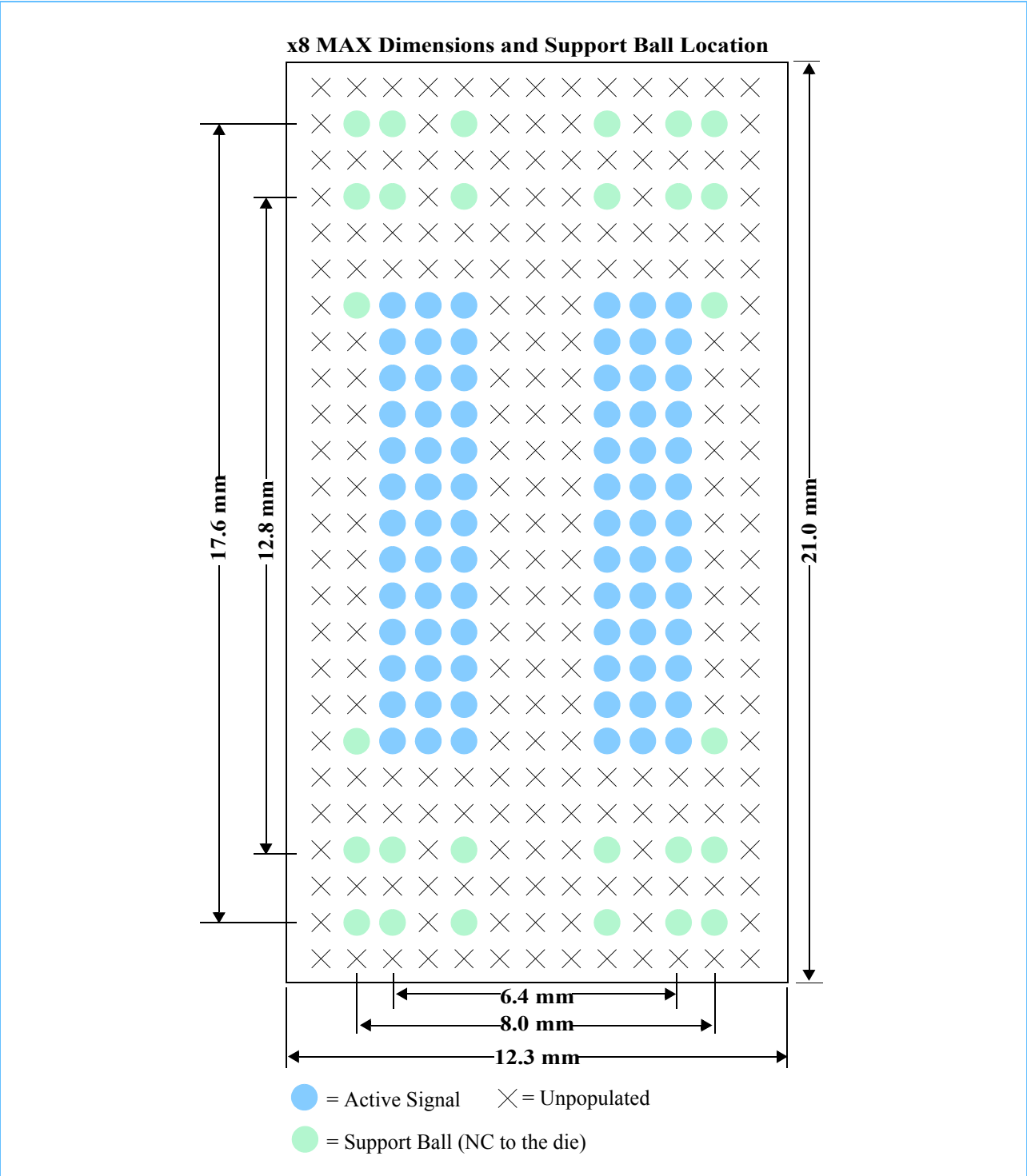


**Figure 8 — Block Diagram: SPD and Thermal Sensor**

An optional on-DIMM thermal sensor will provide DRAM temperature readout through a discrete or integrated thermal sensor.

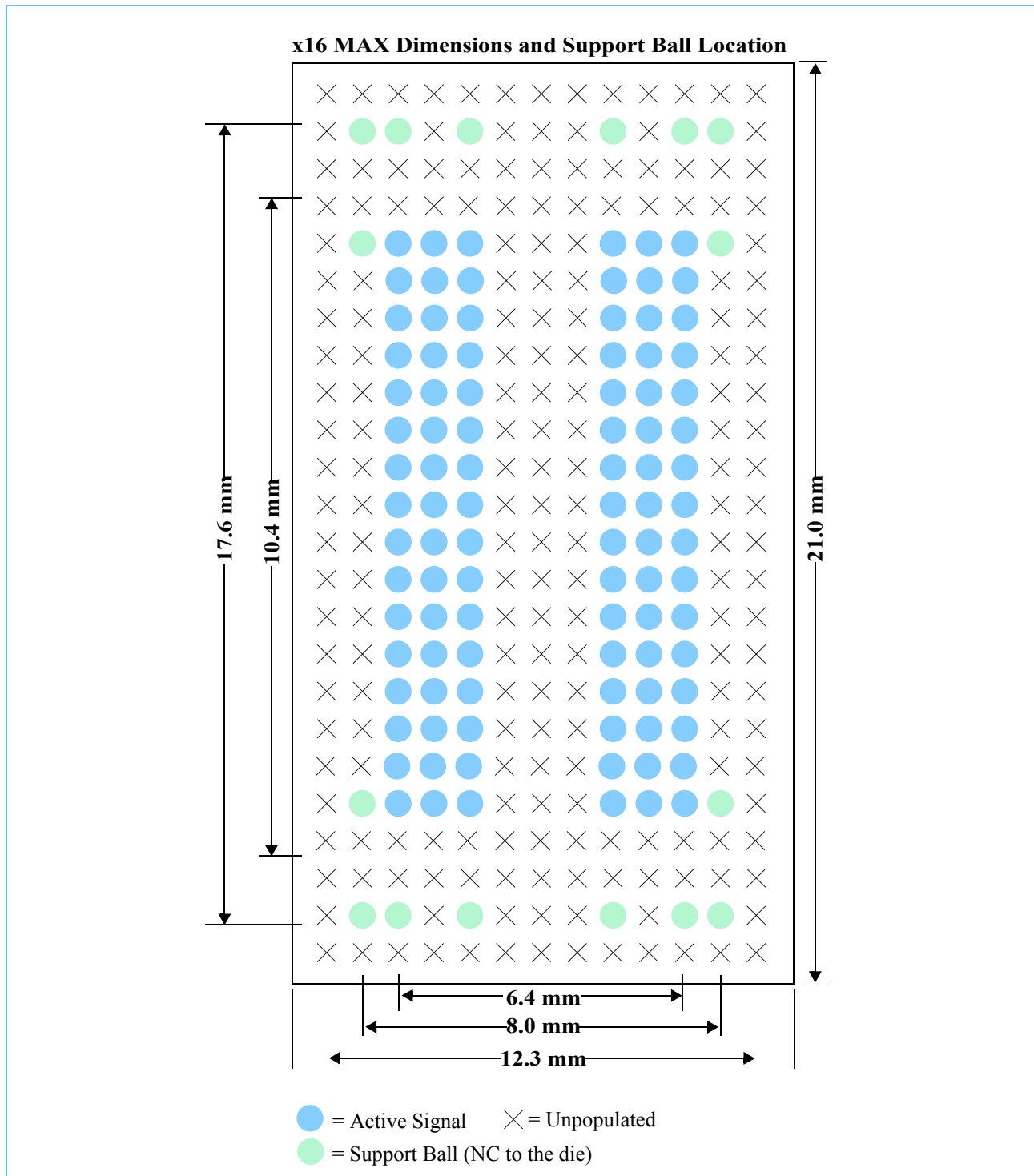
On low-profile, 30mm DIMMs, the thermal sensor and serial presence-detect footprint will be placed near the center of the DIMM, both vertically and horizontally (refer to MO-269 for placement requirements). TDFN packages are used for the thermal sensor and the serial presence-detect. MO-229C, variations VCED-3 or VEED-7 will be referenced for the thermal sensor and serial presence-detect part.

### 4 Component Details



**Figure 9 — DIMM Ball Pattern for x8 - 512Mb, 1Gb, 2Gb, 4Gb, and 8Gb DDR3 SDRAM Planar Components (Top View)**

4 Component Details (Cont'd)



**Figure 10 — DIMM Ball Pattern for x16 - 512Mb, 1Gb, 2Gb, 4Gb, and 8Gb DDR3 SDRAM Planar Components (Top View)**

## 5 Unbuffered DIMM Details

**Table 9 — SDRAM Module Configurations (Reference Designs)**

Raw Card Version	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	Number of SDRAMs	Number of Physical Ranks	Number of Banks in SDRAM	Number of Address Bits Row/Column
A	512MB	64 Meg x 64	512 Megabit	64 Meg x 8	8	1	8	13/10
	1GB	128 Meg x 64	1 Gigabit	128 Meg x 8	8	1	8	14/10
	2GB	256 Meg x 64	2 Gigabit	256 Meg x 8	8	1	8	15/10
	4GB	512 Meg x 64	4 Gigabit	512 Meg x 8	8	1	8	16/10
	8GB	1 Gig x 64	8 Gigabit	1 Gig x 8	8	1	8	16/11
B	1GB	128 Meg x 64	512 Megabit	64 Meg x 8	16	2	8	13/10
	2GB	256 Meg x 64	1 Gigabit	128 Meg x 8	16	2	8	14/10
	4GB	512 Meg x 64	2 Gigabit	256 Meg x 8	16	2	8	15/10
	8GB	1 Gig x 64	4 Gigabit	512 Meg x 8	16	2	8	16/10
	16GB	2 Gig x 64	8 Gigabit	1 Gig x 8	16	2	8	16/11
C <sup>1</sup>	256MB	32 Meg x 64	512 Megabit	32 Meg x 16	4	1	8	12/10
	512MB	64 Meg x 64	1 Gigabit	64 Meg x 16	4	1	8	13/10
	1GB	128 Meg x 64	2 Gigabit	128 Meg x 16	4	1	8	14/10
	2GB	256 Meg x 64	4 Gigabit	256 Meg x 16	4	1	8	15/10
D	512MB	64 Meg x 72	512 Megabit	64 Meg x 8	9	1	8	13/10
	1GB	128 Meg x 72	1 Gigabit	128 Meg x 8	9	1	8	14/10
	2GB	256 Meg x 72	2 Gigabit	256 Meg x 8	9	1	8	15/10
	4GB	512 Meg x 72	4 Gigabit	512 Meg x 8	9	1	8	16/10
	8GB	1 Gig x 72	8 Gigabit	1 Gig x 8	9	1	8	16/11
E	1GB	128 Meg x 72	512 Megabit	64 Meg x 8	18	2	8	13/10
	2GB	256 Meg x 72	1 Gigabit	128 Meg x 8	18	2	8	14/10
	4GB	512 Meg x 72	2 Gigabit	256 Meg x 8	18	2	8	15/10
	8GB	1 Gig x 72	4 Gigabit	512 Meg x 8	18	2	8	16/10
	16GB	2 Gig x 72	8 Gigabit	1 Gig x 8	18	2	8	16/11
F <sup>1</sup>	512MB	32 Meg x 64	512 Megabit	32 Meg x 16	8	2	8	12/10
	1GB	64 Meg x 64	1 Gigabit	64 Meg x 16	8	2	8	13/10
	2GB	128 Meg x 64	2 Gigabit	128 Meg x 16	8	2	8	14/10
	4GB	256 Meg x 64	4 Gigabit	256 Meg x 16	8	2	8	15/10

Note 1 Registrations C0 and F0 do not wire A15 and therefore the 8Gb device is not supported on the registration.

## 5 Unbuffered DIMM Details (Cont'd)

**Table 10 — Input Loading Matrix**

Signal Names	Input Device	Raw Card Version A	Raw Card Version B	Raw Card Version C	Raw Card Version D	Raw Card Version E	Raw Card Version F
CK_t/CK_c	SDRAM	8	8	4	9	9	4
CS_n/CKE/ODT	SDRAM	8	8	4	9	9	4
Addr/RAS_n/CAS_n/BA/WE_n	SDRAM	8	16	4	9	18	8
DQ/DQS_t/DQS_c/DM	SDRAM	1	2	1	1	2	2
CB/DQS8_t/DQS8_c/DM8	SDRAM	—	—	—	1	2	—
SCL/SDA/SA	EEPROM	1	1	1	1	1	1
RESET_n	SDRAM	8	16	4	9	18	8

Note 1 ODT1, CKE1, and CS1 have no loads on Raw Cards A, C, or D

### 5.1 DDR3 Unbuffered Design File Releases

"Reference" design file updates will be released as needed. This DDR3 Unbuffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

Note: Future design file releases will include both a date and a revision label. All changes to the design file are also documented within the 'read-me' file.

**Table 11 — Design File Releases**

Raw Card Version	Specification Revision	Applicable Gerber File (zip)	Special notes	Maximum Speed
A0	0.71	PC3_12800_UDIMM_V071_RC_A0_20070426		12800
A1	1.03	PC3-UDIMM_V103_RC_A1_20100805		14900
B0	0.70	PC3_12800_UDIMM_V07_RC_B0_20070529	Uses address mirroring	12800
B1	1.03	PC3-UDIMM_V103_RC_B1_20100805	Uses address mirroring	14900
C0	0.50	PC3_10600_UDIMM_V050_RC_C0_20070530		12800
D0	0.84	PC3_12800_UDIMM_V084_RC_D0_20071025	Supports thermal sensor option	12800
D1	1.02	PC3-UDIMM_V102_RC_D1_20100422	Supports thermal sensor option	14900
E1	0.87	PC3_12800_UDIMM_V087_RC_E1_20071025	Uses address mirroring Supports thermal sensor option	12800
E2	1.02	PC3-UDIMM_V102_RC_E2_20100930	Uses address mirroring Supports thermal sensor option	14900
E3	1.03	PC3-UDIMM_V103_RC_E3_20100908	Uses address mirroring Supports thermal sensor option	14900
F0	0.50	PC3_10600_UDIMM_V050_RC_F0_20070530	Uses address mirroring	12800

5 Unbuffered DIMM Details (Cont'd)

5.2 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins.

The following layouts suggest placement for raw card versions A, B, C, D, E, and F. Exact spacing is not provided but should be based on manufacturing constraints and signal routing constraints imposed by this design guide. For all dimensions, refer to MO-269.

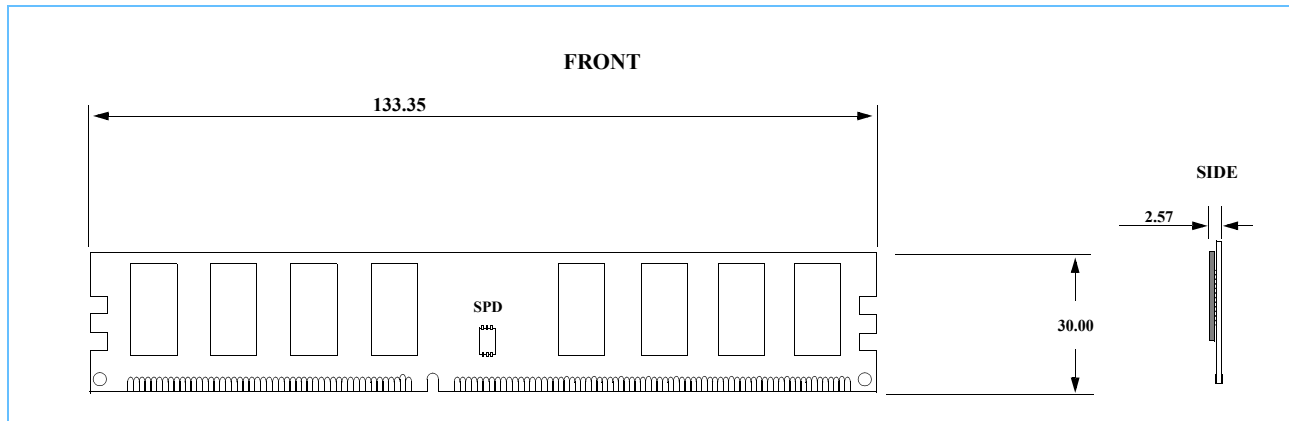


Figure 11 — Example Component Placement (Raw Card Version A)

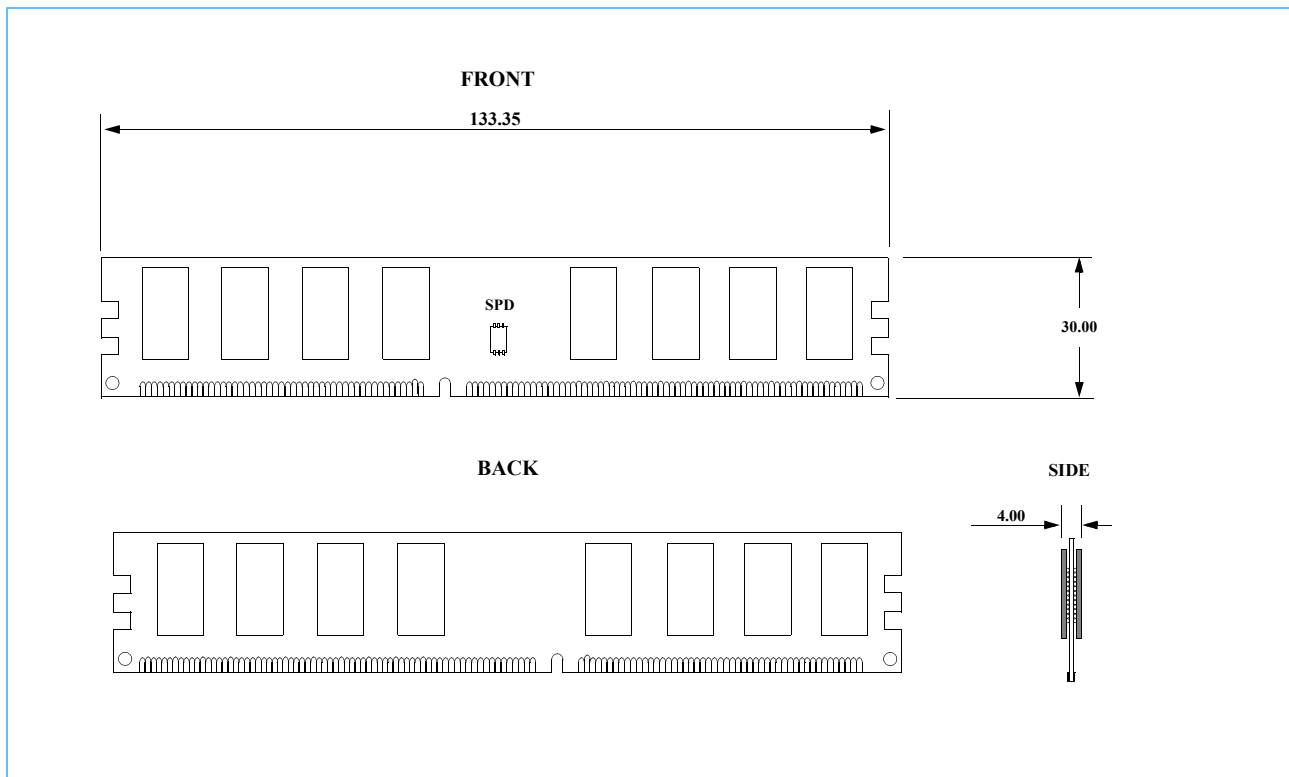


Figure 12 — Example Component Placement (Raw Card Version B)

5 Unbuffered DIMM Details (Cont'd)

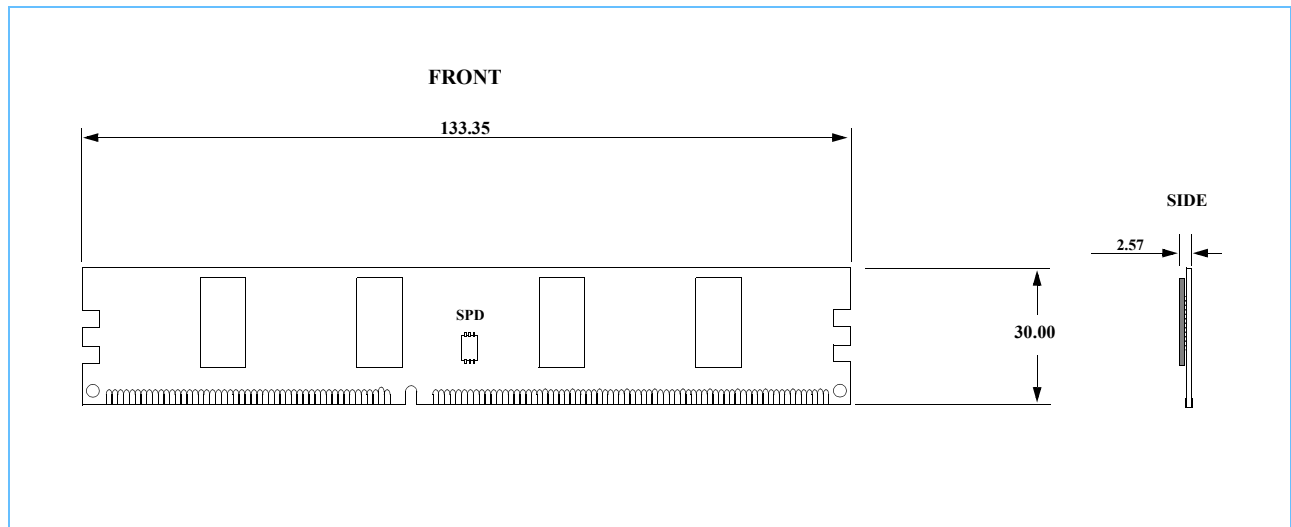


Figure 13 — Example Component Placement (Raw Card Version C)

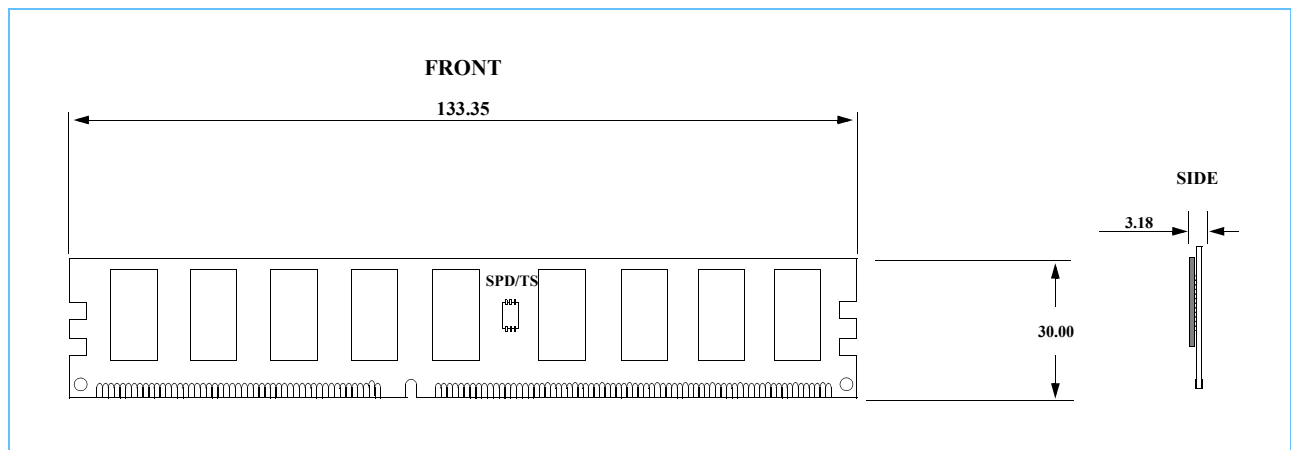


Figure 14 — Example Component Placement (Raw Card Version D)

5 Unbuffered DIMM Details (Cont'd)

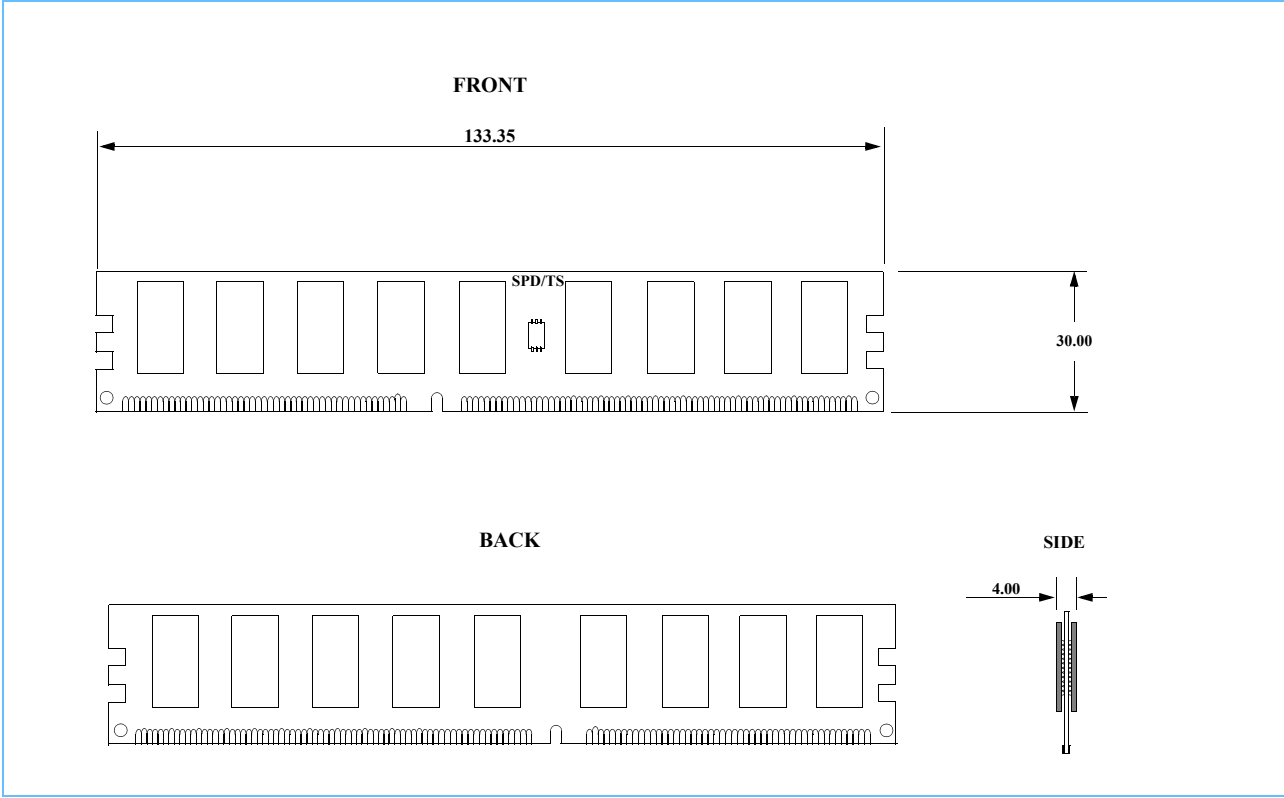


Figure 15 — Example Component Placement (Raw Card Version E)

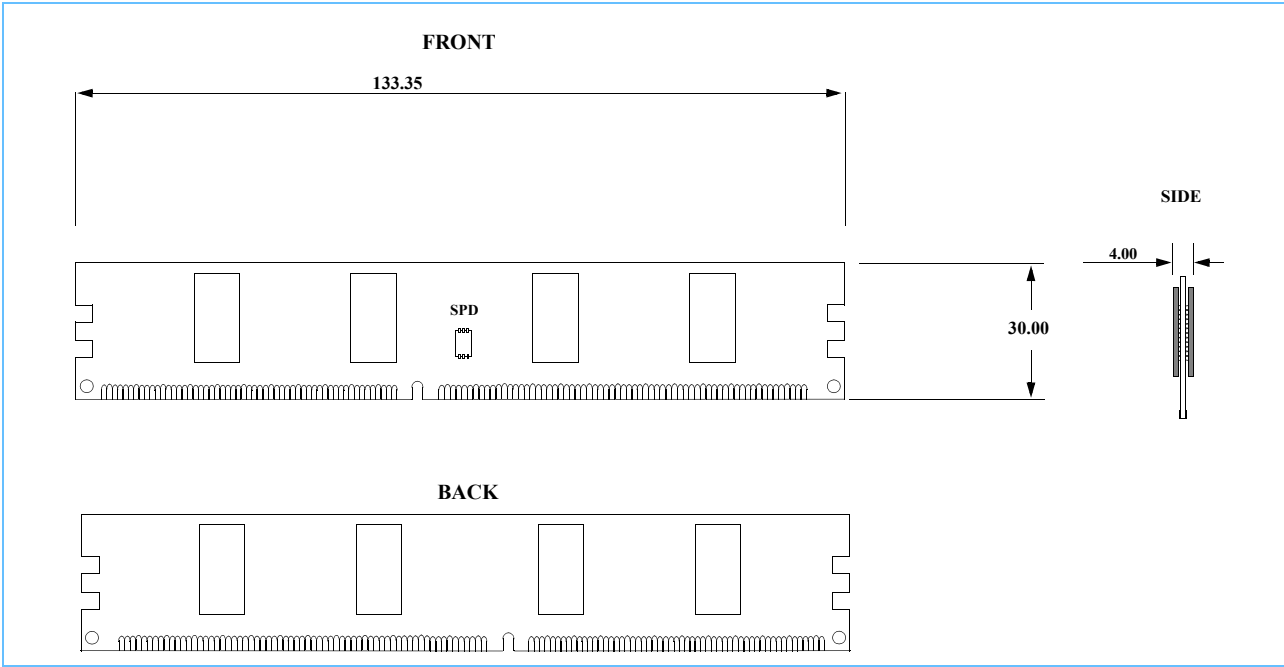


Figure 16 — Example Component Placement (Raw Card Version F)

## 5 Unbuffered DIMM Details (Cont'd)

### 5.3 Decoupling Guidelines

**Table 12 — UDIMM Decoupling Capacitor Guidelines**

	Value, Counts	Notes
V <sub>DD</sub>	Minimum of two decoupling capacitors to V <sub>SS</sub> per SDRAM	Should be placed as close as possible to the DRAM V <sub>DD</sub> ball
	Minimum of four bulk decoupling capacitors to V <sub>SS</sub> per module	
V <sub>TT</sub>	Minimum of one decoupling capacitor to V <sub>DD</sub> per every two termination resistors or a decoupling capacitor at both ends of each R <sub>PACK</sub>	Should be placed as close as possible to the DRAM V <sub>DD</sub> ball
	Minimum of one decoupling capacitor to V <sub>DD</sub> (located near the card edge V <sub>TT</sub> pin) or a decoupling capacitor at both ends of each R <sub>PACK</sub>	
V <sub>REFCA</sub>	Minimum of one decoupling capacitor to V <sub>DD</sub> per DRAM	Should be placed as close as possible to the DRAM V <sub>REFCA</sub> ball
	Minimum of one decoupling capacitor to V <sub>DD</sub> (located near the card edge V <sub>REFCA</sub> pin)	
V <sub>REFDQ</sub>	Minimum of one decoupling capacitor to V <sub>SS</sub> per DRAM	Should be placed as close as possible to the DRAM V <sub>REFDQ</sub> ball
	Minimum of one decoupling capacitor to V <sub>SS</sub> (located near the card edge V <sub>REFDQ</sub> pin)	

Note 1 Decoupling capacitor values vary by module and may be staggered to achieve best overall impedance vs. frequency response

Note 2 Recommended values for decoupling are 0.01 $\mu$ f, 0.022 $\mu$ f, 0.047 $\mu$ f, 0.1 $\mu$ f, and 0.22 $\mu$ f

Note 3 Recommended values for bulk decoupling are 1.0 $\mu$ f, 2.2 $\mu$ f, 3.3 $\mu$ f, and 4.7 $\mu$ f

Note 4 Depending on the DRAM package size, all placements may not be possible

## 6 DIMM Wiring Details

### 6.1 Signal Groups

This specification categorizes DDR3 SDRAM timing-critical signals into four groups. The following table summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. They sweep from the left side of the module to the right.

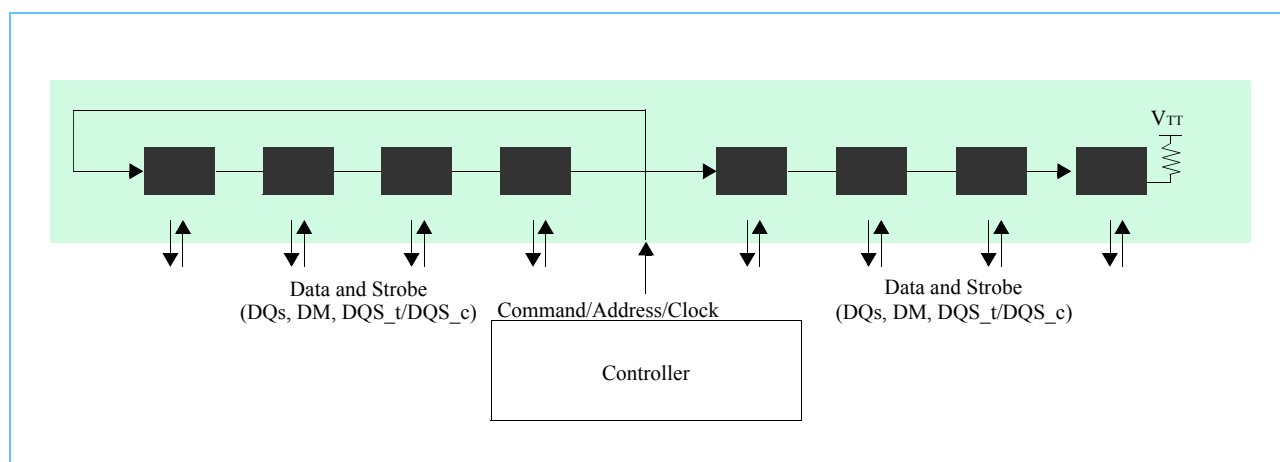


Figure 17 — Fly-By Topology

Table 13 — Timing-Critical Signals

Signal Group	Signals In Group	Raw Card Version	Page
Clock	CK0_t, CK0_c	A, C, D	37, 39, 40
	CK0_t, CK0_c, CK1_t, CK1_c	B, E, F	38, 41, 42
Data	DQ, DM, DQS_t, DQS_c	A, B, C, D, E, F	49, 51, 53, 55, 57, 60
Control	S0_n, ODT0, CKE0	A, C, D	43, 44, 44
	S0_n, S1_n, ODT0, ODT1, CKE0, CKE1	B, E, F	43, 45, 45
Address/Command	ADD, CMD	A, B, C, D, E, F	46, 46, 47, 47, 48, 48

### 6.2 General Net Structure Routing Rules

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that summarizes the minimum and maximum length for each trace segment in each signal group. The remainder of this section provides a general overview of DDR3 net structure concepts and documents the routing rules to be followed in the design of the DDR3 modules.

#### 6.2.1 Clock, Control, and Address/Command Groups

Rather than the traditional tree structure utilized on legacy DDR modules, the DDR3 modules implement a fly-by topology for routing CK, CTRL, and ADD/CMD signal groups. Compared to legacy modules, the CTRL and ADD/CMD groups on DDR3 modules are length/delay matched to CK—between the connector and each SDRAM—resulting in a significantly reduced timing skew across these groups. This fundamental topology change is instrumental in enabling the higher operating speeds of DDR3. A summary table of the length/delay matching rules associated with these signal groups is provided below.

## 6 DIMM Wiring Details (Cont'd)

**Table 14 — CK, CTRL, and ADD/CMD Group Length Matching Rules**

Signal Group	Matching Rules
CK_t-to-CK_c Matching	Match TLx segment by TLx segment to within 0.1 mm
CK Pair-to-CK Pair Matching (Pair-to-Pair: Average Length)	Match total compensated length from connector to each SDRAM to within 0.25 mm
CTRL Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
CTRL-to-CK Matching	Match total compensated length of all CTRL signals from connector to each SDRAM to within CK $\pm 0.5$ mm
ADR/CMD Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
ADR/CMD-to-CK Matching	Match total compensated length of all ADR/CMD signals from connector to each SDRAM to within CK $\pm 0.5$ mm
TL2 Stub Length Matching	Match TL2 stub length at each SDRAM (top and bottom), on a given signal, to within 0.5 mm
TL2 MAX Stub Length Limits	TL2 $\leq 3.0$ mm
CK First-to-Last Length	Maximum length from first SDRAM and last SDRAM = 153 mm
Neckdown Length	5.0 mm $\leq$ length $\leq$ 10.0 mm; match to within $\pm 1.0$ mm
Note 1 All length matching is done using velocity compensated stripline equivalent lengths Note 2 A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length) Note 3 Neckdown length is the trailing portion of the TL1 segment, which is routed at the standard 0.1 mm width Note 4 Maximum first-to-last length can be calculated by subtracting length to first SDRAM from length to last SDRAM Note 5 Via compensation is not required but is optional; via equivalent length is defined as 2.5 mm of microstrip	

### 6.2.2 Lead-in vs. Loaded Sections

The CK, CTRL, and ADD/CMD topologies are conceptually divided into two topology sections. The segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section, while the segments that run between SDRAM node vias (TL3, TL4, TL5...), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section. The loaded section also contains the segments between the last SDRAM and the termination.

In order to reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, typically with the lead-in section routed at 40 ohms nominal, and the loaded section routed at 60 ohms nominal, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via, which is termed the neckdown length.

### 6.2.3 Length/Delay Matching to SDRAM Devices

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single-best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1 + TL2) be matched across the CK group, and then across the CTRL and ADD/CMD groups—as per the length matching guidelines—adjusting the CK length as needed to reach the length window of the CTRL and ADD/CMD groups. It is important to note that matching is done from connector to the SDRAM ball, and includes the TL2 segment. It is during this process that the breakout pattern dependent length variance in the TL2 stub on each signal will be tuned out.

Once length/delay matching to the first device is complete, the length matching to the remaining devices is straightforward and can be accomplished by simply length-matching the intra-node segments (TL3, TL4, TL5...), assuming the TL2 stub length for a given signal does not vary from SDRAM to SDRAM.

Note that it is recommended that the TL2 stub length on any given signal be closely matched on the top- and bottom-side pattern, and at each SDRAM. This will facilitate the most accurate overall length/delay matching.

The total compensated length from the connector to the first and last SDRAM is documented in the segment length tables for each module type, in the net structure definitions sections; however, it is assumed that the length matching rules are met at all SDRAM devices.

## 6 DIMM Wiring Details (Cont'd)

### 6.2.4 Velocity Compensation

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip (MS) and stripline (SL), the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

### 6.2.5 Load/Delay Compensation

Some newer implementations of the 2R x8 modules implement what is referred to as load/delay compensation across the CLK, CTRL and CMD/ADR signal groups, within the loaded section of the topology. These modules are thereby granted an exception to the original length matching rules shown in table 13. The concept of load/delay compensation refers to the technique whereby the segment lengths between SDRAMs, on the CLK and CTRL signal groups, are purposely lengthened in order to add additional flight time delay, as required to compensate for the fact that the CMD/ADR topology for 2 rank modules has 2 loads (1 top + 1 bottom) for each fly-by node, whereas the CLK and CTRL topologies have only one load per node. Where implemented, the CLK and CTRL segments between SDRAMs shall be routed approximately 4.5mm longer than the corresponding segment on CMD/ADR group. The net result of this compensation is less overall CMD/ADR to CLK skew across the module, thereby improving the ability of the controller to correctly center the CLK within the CMD/ADR valid window.

### 6.2.6 Data and Strobe Group

The DDR3 modules treat each byte lane as a separate signal sub-group, with each byte lane group length/delay matched with velocity compensation as previously described. The length of the individual byte lanes may vary substantially across the module, with the controller providing timing realignment circuitry. A summary table of the length/delay matching rules associated with the data signal group is provided below.

**Table 15 — Data and Strobe Group Length Matching Rules**

Signal Group	Matching Rules
DQS <sub>t</sub> -to-DQS <sub>c</sub> Matching	Match TLx segment by TLx segment to within 0.1 mm
DQ/DM to DQS within Byte Lane	Match total compensated length from the connector to each SDRAM of all DQ and DM signals within a byte lane to within DQS ±0.2 mm
Minimum Byte Lane Length	Minimum compensated length from the connector to the SDRAM shall not be less than 12.0 mm
Maximum Byte Lane Length	Maximum compensated length from the connector to the SDRAM shall not be greater than 32.0 mm
Note 1 All length matching is done using velocity compensated stripline equivalent lengths Note 2 A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length) Note 3 Via compensation is required if the via count varies within a byte lane; via equivalent length = 2.5 mm	

### 6.2.7 Via Compensation

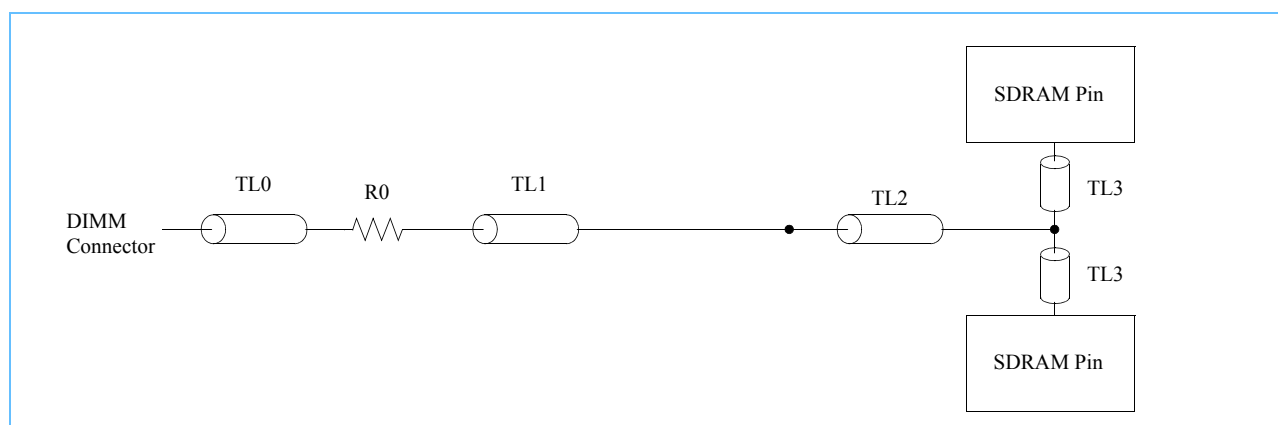
Via compensation on the CK, CTRL, and ADD/CMD signal groups is not required but is to be implemented optionally at the discretion of the module designer. Via compensation is required on the DQ/DQS byte lanes, where the via count varies within a byte lane. This is the case on most single-sided modules. In all cases when via compensation is implemented, the via equivalent shall be defined as 2.5 mm of microstrip.

## 6 DIMM Wiring Details (Cont'd)

### 6.3 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input.



**Figure 18 — Net Structure Example**

A typical data net structure is shown in the following diagram.

6 DIMM Wiring Details (Cont'd)

6.4 Clock Net Structures

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

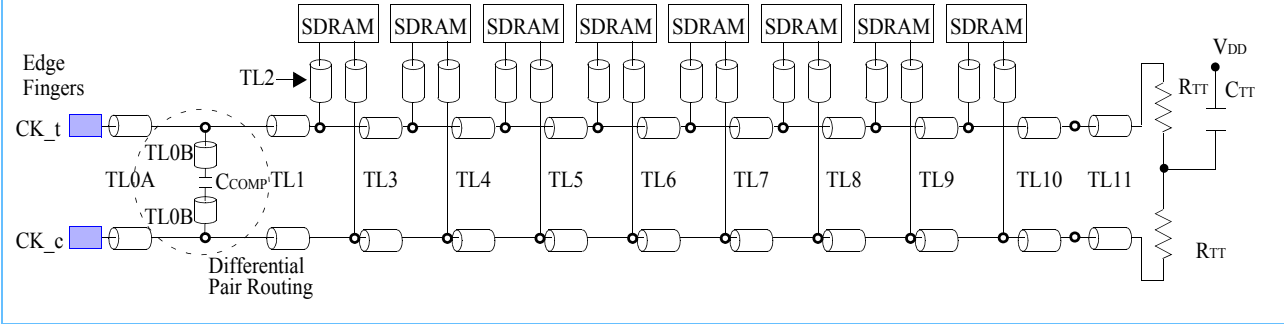


Figure 19 — Clock Net Structures (Raw Card Version A) CK0\_t, CK0\_c

Table 16 — Trace Lengths for Clock Net Structures (Raw Card Version A) CK0\_t, CK0\_c

RC	Length (mm)	TL0 A	TL0 B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	TL10	TL11	CCOMP	RTT	CTT
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL			MS				
A0/A1	MIN	4.2	1.1	94.0	1.0	15.3	15.3	24.8	15.3	15.3	15.3	15.3	98.9	215.5	11.7	0.7	2.2pF	36Ω	0.1μF
	MAX	4.3	1.2	94.1	1.1	15.4	15.4	24.9	15.4	15.4	15.4	15.4	99.0	215.6	11.8	0.8	2.2pF	36Ω	0.1μF

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL1 + TL2/1.1].

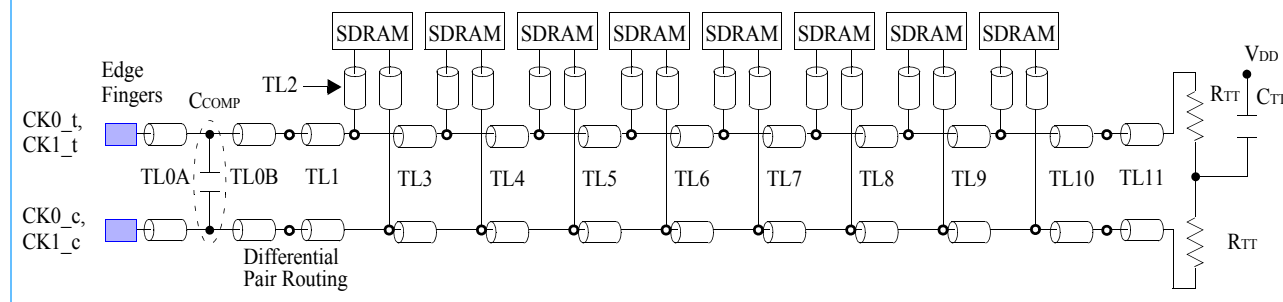
Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9].

Note 4 The pair CK1\_t and CK1\_c is routed to a 75Ω termination resistor but is not connected to any DRAM.

## 6 DIMM Wiring Details (Cont'd)

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew



**Figure 20 — Clock Net Structures (Raw Card Version B) CK0\_t, CK0\_c, CK1\_t, CK1\_c**

**Table 17 — Trace Lengths for Clock Net Structures (Raw Card B)  
CK0\_t, CK0\_c, CK1\_t, CK1\_c**

RC	Length (mm)	TL0 A	TL0 B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	C <sub>COMP</sub>	R <sub>TT</sub>	C <sub>TT</sub>
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	MS						
B0	MIN	3.4	0.7	95.2	1.0	15.6	15.6	15.6	18.1	15.6	15.6	12.1	1.6	102.9	214.9	2.2pF	36Ω	0.1μF	
	MAX	3.4	4.0	95.9	1.2	15.7	15.7	15.7	18.1	15.7	15.7	13.0	1.8	103.0	215.0	2.2pF	36Ω	0.1μF	
B1	MIN	3.4	0.7	95.2	1.0	20.2	20.2	20.2	23.9	20.2	20.2	20.2	12.1	1.6	102.9	248.4	2.2pF	36Ω	0.1μF
	MAX	3.4	4.0	95.9	1.2	20.3	20.3	20.3	24.0	20.3	20.3	13.0	1.8	103.0	248.5	2.2pF	36Ω	0.1μF	

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$

Note 3 Equivalent stripline length to last DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]$

6 DIMM Wiring Details (Cont'd)

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

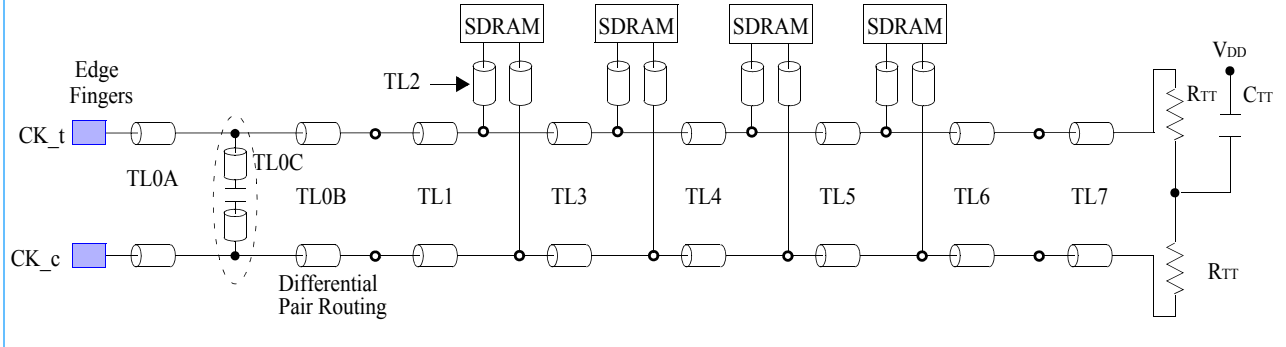


Figure 21 — Clock Net Structures (Raw Card Version C) CK<sub>0\_t</sub>, CK<sub>0\_c</sub>

Table 18 — Trace Lengths for Clock Net Structures (Raw Card C) CK<sub>0\_t</sub>, CK<sub>0\_c</sub>

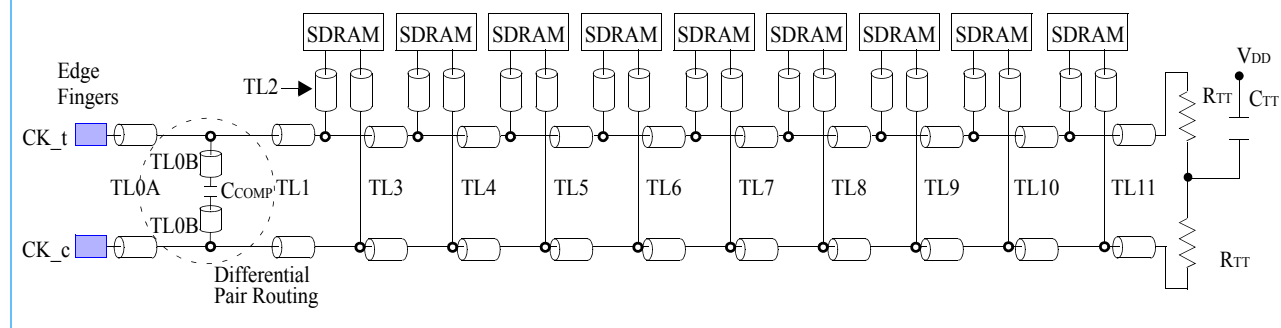
Length (mm)	TL0A	TL0B	TL0C	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	C <sub>COMP</sub>	R <sub>TT</sub>	C <sub>TT</sub>
	MS	MS	MS	SL	MS	SL	SL	SL	SL	MS					
MIN	2.6	35.7	0.7	71.2	1.1	19.0	65.5	19.0	11.8	0.8	109.4	212.9	2.2pF	36Ω	0.1μF
MAX	2.6	35.7	0.8	71.2	1.1	19.0	65.5	19.0	11.8	0.8	109.4	212.9	2.2pF	36Ω	0.1μF

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
 Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + 2.5/1.1 + TL0B/1.1 + TL1 + TL2/1.1]  
 Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + 2.5/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]  
 Note 4 2.5 mm of additional microstrip length is added to compensate for an extra via in the CK path  
 Note 5 The pair CK<sub>1\_t</sub> and CK<sub>1\_c</sub> is routed to a 75Ω termination resistor but is not connected to any DRAM.

## 6 DIMM Wiring Details (Cont'd)

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew



**Figure 22 — Clock Net Structures (Raw Card Version D) CK0\_t, CK0\_c**

**Table 19 — Trace Lengths for Clock Net Structures (Raw Card Version D) CK0\_t, CK0\_c**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	C <sub>COMP</sub>	R <sub>TT</sub>	C <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS						
MIN	2.0	1.3	92.5	2.1	14.0	14.0	14.0	14.0	16.6	14.0	14.0	14.0	10.4	1.4	96.2	210.9	2.2pF	36Ω	0.1μF
MAX	2.1	1.4	92.6	2.2	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	10.5	1.5	96.3	211.0	2.2pF	36Ω	0.1μF

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$ .

Note 3 Equivalent stripline length to last DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]$ .

Note 4 The pair CK1\_t and CK1\_c is routed to a 75Ω termination resistor but is not connected to any DRAM.

6 DIMM Wiring Details (Cont'd)

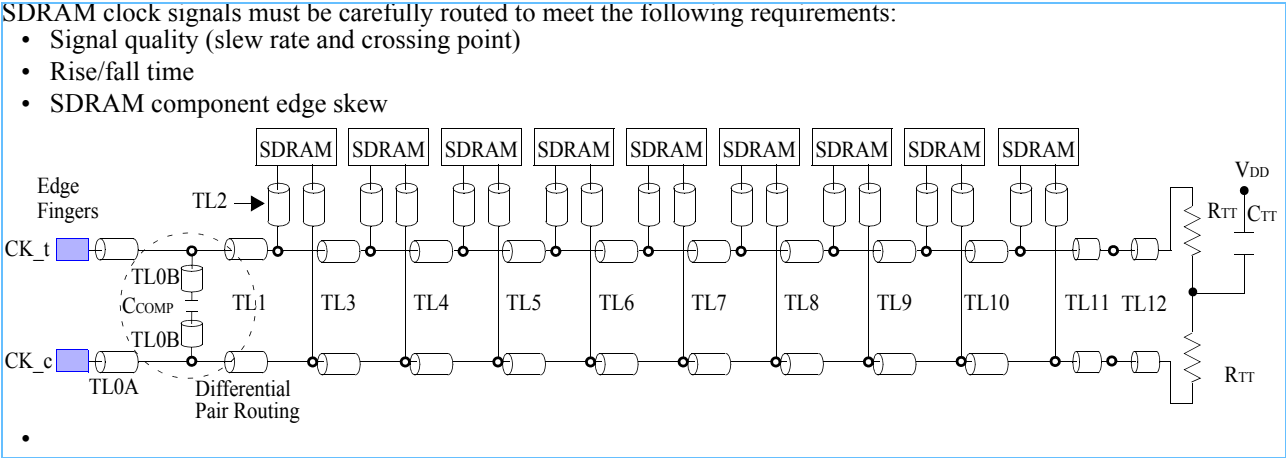


Figure 23 — Clock Net Structures (Raw Card Version E) CK0\_t, CK0\_c, CK1\_t, CK1\_c

Table 20 — Trace Lengths for Clock Net Structures (Raw Card Version E)  
CK0\_t, CK0\_c, CK1\_t, CK1\_c

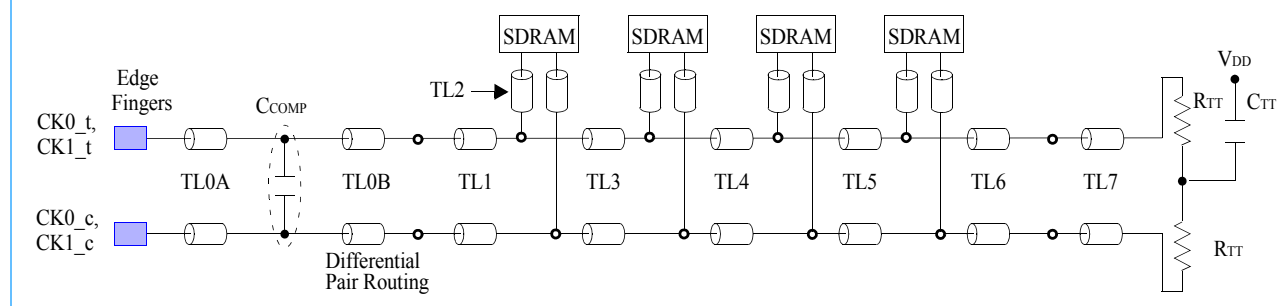
RC	Length (mm)	TL0 A	TL0 B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sub>2</sub>	Last DRAM Compensated <sub>3</sub>	C <sub>COMP</sub> pF	R <sub>TT</sub> Ω	C <sub>TT</sub> uF
E0/E1	MIN	2.1	0.8	95.0	1.9	14.0	14.0	14.0	14.0	18.2	14.0	14.0	14.0	9.1	2.0	100.5	216.8	2.2	36	0.1
	MAX	4.0	1.2	97.0	2.1	14.1	14.1	14.1	14.1	19.1	14.1	14.1	14.1	9.9	2.8	100.6	217.6	2.2	36	0.1
E2	MIN	2.1	0.8	95.0	1.9	18.6	18.6	18.6	18.6	26.3	18.6	18.6	18.6	9.1	2.0	100.5	257.1	2.2	36	0.1
	MAX	4.0	1.2	97.0	2.1	18.7	18.7	18.7	18.7	26.4	18.7	18.7	18.7	9.9	2.8	100.6	258.9	2.2	36	0.1
E3	MIN	2.8	0.7	95.8	1.9	18.6	18.6	18.6	18.6	26.3	18.6	18.6	18.6	10.8	0.6	100.5	257.0	2.2	36	0.1
	MAX	3.1	1.1	96.3	2.2	18.7	18.7	18.7	18.7	26.4	18.7	18.7	18.7	12.0	0.8	100.6	257.1	2.2	36	0.1

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
 Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]  
 Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]

## 6 DIMM Wiring Details (Cont'd)

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew



**Figure 24 — Clock Net Structures (Raw Card Version F) CK0\_t, CK0\_c, CK1\_t, CK1\_c**

**Table 21 — Trace Lengths for Clock Net Structures (Raw Card Version F)  
CK0\_t, CK0\_c, CK1\_t, CK1\_c**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	C <sub>COMP</sub>	R <sub>TT</sub>	C <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	MS						
MIN	3.4	30.4	78.9	1.0	19.6	67.8	19.6	16.2	0.8	112.8	219.8	2.2pF	36Ω	0.1μF
MAX	3.4	30.4	78.9	1.0	19.6	67.8	19.6	16.2	0.8	112.8	219.8	2.2pF	36Ω	0.1μF

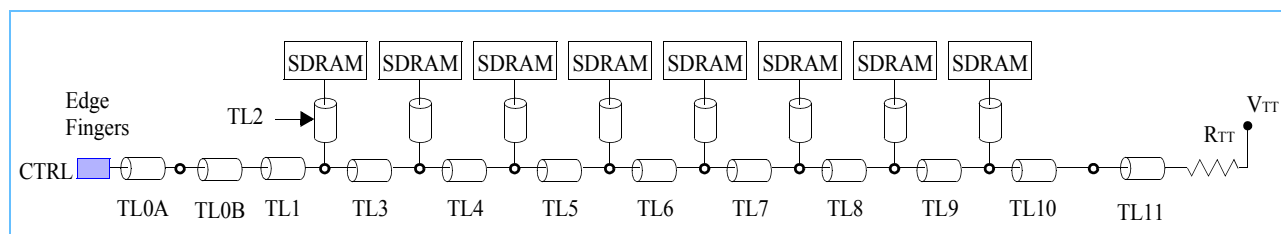
Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]

## 6 DIMM Wiring Details (Cont'd)

### 6.5 Net Structure Routing for Control



**Figure 25 — Net Structure Routing for Control (Raw Card Version A)  
S0\_n, ODT0 and CKE0**

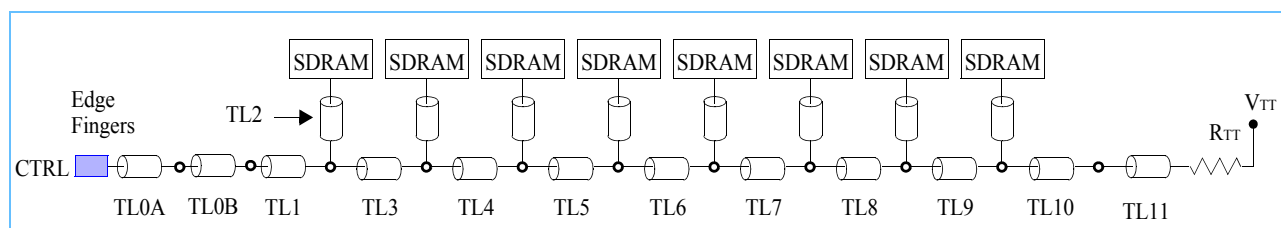
**Table 22 — Trace Lengths for Control Net Structures (Raw Card Version A)  
S0\_n, ODT0 and CKE0**

RC	Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	MS				
A0/A1	MIN	2.0	0.0	92.0	0.5	15.3	15.3	15.3	24.8	15.3	15.3	15.3	4.3	0.7	98.7	215.5	39Ω
	MAX	6.6	0.0	96.4	0.6	15.4	15.4	15.4	24.9	15.4	15.4	15.4	11.8	1.1	98.7	215.5	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]



**Figure 26 — Net Structure Routing for Control (Raw Card Version B)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, and CKE1**

**Table 23 — Trace Lengths for Control Net Structures (Raw Card Version B)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, and CKE1**

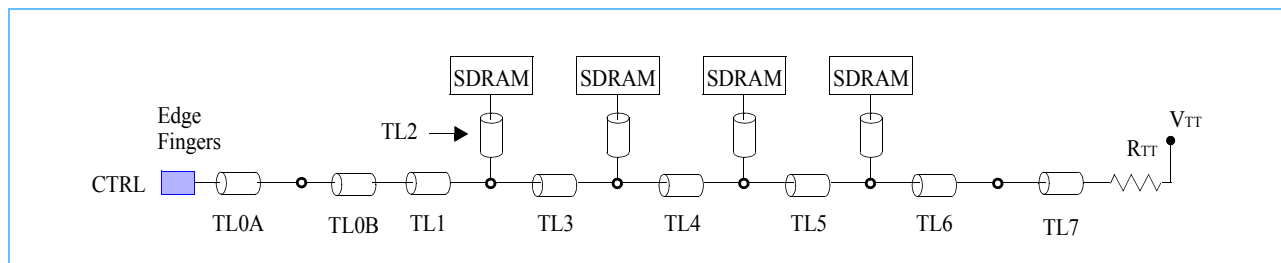
RC	Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	MS				
B0	MIN	1.6	0.0	91.9	0.6	15.6	15.6	15.6	18.1	15.6	15.6	15.6	6.0	0.9	102.9	215.0	39Ω
	MAX	6.6	7.1	100.8	0.8	15.7	15.7	15.7	18.2	15.7	15.7	15.7	14.9	1.8	103.0	215.1	39Ω
B1	MIN	1.6	0.0	91.9	0.6	20.2	20.2	20.2	23.9	20.2	20.2	20.2	6.0	0.9	102.9	248.4	39Ω
	MAX	6.6	7.1	100.8	0.8	20.3	20.3	20.3	24.0	20.3	20.3	20.3	14.9	1.8	103.0	248.5	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

## 6 DIMM Wiring Details (Cont'd)



**Figure 27 — Net Structure Routing for Control (Raw Card Version C)  
S0\_n, ODT0 and CKE0**

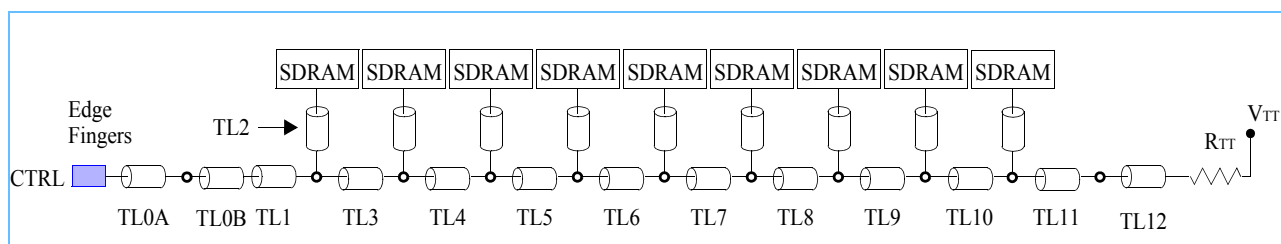
**Table 24 — Trace Lengths for Control Net Structures (Raw Card Version C)  
S0\_n, ODT0 and CKE0**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	34.1	0.0	57.1	1.2	19.0	65.5	19.0	13.3	0.7	107.0	210.5	36Ω
MAX	53.6	0.0	74.8	1.4	19.0	65.5	19.0	13.8	1.3	107.0	210.5	36Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]



**Figure 28 — Net Structure Routing for Control (Raw Card Version D)  
S0\_n, ODT0 and CKE0**

**Table 25 — Trace Lengths for Control Net Structures (Raw Card Version D)  
S0\_n, ODT0 and CKE0**

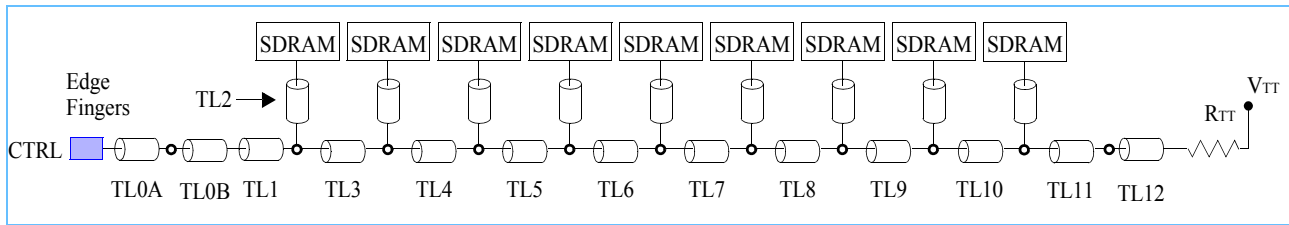
Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS				
MIN	2.0	0.0	0.0	0.5	13.9	13.9	13.9	13.9	16.6	13.9	13.9	13.9	4.0	2.0	96.1	210.7	39Ω
MAX	104.6	0.0	94.0	2.3	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	10.2	3.0	96.4	211.1	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]

6 DIMM Wiring Details (Cont'd)



**Figure 29 — Net Structure Routing for Control (Raw Card Version E)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, CKE1**

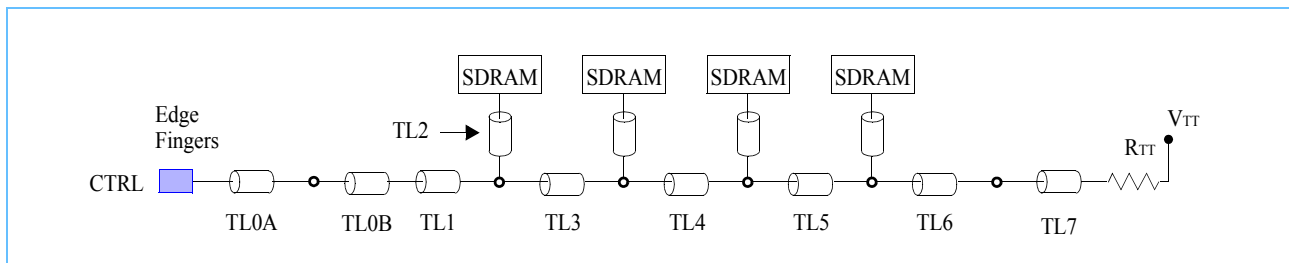
**Table 26 — Trace Lengths for Control Net Structures (Raw Card Version E)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, and CKE1**

RC	Length (mm)	TL0 A	TL0 B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub> Ω
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	MS					
E0/E1	MIN	9.7	0.0	17.4	0.5	14.0	14.0	14.0	14.0	18.9	14.0	14.0	14.0	2.8	1.3	100.5	216.2	39
	MAX	90.6	0.0	91.2	1.4	14.1	14.1	14.1	14.1	19.0	14.1	14.1	14.1	12.4	2.5	100.6	217.6	39
E2	MIN	9.7	0.0	17.4	0.5	18.6	18.6	18.6	18.6	26.3	18.6	18.6	18.6	2.8	1.3	100.5	255.8	39
	MAX	90.6	0.0	91.2	1.4	18.7	18.7	18.7	18.7	26.4	18.7	18.7	18.7	12.4	2.5	100.6	257.2	39
E3	MIN	9.7	0.0	16.9	0.5	18.6	18.6	18.6	18.6	26.3	18.6	18.6	18.6	3.0	1.2	100.5	257.0	39
	MAX	91.2	0.0	91.3	1.4	18.7	18.7	18.7	18.7	26.4	18.7	18.7	18.7	12.4	2.2	100.6	257.1	39

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]



**Figure 30 — Net Structure Routing for Control (Raw Card Version F)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, CKE1**

**Table 27 — Trace Lengths for Control Net Structures (Raw Card Version F)  
S0\_n, S1\_n, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	1.9	0.0	64.8	2.2	19.6	67.8	19.6	13.3	0.7	112.8	219.7	39Ω
MAX	50.9	43.9	93.7	2.2	19.6	67.8	19.6	13.8	1.3	113.0	220.0	39Ω

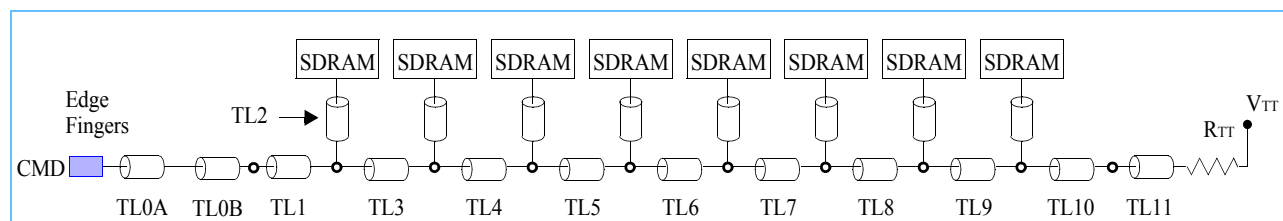
Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]

## 6 DIMM Wiring Details (Cont'd)

### 6.6 Net Structure Routing for Address/Command



**Figure 31 — Net Structure Routing for Address and Command (Raw Card Version A)**

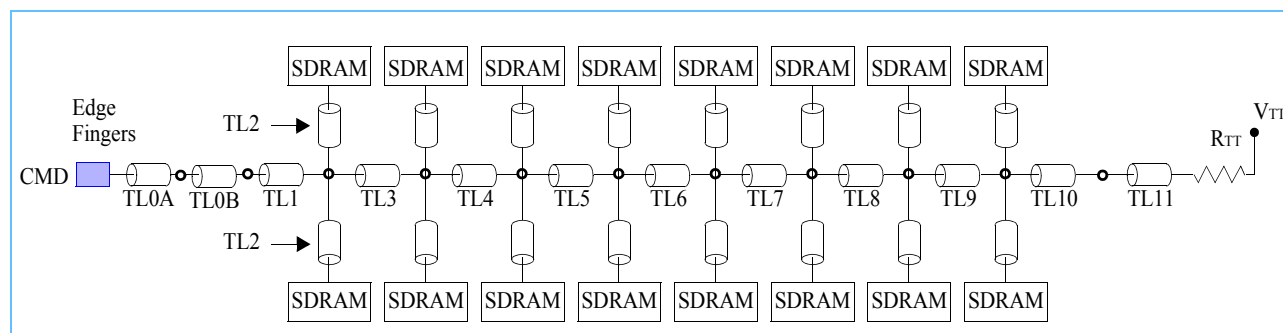
**Table 28 — Trace Lengths for Address and Command Net Structures (Raw Card Version A)**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	1.9	0.0	9.0	0.5	15.3	15.3	15.3	24.8	15.3	15.3	15.3	3.6	0.7	98.6	215.4	39Ω
MAX	98.1	0.0	95.7	2.3	15.4	15.4	15.4	24.9	15.4	15.4	15.4	12.5	1.9	98.7	216.0	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]



**Figure 32 — Net Structure Routing for Address and Command (Raw Card Version B)**

**Table 29 — Trace Lengths for Address and Command Net Structures (Raw Card Version B)**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	1.6	0.0	8.6	1.6	15.6	15.6	15.6	18.1	15.6	15.6	15.6	4.3	0.8	102.6	214.6	39Ω
MAX	102.0	97.3	79.6	2.4	15.7	15.7	15.7	18.2	15.7	15.7	15.7	13.2	1.7	103.5	215.5	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

6 DIMM Wiring Details (Cont'd)

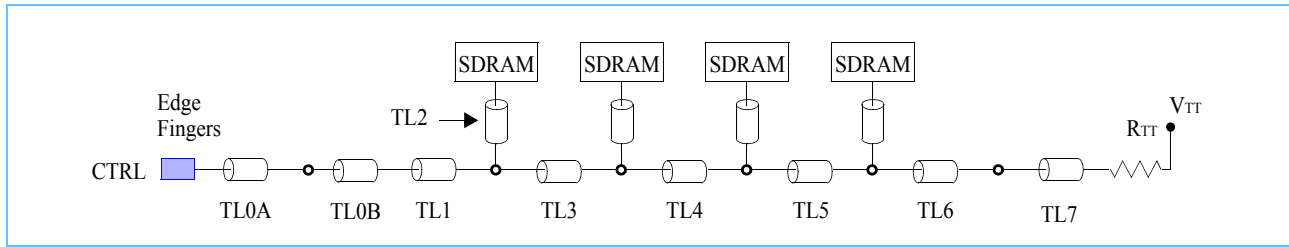


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version C)

Table 30 — Trace Lengths for Address and Command Net Structures (Raw Card Version C)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	4.0	0.0	41.3	2.5	19.0	65.5	19.0	13.3	0.7	107.0	210.5	39Ω
MAX	69.8	0.0	100.6	3.0	19.0	65.5	19.0	13.8	1.3	107.0	210.5	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
 Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]  
 Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]  
 Note 4 A15 is not routed on the module

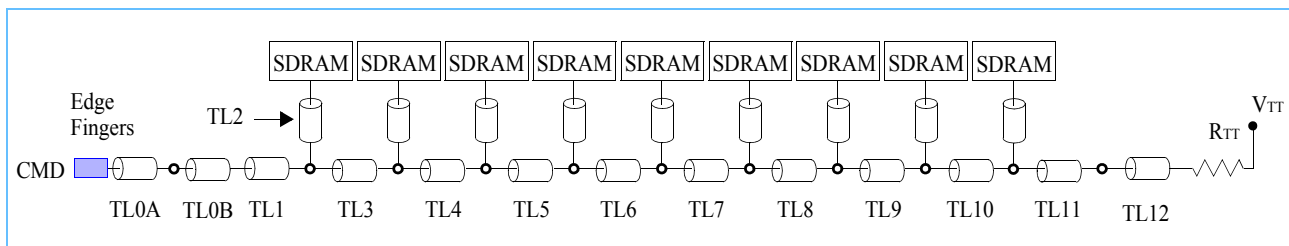


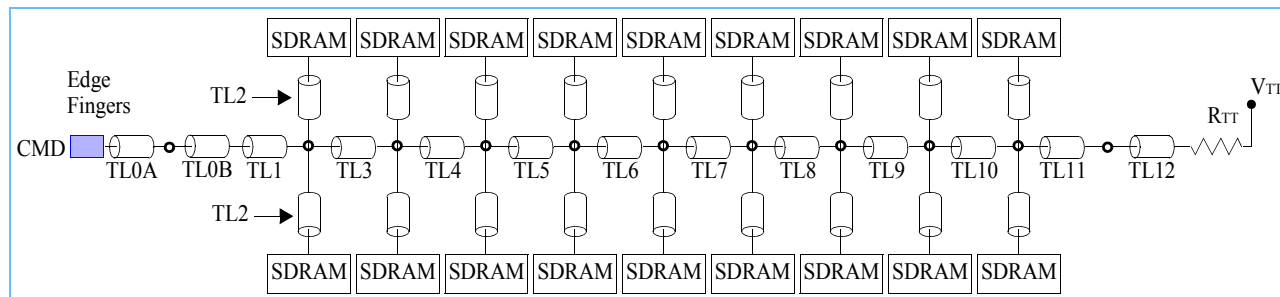
Figure 34 — Net Structure Routing for Address and Command (Raw Card Version D)

Table 31 — Trace Lengths for Address and Command Net Structures (Raw Card Version D)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS				
MIN	2.0	0.0	0.0	0.5	13.9	13.9	13.9	13.9	16.6	13.9	13.9	13.9	5.3	1.0	96.1	210.7	39Ω
MAX	104.6	0.0	94.0	2.3	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	13.0	2.1	96.4	211.1	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
 Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].  
 Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10].  
 Note 4 R<sub>TT</sub> resistor tolerance is 2 percent.

### 6 DIMM Wiring Details (Cont'd)



**Figure 35 — Net Structure Routing for Address and Command (Raw Card Version E)**

**Table 32 — Trace Lengths for Address and Command Net Structures (Raw Card Version E)**

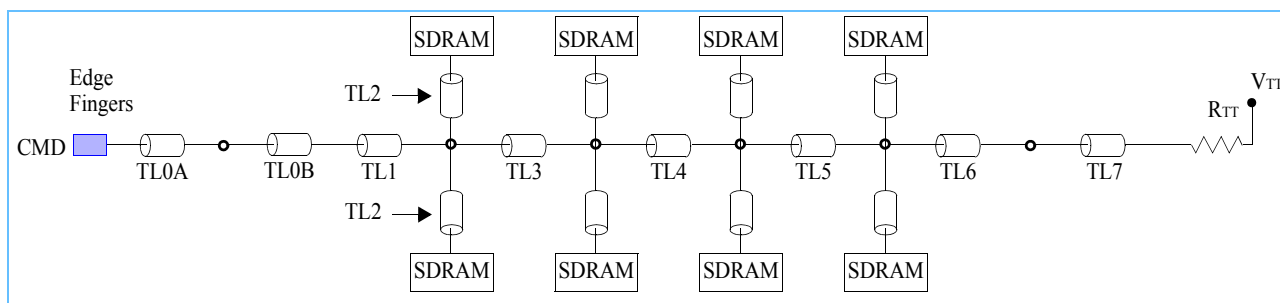
RC	Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
		MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS				
E0/E1/E2	MIN	9.7	0.0	17.4	0.5	14.0	14.0	14.0	13.9	18.9	14.0	14.0	14.0	5.2	1.2	100.5	216.2	39Ω
	MAX	90.6	0.0	91.2	3.0	14.1	14.1	14.1	14.1	19.0	14.1	14.1	14.1	11.6	2.7	100.6	217.6	39Ω
E3	MIN	2.2	0.0	19.0	0.5	14.0	14.0	14.0	14.0	18.9	14.0	14.0	14.0	5.1	1.2	100.5	217.4	39Ω
	MAX	87.4	0.0	98.1	3.0	14.1	14.1	14.1	14.1	19.0	14.1	14.1	14.1	11.7	2.7	100.6	217.5	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10].

Note 4 R<sub>TT</sub> resistor tolerance is 2 percent.



**Figure 36 — Net Structure Routing for Address and Command (Raw Card Version F)**

**Table 33 — Trace Lengths for Address and Command Net Structures (Raw Card Version F)**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated <sup>2</sup>	Last DRAM Compensated <sup>3</sup>	R <sub>TT</sub>
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	8.7	0.0	9.8	2.0	19.6	67.8	19.6	13.3	0.7	113.0	220.0	39Ω
MAX	111.5	0.0	102.6	2.8	19.6	67.8	19.6	13.8	1.3	113.0	220.0	39Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

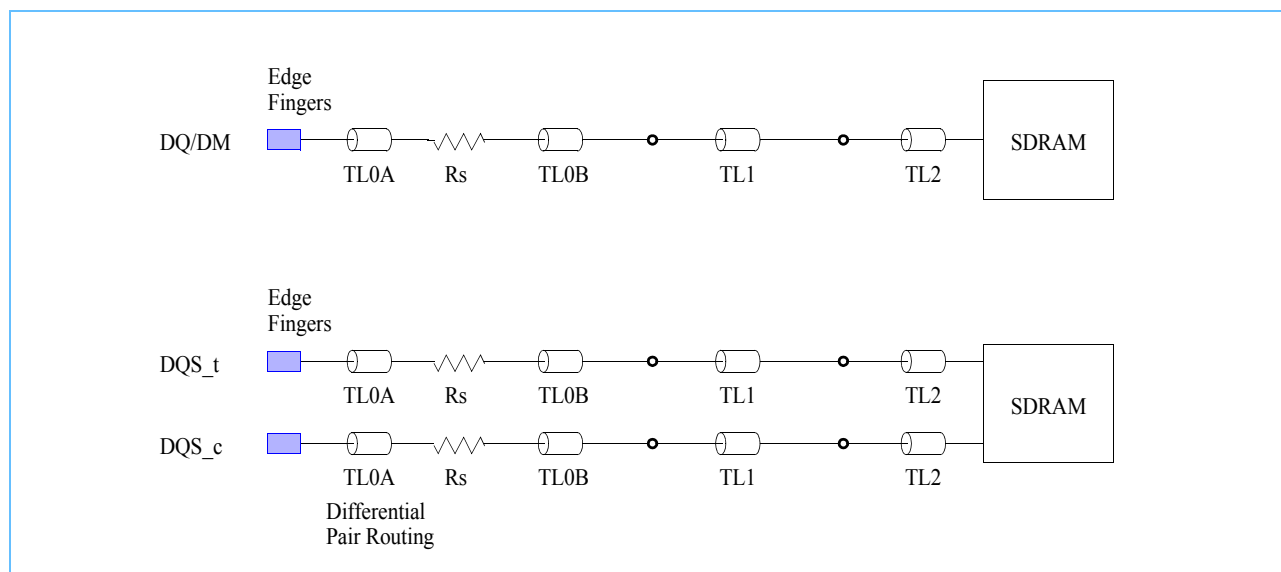
Note 2 Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

Note 3 Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5].

Note 4 A15 is not routed.

## 6 DIMM Wiring Details (Cont'd)

### 6.7 Net Structure Routing for Data



**Figure 37 — Net Structure Routing for Data (Raw Card Version A)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub>**

**Table 34 — Trace Lengths for Data Net Structures (Raw Card Version A)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub>**

DQ0–DQ7, DM0, DQS0 <sub>t</sub> , DQS0 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	R <sub>s</sub>
	MS	MS	SL	MS		
MIN	3.0	1.0	9.5	0.5	16.8	15Ω
MAX	3.2	1.6	12.6	1.1	16.8	15Ω
DQ8–DQ15, DM1, DQS1 <sub>t</sub> , DQS1 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	R <sub>s</sub>
	MS	MS	SL	MS		
MIN	3.0	0.9	12.2	0.5	19.8	15Ω
MAX	3.2	1.9	15.6	1.0	19.8	15Ω
DQ16–DQ23, DM2, DQS2 <sub>t</sub> , DQS2 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	R <sub>s</sub>
	MS	MS	SL	MS		
MIN	3.1	0.9	15.8	0.5	23.2	15Ω
MAX	3.2	1.8	19.2	1.1	23.2	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$ .

6 DIMM Wiring Details (Cont'd)

**Table 34 — Trace Lengths for Data Net Structures (Raw Card Version A)  
DQ/DM and DQS\_t/DQS\_c**

DQ24–DQ31, DM3, DQS3_t, DQS3_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.0	1.1	20.8	0.5	28.1	15Ω
MAX	3.2	2.0	23.4	0.6	28.1	15Ω

DQ32–DQ39, DM4, DQS4_t, DQS4_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	0.9	19.2	0.5	26.7	15Ω
MAX	3.2	1.9	22.5	1.0	26.7	15Ω

DQ40–DQ47, DM5, DQS5_t, DQS5_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.0	0.9	14.8	0.5	22.1	15Ω
MAX	3.2	2.0	17.9	1.0	22.1	15Ω

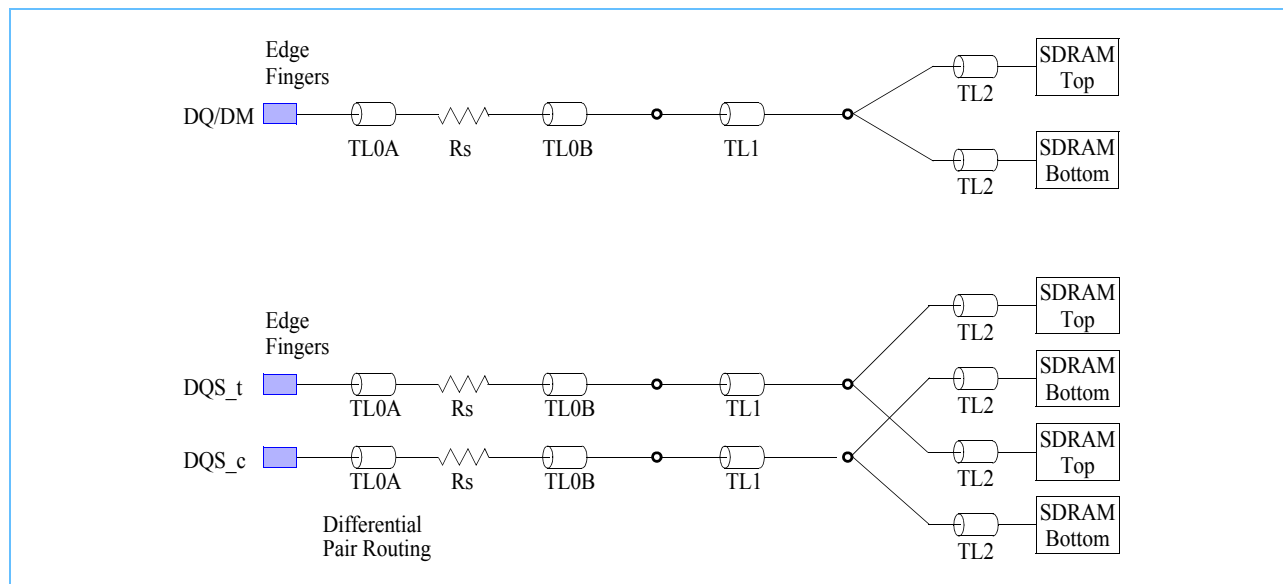
DQ48–DQ55, DM6, DQS6_t, DQS6_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.0	1.0	11.1	0.5	18.5	15Ω
MAX	3.2	1.6	14.3	1.1	18.5	15Ω

DQ56–DQ63, DM7, DQS7_t, DQS7_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.0	0.9	9.5	0.5	16.9	15Ω
MAX	3.2	1.6	12.7	1.0	16.9	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)



**Figure 38 — Net Structure Routing for Data (Raw Card Version B)  
DQ/DM and DQS\_t/DQS\_c**

**Table 35 — Trace Lengths for Data Net Structures (Raw Card Version B)  
DQ/DM and DQS\_t/DQS\_c**

DQ0–DQ7, DM0, DQS0_t, DQS0_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	10.2	0.6	16.0	15Ω
MAX	3.9	1.7	11.9	1.8	16.1	15Ω

DQ8–DQ15, DM1, DQS1_t, DQS1_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	13.5	0.6	19.3	15Ω
MAX	3.9	1.7	15.0	1.8	19.4	15Ω

DQ16–DQ23, DM2, DQS2_t, DQS2_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	19.4	0.6	25.2	15Ω
MAX	3.9	1.7	20.9	1.8	25.3	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$ .

6 DIMM Wiring Details (Cont'd)

**Table 35 — Trace Lengths for Data Net Structures (Raw Card Version B)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub> (Cont'd)**

DQ24–DQ31, DM3, DQS3 <sub>t</sub> , DQS3 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	25.1	0.6	30.9	15Ω
MAX	3.9	1.7	26.7	1.8	31.0	15Ω

DQ32–DQ39, DM4, DQS4 <sub>t</sub> , DQS4 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	23.2	0.6	29.0	15Ω
MAX	3.9	1.7	25.0	1.8	29.1	15Ω

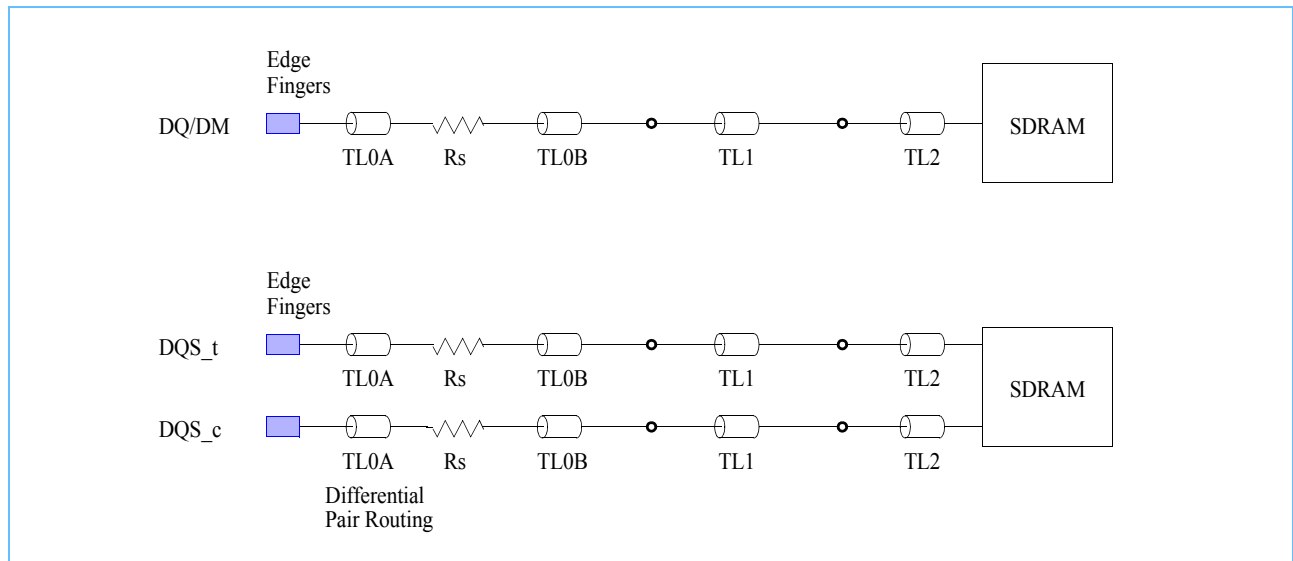
DQ40–DQ47, DM5, DQS5 <sub>t</sub> , DQS5 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	17.3	0.6	23.1	15Ω
MAX	3.9	1.7	18.9	1.8	23.2	15Ω

DQ48–DQ55, DM6, DQS6 <sub>t</sub> , DQS6 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	11.6	0.6	17.4	15Ω
MAX	3.9	1.7	13.1	1.8	17.5	15Ω

DQ56–DQ63, DM7, DQS7 <sub>t</sub> , DQS7 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	0.9	8.0	0.6	14.8	15Ω
MAX	3.9	1.7	10.9	1.8	15.1	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)



**Figure 39 — Net Structure Routing for Data (Raw Card Version C)  
DQ/DM and DQS\_t/DQS\_c**

**Table 36 — Trace Lengths for Data Net Structures (Raw Card Version C)  
DQ/DM and DQS\_t/DQS\_c**

DQ0–DQ7, DM0, DQS0_t, DQS0_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ8–DQ15, DM1, DQS1_t, DQS1_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

DQ16–DQ23, DM2, DQS2_t, DQS2_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$ .

6 DIMM Wiring Details (Cont'd)

**Table 36 — Trace Lengths for Data Net Structures (Raw Card Version C)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub> (Cont'd)**

DQ24–DQ31, DM3, DQS3 <sub>t</sub> , DQS3 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

DQ32–DQ39, DM4, DQS4 <sub>t</sub> , DQS4 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ40–DQ47, DM5, DQS5 <sub>t</sub> , DQS5 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

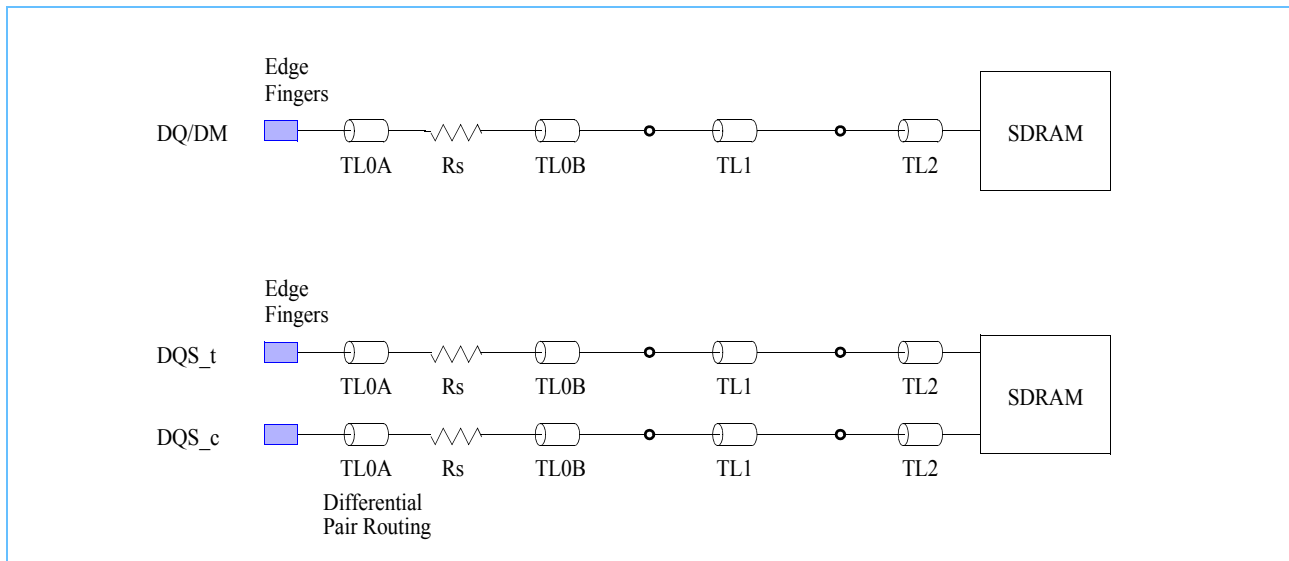
DQ48–DQ55, DM6, DQS6 <sub>t</sub> , DQS6 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ56–DQ63, DM7, DQS7 <sub>t</sub> , DQS7 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)



**Figure 40 — Net Structure Routing for Data (Raw Card Version D)  
DQ/DM and DQS\_t/DQS\_c**

**Table 37 — Trace Lengths for Data Net Structures (Raw Card Version D)  
DQ/DM and DQS\_t/DQS\_c**

DQ0–DQ7, DM0, DQS0_t, DQS0_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	11.4	0.5	17.4	15Ω
MAX	3.9	1.5	13.3	1.9	17.5	15Ω

DQ8–DQ15, DM1, DQS1_t, DQS1_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	13.5	0.5	19.4	15Ω
MAX	3.3	1.5	15.6	1.9	19.6	15Ω

DQ16–DQ23, DM2, DQS2_t, DQS2_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	17.0	0.5	23.0	15Ω
MAX	3.3	1.5	19.1	1.9	23.1	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)

**Table 37 — Trace Lengths for Data Net Structures (Raw Card Version D)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub> (Cont'd)**

DQ24–DQ31, DM3, DQS3 <sub>t</sub> , DQS3 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	20.7	0.5	26.7	15Ω
MAX	3.5	1.5	22.8	1.9	26.8	15Ω

DQ32–DQ39, DM4, DQS4 <sub>t</sub> , DQS4 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	20.8	0.5	26.7	15Ω
MAX	4.4	1.8	22.9	1.9	26.9	15Ω

DQ40–DQ47, DM5, DQS5 <sub>t</sub> , DQS5 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	17.0	0.5	23.0	15Ω
MAX	4.4	1.7	19.0	1.9	23.1	15Ω

DQ48–DQ55, DM6, DQS6 <sub>t</sub> , DQS6 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	13.3	0.5	19.4	15Ω
MAX	4.4	2.8	15.6	1.9	19.6	15Ω

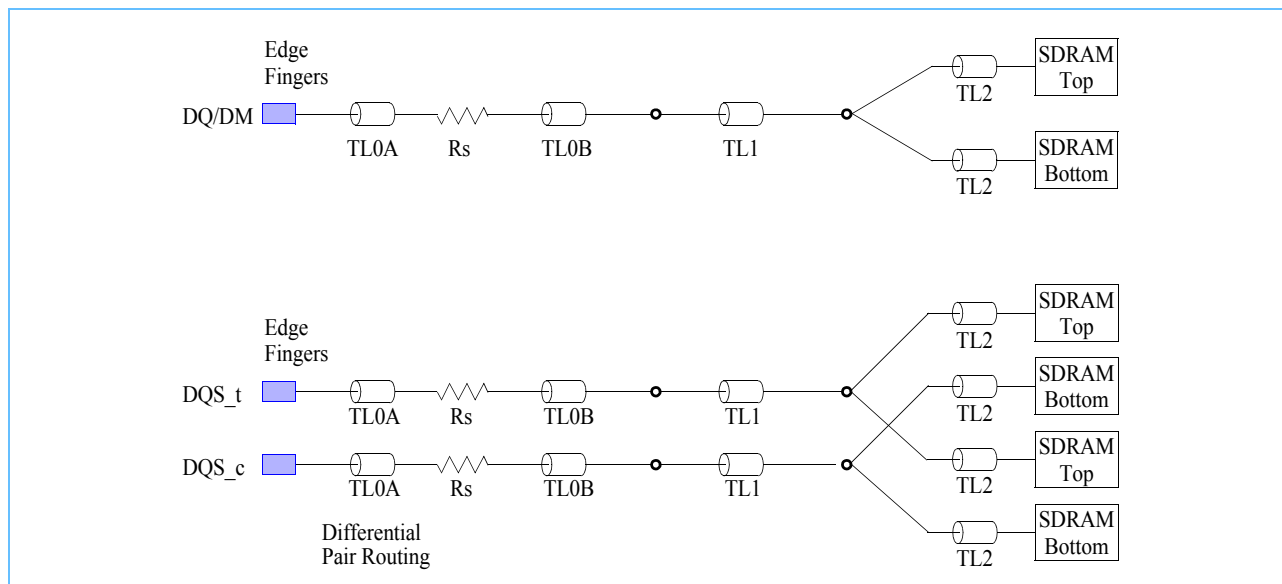
DQ56–DQ63, DM7, DQS7 <sub>t</sub> , DQS7 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	11.5	0.5	17.4	15Ω
MAX	4.4	1.8	13.5	1.9	17.5	15Ω

CB0–DQ7, DM8, DQS8 <sub>t</sub> , DQS8 <sub>c</sub>						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	24.4	0.5	30.4	15Ω
MAX	3.6	1.5	26.4	1.9	30.5	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)



**Figure 41 — Net Structure Routing for Data (Raw Card Version E)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub>**

**Table 38 — Trace Lengths for Data Net Structures (Raw Card Version E)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub>**

DQ0–DQ7, DM0, DQS0 <sub>t</sub> , DQS0 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	11.4	0.5	17.3	15Ω
	MAX	4.2	1.6	13.4	1.9	17.4	15Ω
E3	MIN	3.0	0.6	11.7	0.5	18.9	15Ω
	MAX	3.3	1.0	15.1	1.9	19.1	15Ω

DQ8–DQ15, DM1, DQS1 <sub>t</sub> , DQS1 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	13.5	0.5	19.3	15Ω
	MAX	3.3	1.5	15.5	1.9	19.5	15Ω
E3	MIN	2.9	0.6	12.6	0.5	19.9	15Ω
	MAX	3.3	1.0	16.1	1.9	20.1	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
 Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)

**Table 38 — Trace Lengths for Data Net Structures (Raw Card Version E)  
DQ/DM and DQS<sub>t</sub>/DQS<sub>c</sub> (Cont'd)**

DQ16–DQ23, DM2, DQS2 <sub>t</sub> , DQS2 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	17.0	0.5	22.9	15Ω
	MAX	3.2	1.4	19.0	1.9	23.0	15Ω
E3	MIN	2.9	0.6	15.8	0.5	23.1	15Ω
	MAX	3.3	1.0	19.4	1.9	23.3	15Ω

DQ24–DQ31, DM3, DQS3 <sub>t</sub> , DQS3 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	20.8	0.5	26.6	15Ω
	MAX	3.4	1.7	22.7	1.9	26.8	15Ω
E3	MIN	2.9	0.6	19.8	0.5	27.1	15Ω
	MAX	3.3	1.0	23.3	1.9	27.3	15Ω

DQ32–DQ39, DM4, DQS4 <sub>t</sub> , DQS4 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.6	20.6	0.5	26.6	15Ω
	MAX	4.3	1.5	22.8	1.9	26.8	15Ω
E3	MIN	2.9	0.6	19.3	0.5	26.6	15Ω
	MAX	3.3	1.0	22.8	1.9	26.7	15Ω

DQ40–DQ47, DM5, DQS5 <sub>t</sub> , DQS5 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	16.9	0.5	22.9	15Ω
	MAX	4.3	1.7	18.9	1.9	23.0	15Ω
E3	MIN	2.9	0.6	15.6	0.5	22.9	15Ω
	MAX	3.3	1.0	19.1	1.9	23.0	15Ω

DQ48–DQ55, DM6, DQS6 <sub>t</sub> , DQS6 <sub>c</sub>							
RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	13.3	0.5	19.3	15Ω
	MAX	4.3	1.8	15.5	1.9	19.5	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

6 DIMM Wiring Details (Cont'd)

**Table 38 — Trace Lengths for Data Net Structures (Raw Card Version E)  
DQ/DM and DQS\_t/DQS\_c (Cont'd)**

E3	MIN	2.9	0.6	12.0	0.5	19.3	15Ω
	MAX	3.3	1.0	15.5	1.9	19.4	15Ω

DQ56–DQ63, DM7, DQS7\_t, DQS7\_c

RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.7	11.2	0.5	17.3	15Ω
	MAX	4.3	1.8	13.4	1.9	17.4	15Ω
E3	MIN	2.9	0.6	10.0	0.5	17.3	15Ω
	MAX	3.3	1.0	13.5	1.9	17.4	15Ω

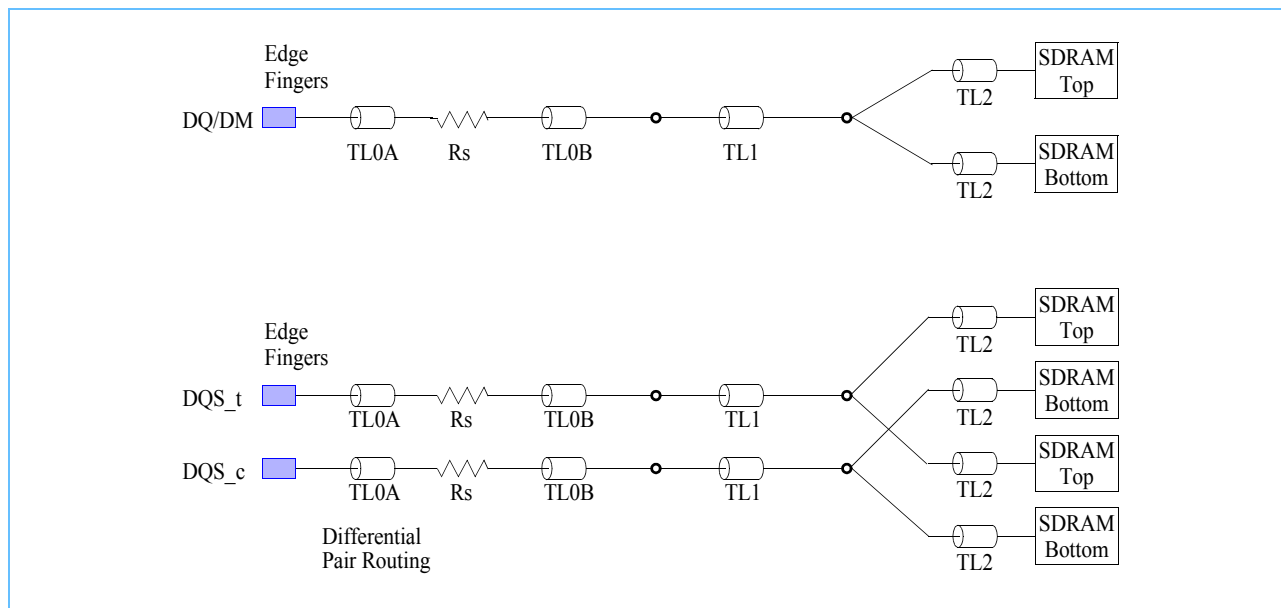
CB0–CB7, DM8, DQS8\_t, DQS8\_c

RC	Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
		MS	MS	SL	MS		
E0/E1/E2	MIN	2.9	0.6	24.4	0.5	30.4	15Ω
	MAX	3.6	1.5	26.4	1.9	30.5	15Ω
E3	MIN	2.9	0.6	23.2	0.5	30.5	15Ω
	MAX	3.3	1.0	26.9	1.9	30.7	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

## 6 DIMM Wiring Details (Cont'd)



**Figure 42 — Net Structure Routing for Data (Raw Card Version F)  
DQ/DM and DQS\_t/DQS\_c**

**Table 39 — Trace Lengths for Data Net Structures (Raw Card Version F)  
DQ/DM and DQS\_t/DQS\_c**

DQ0–DQ7, DM0, DQS0_t, DQS0_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ8–DQ15, DM1, DQS1_t, DQS1_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ16–DQ23, DM2, DQS2_t, DQS2_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.

Note 2 Equivalent stripline length to DRAM  $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$ .

6 DIMM Wiring Details (Cont'd)

**Table 39 — Trace Lengths for Data Net Structures (Raw Card Version F)  
DQ/DM and DQS\_t/DQS\_c (Cont'd)**

DQ24–DQ31, DM3, DQS3_t, DQS3_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ32–DQ39, DM4, DQS4_t, DQS4_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ40–DQ47, DM5, DQS5_t, DQS5_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ48–DQ55, DM6, DQS6_t, DQS6_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ56–DQ63, DM7, DQS7_t, DQS7_c						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated <sup>2</sup>	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

Note 1 Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.  
Note 2 Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

## 6 DIMM Wiring Details (Cont'd)

### 6.8 Cross Section Recommendations

DIMM printed circuit board designs use six-layers or eight-layers of glass epoxy materl PCB.

**Table 40 — Six-Layer Geometry and Impedance Targets(Raw Cards A0, B0, C0, D0, F0)**

Layer	Single-Ended		Differential	
	Width	Target Zo	Width/Space	Target Z <sub>DIFF</sub>
L1	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
L3	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
	0.17 mm	49Ω ±15%		
L4	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
	0.17 mm	49Ω ±15%		
L6	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
	0.17 mm	49Ω ±15%		

Note 1 All impedances other than the basic single-ended 60 ohms target are provided for reference only.  
Note 2 Due to the light load on Raw Cards A, C, and D (1 rank), the impedance of the command and address traces through the DRAM area is 49 ohms rather than 60 ohms.

**Table 41 — Six-Layer Geometry and Impedance Targets(Raw Cards A1, B1, D1, E3)**

Layer	Single-Ended		Differential	
	Width	Target Zo	Width/Space	Target Z <sub>DIFF</sub>
L1	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
L3	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
	0.127 mm	49Ω ±15%		
L4	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
	0.127 mm	49Ω ±15%		
L6	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%

Note 1 All impedances other than the basic single-ended 60 ohms target are provided for reference only.  
Note 2 Due to the light load on Raw Cards A, and D (1 rank), the impedance of the command and address traces through the DRAM area is 49 ohms rather than 60 ohms.

6 DIMM Wiring Details (Cont'd)

Stackup 1 (For use with wider lines)				Stackup 2 (For use with thinner lines)			
Mask		0.015 mm		Mask		0.015 mm	
L1	Cu	0.045 mm	Signal Layer 0.5oz. + Plating	L1	Cu	0.045 mm	
	Prepreg	0.1 mm			Prepreg	0.08 mm	
L2	Cu	0.03 mm	V <sub>DD</sub> /V <sub>SS</sub> 1oz.	L2	Cu	0.03 mm	
	Core	0.127 mm			Core	0.1 mm	
L3	Cu	0.03 mm	Signal 1oz.	L3	Cu	0.03 mm	
	Prepreg	0.6 mm			Prepreg	0.7 mm	
L4	Cu	0.03 mm	Signal 1oz.	L4	Cu	0.03 mm	
	Core	0.127 mm			Core	0.1 mm	
L5	Cu	0.03 mm	V <sub>DD</sub> /V <sub>SS</sub> 1oz.	L5	Cu	0.03 mm	
	Prepreg	0.1 mm			Prepreg	0.08 mm	
L6	Cu	0.045 mm	Signal 0.5oz. + Plating	L6	Cu	0.045 mm	
	Mask	0.015 mm			Mask	0.015 mm	

Note 1. Overall Thickness = 1.27 mm ±0.1 mm.  
 Note 2. RC's A0, B0, C0, D0, F0 use Stackup 1.  
 Note 3. RC A1, B1, D1, E3 use Stackup 2.

Figure 43 — Six-Layer Stackup (Example)

6 DIMM Wiring Details (Cont'd)

**Table 42 — Eight-Layer Geometry and Impedance Targets(Raw Cards E0, E1)**

Layer	Single-Ended		Differential	
	Width	Target $Z_0$	Width/Space	Target $Z_{DIFF}$
L1	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L3	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L6	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L8	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%

Note 1 All impedances other than the basic single-ended 60Ω target are provided for reference only.

**Table 43 — Eight-Layer Geometry and Impedance Targets(Raw Card E2)**

Layer	Single-Ended		Differential	
	Width	Target $Z_0$	Width/Space	Target $Z_{DIFF}$
L1	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
L3	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
L6	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%
L8	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	95Ω ±15%
	0.19 mm	40Ω ±15%	0.19 mm/0.1 mm	66Ω ±15%

Note 1 All impedances other than the basic single-ended 60Ω target are provided for reference only.

6 DIMM Wiring Details (Cont'd)



Figure 44 — Eight-Layer Stackup (Example)

## 6 DIMM Wiring Details (Cont'd)

### 6.9 Test Point Identification

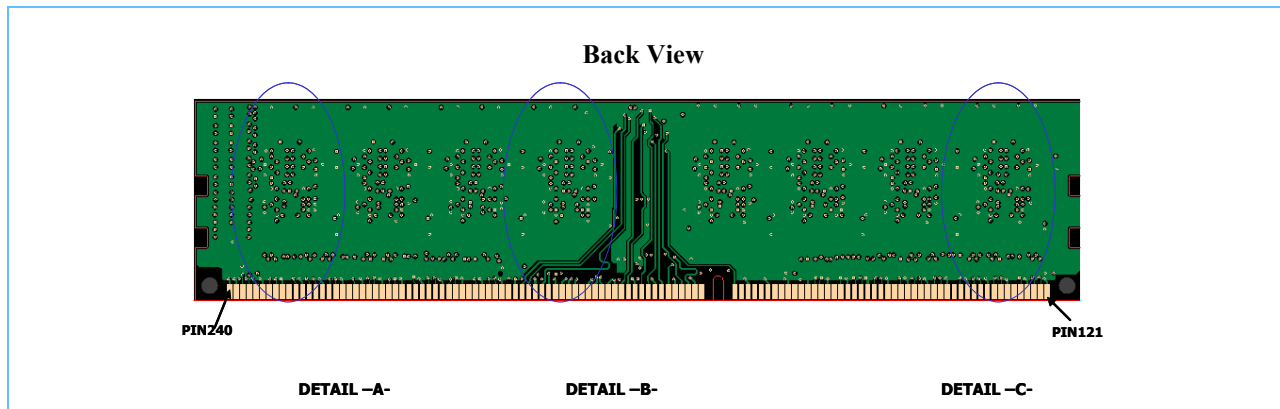


Figure 45 — Test Point Identification (Raw Card Version A): Back View

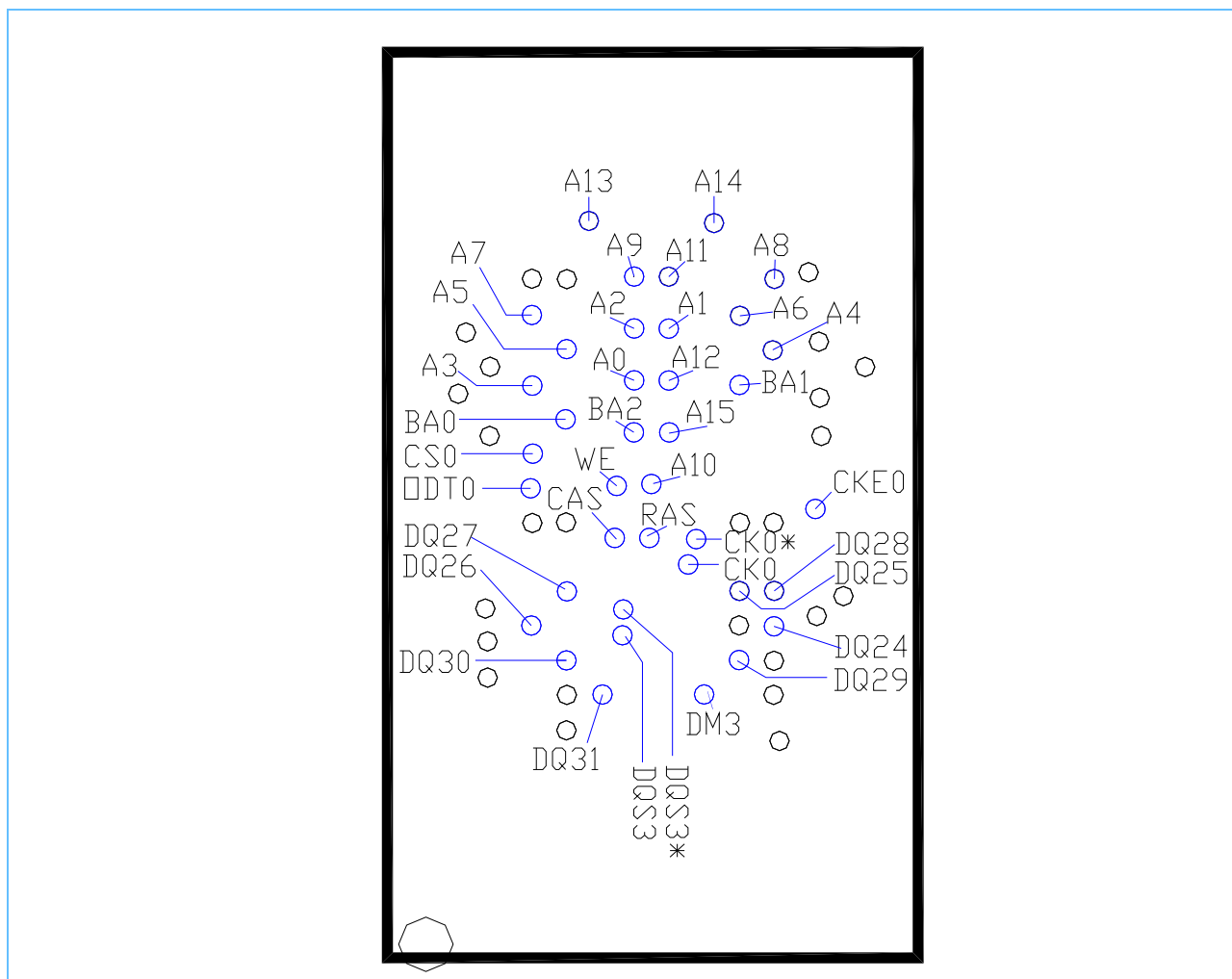
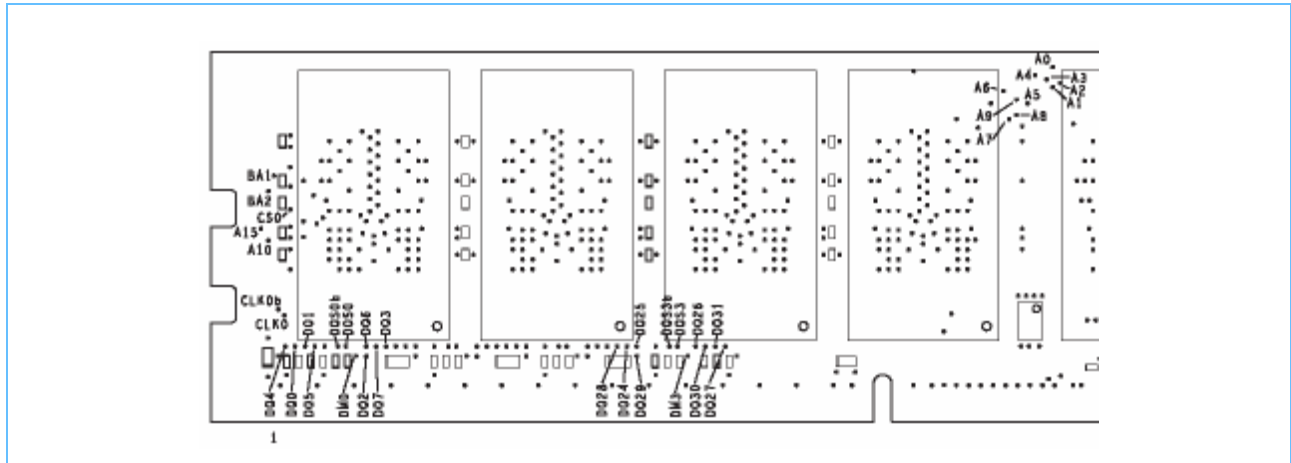


Figure 46 — Test Point Identification (Raw Card Version A): Bottom View

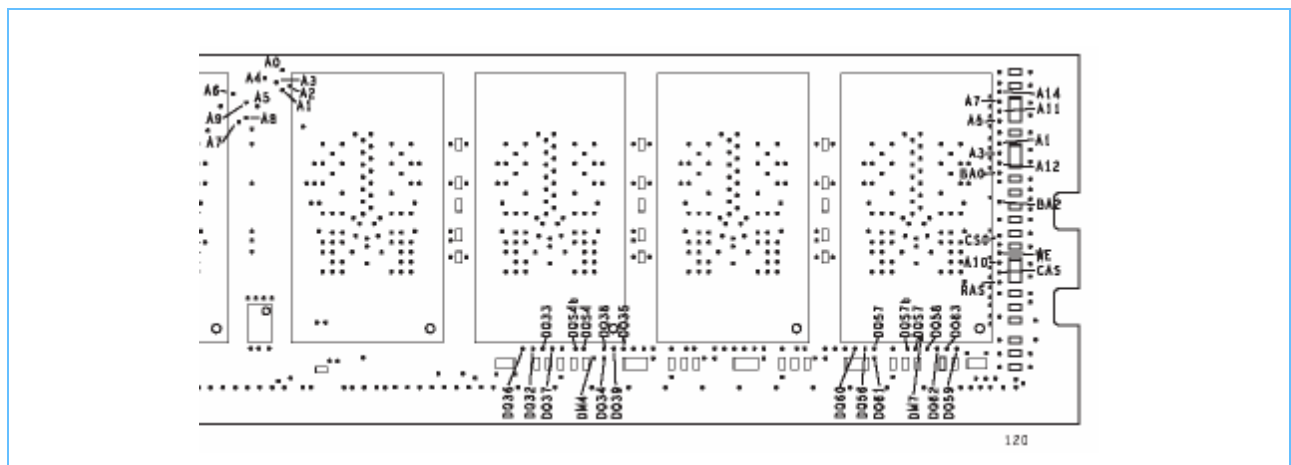
## 6 DIMM Wiring Details (Cont'd)

Raw Card B has DRAMs on either side of the module. All vias under the DRAM are not accessible. The points identified below are at via locations which are not under the DRAM and are not at optimal locations for determining timing or signal integrity at the DRAMs.



**Figure 47 — Test Point Identification (Raw Card Version B): Front View, Left Side**

Vias are located just before the first DRAM on the left side of the module. The location of the vias may provide a good indication of signaling at the first DRAM. The DQ and DQS signals can be measured at the via just after the stub resistor. This can be used for timing, but the signal at the DRAM will usually have better signal integrity. The address signals near the middle of the module are in the lead-in section. They will not be a good indicator of module performance.

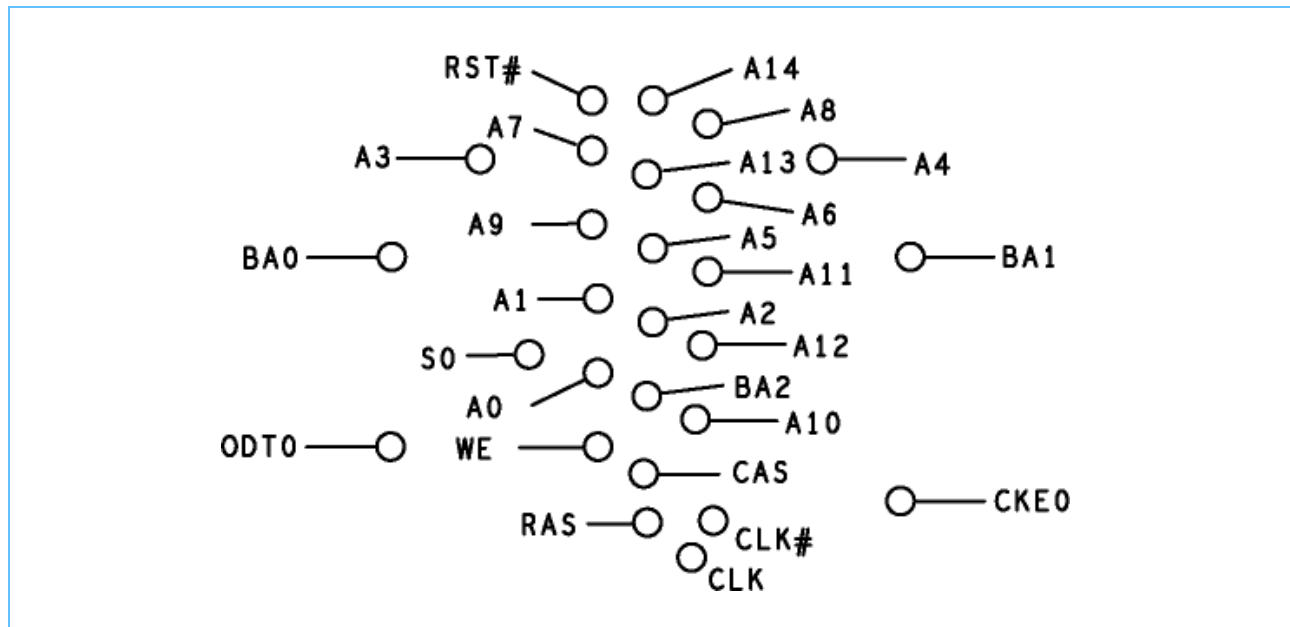


**Figure 48 — Test Point Identification (Raw Card Version B): Front View, Right Side**

The termination resistor on the right side of the module will provide some indication of signal integrity and timing at the last DRAM.

## 6 DIMM Wiring Details (Cont'd)

Raw Card C test points can be found in three locations: on the vias, on the termination resistors, and within the DQ group. First, because Raw Card C is a single-sided module, all test point vias can be accessed on the backside of the module, 2.5 mm from the edge of the DRAM pin (Figure 49 shows the via grid under each DRAM). This grid allows access to all command, address, control, and clock signals near the DRAM pins. After scraping through the soldermask, a ground plane can be connected to the ground side of the probe on the backside of the module.



**Figure 49 — Test Point Identification (Raw Card C): Backside View  
The Address and Command, Control, and Clock Structure Pins**

6 DIMM Wiring Details (Cont'd)

A map of the termination resistor signal assignments, shown in Figure 50, shows how test points can also be accessed on the component side of the module. The component side of the module consists of two planes: the  $V_{TT}$  rail plane—which is located to the right of the termination resistors—and the ground plane. Note: picking up a good ground point for the resistor in the right column may be difficult to do because the capacitors in this area are connected between  $V_{TT}$  and  $V_{DD}$  only.

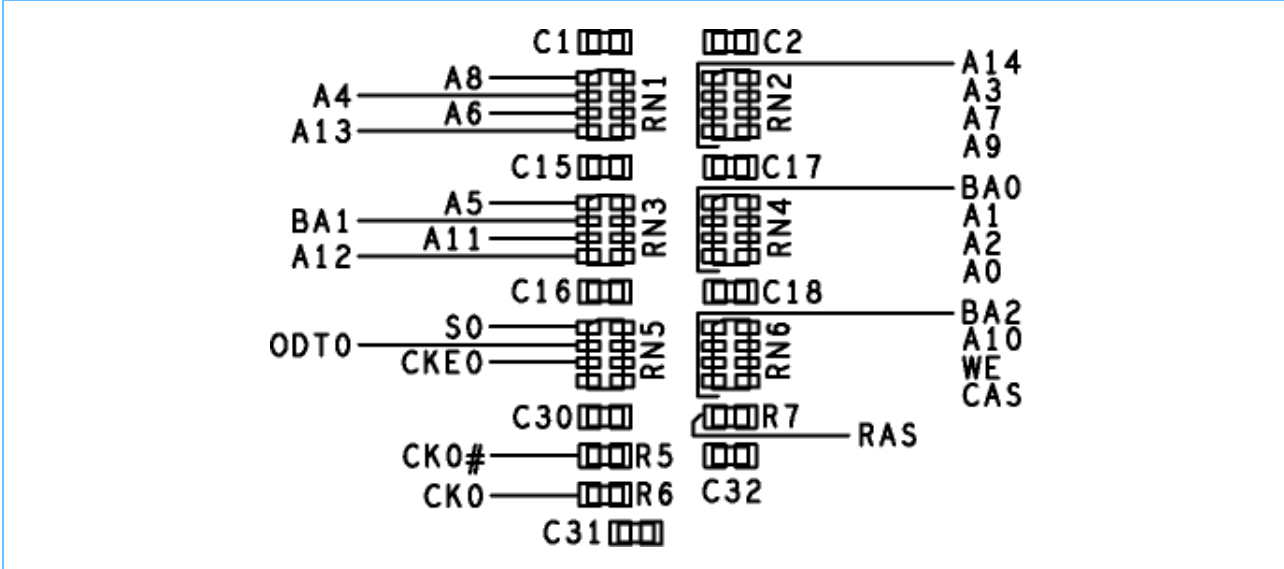


Figure 50 — Raw Card C Test Points (Raw Card C): The Termination Resistors

Finally, test points can be found on the DQ group. Figure 51 illustrates the location of the DQ test point vias located 0.6 mm from the edge of the DRAM pin (vias not shown are used for power and ground points). After scraping through the solder mask, a ground plane can be used to connect to the ground side of the probe on the backside of the module. Figure 51 references the signals for the first two byte groups. To correctly identify the signals for additional byte groups (DQ0–DQ16 or DQ32 or DQ48), add increments of 16 to each subsequent reference designator.

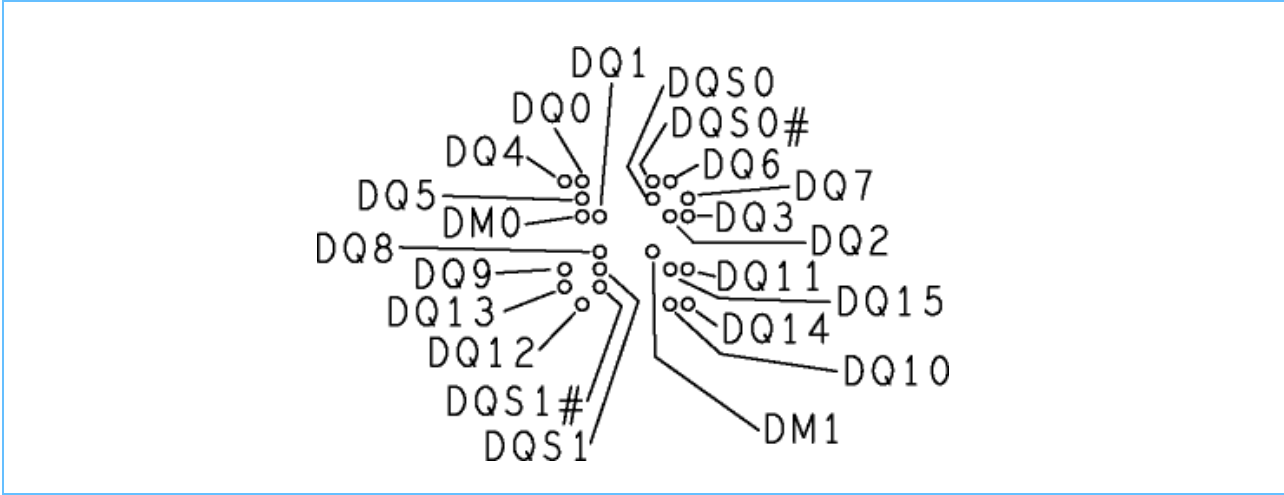
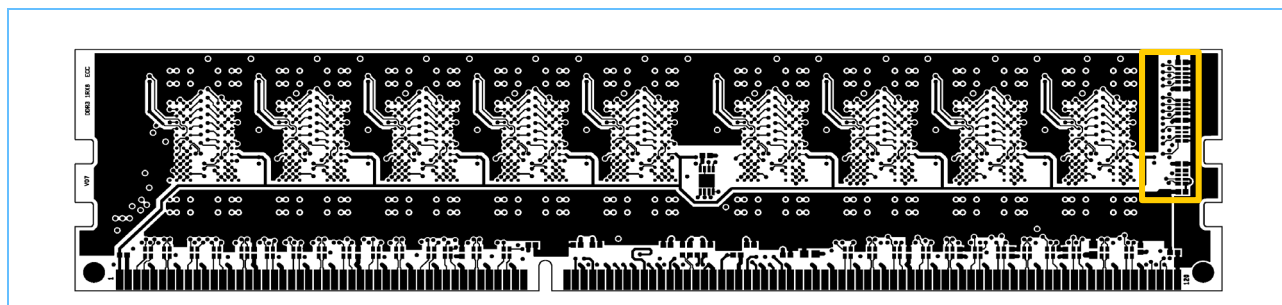


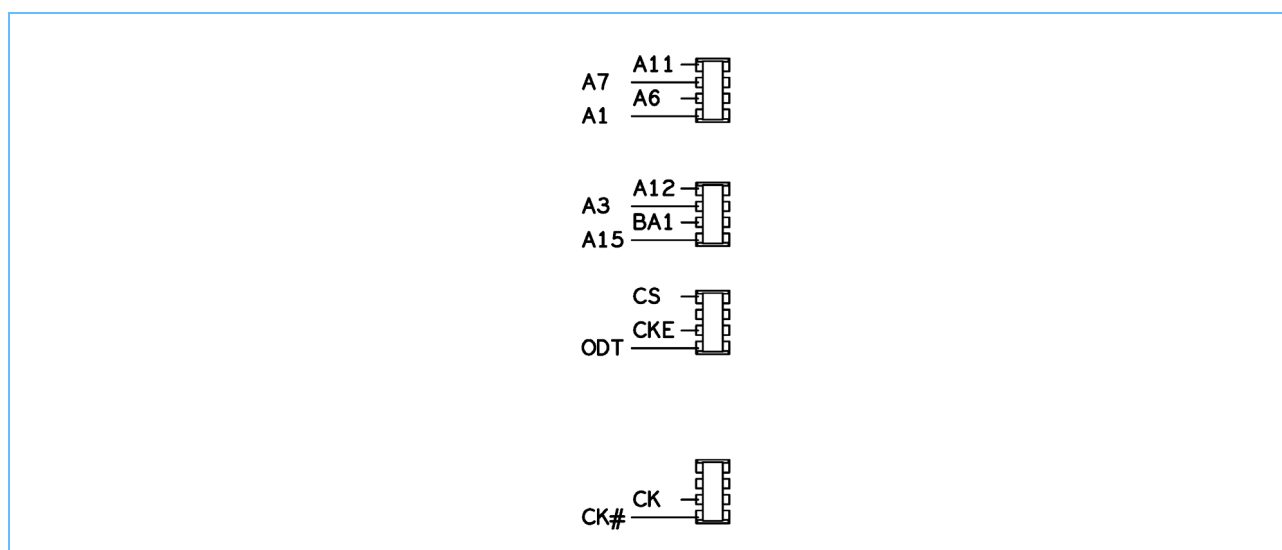
Figure 51 — Test Point Identification (Raw Card C): Backside View, The DQ Group

## 6 DIMM Wiring Details (Cont'd)

Raw Card D DRAMs exist only on the front side of the module. This allows access to the vias under the DRAMs from the back side. Some probe points are also available on the front side of the module (see Figures 52 and 53).

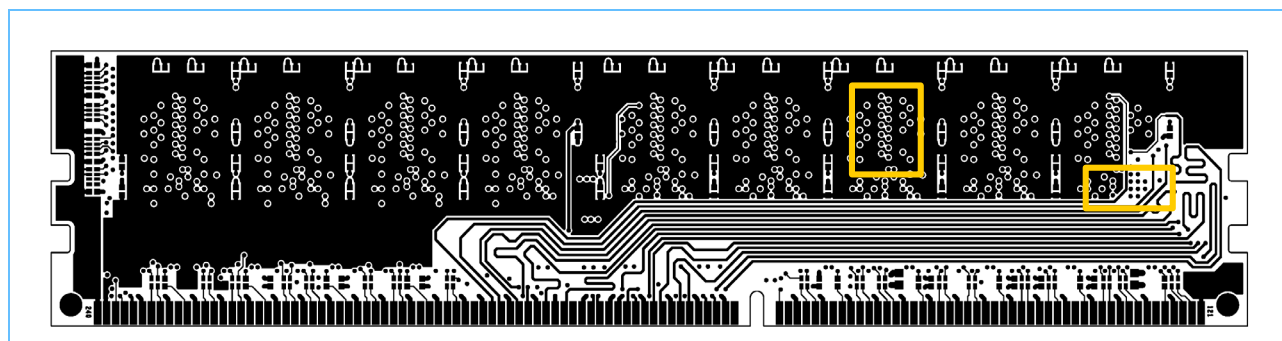


**Figure 52 — Test Point Identification (Raw Card Version D): Front Side, Full Board View**



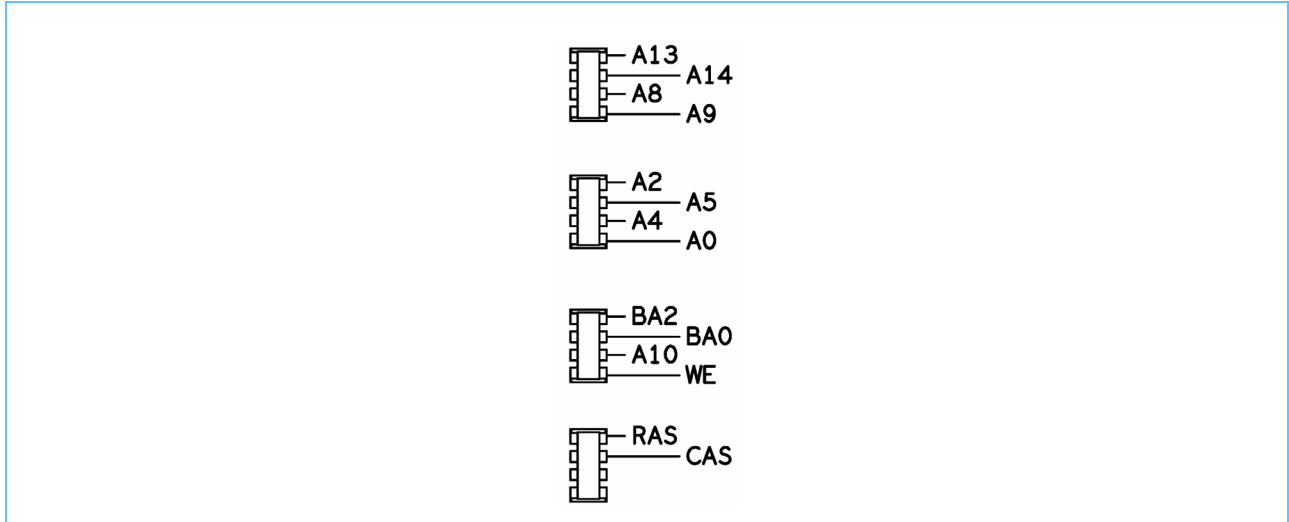
**Figure 53 — Test Point Identification (Raw Card Version D): Front Side, Detailed View**

Most of the test points of interest reside on the back side of the module. Figures 54–57 detail the locations of these test points.

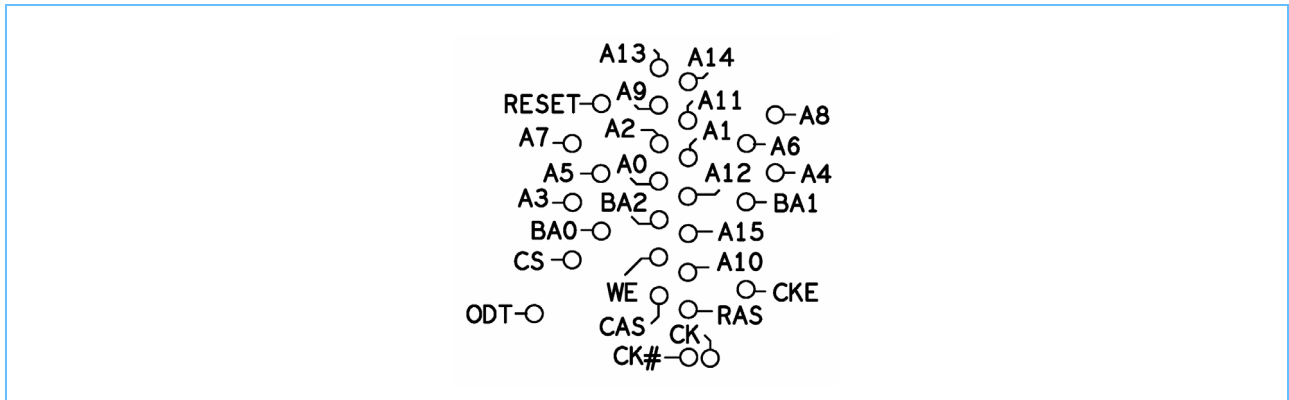


**Figure 54 — Test Point Identification (Raw Card Version D): Back Side, Full Board View**

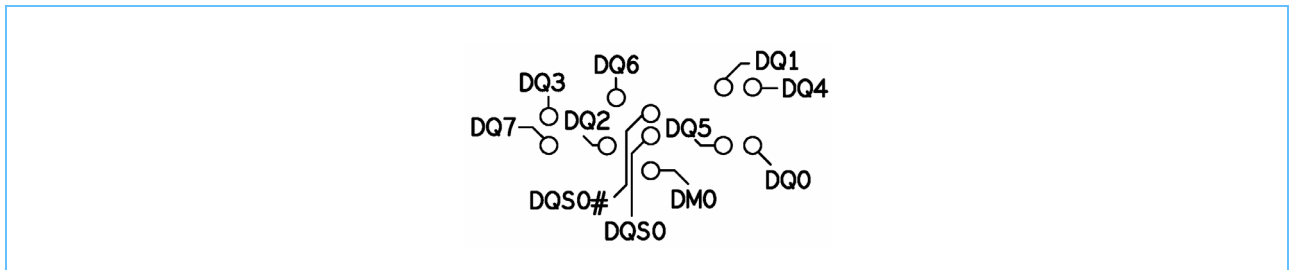
6 DIMM Wiring Details (Cont'd)



**Figure 55 — Test Point Identification (Raw Card Version D): Back Side View Test Point Area at the Terminations**



**Figure 56 — Test Point Identification (Raw Card Version D): Back Side View Test Point Area Under the DRAMs**



**Figure 57 — Test Point Identification (Raw Card Version D): Back Side View Termination Area at the First DRAM**

The detail for the via pattern behind the DRAM is valid for all DRAM locations.

## 6 DIMM Wiring Details (Cont'd)

Raw Card E contains DRAMs on either side of the module, which limits the availability of test points. The available test points accessible from the front side of the module are detailed in Figures 58–61.

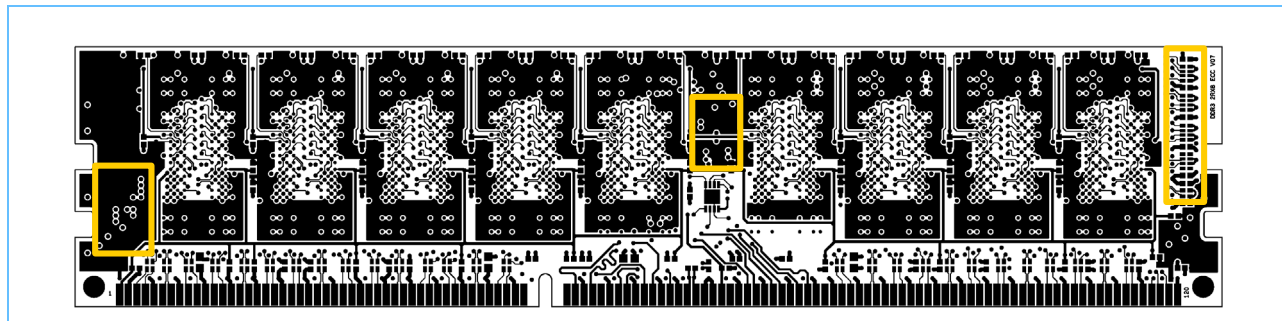


Figure 58 — Test Point Identification (Raw Card Version E): Front Side View, Full Board

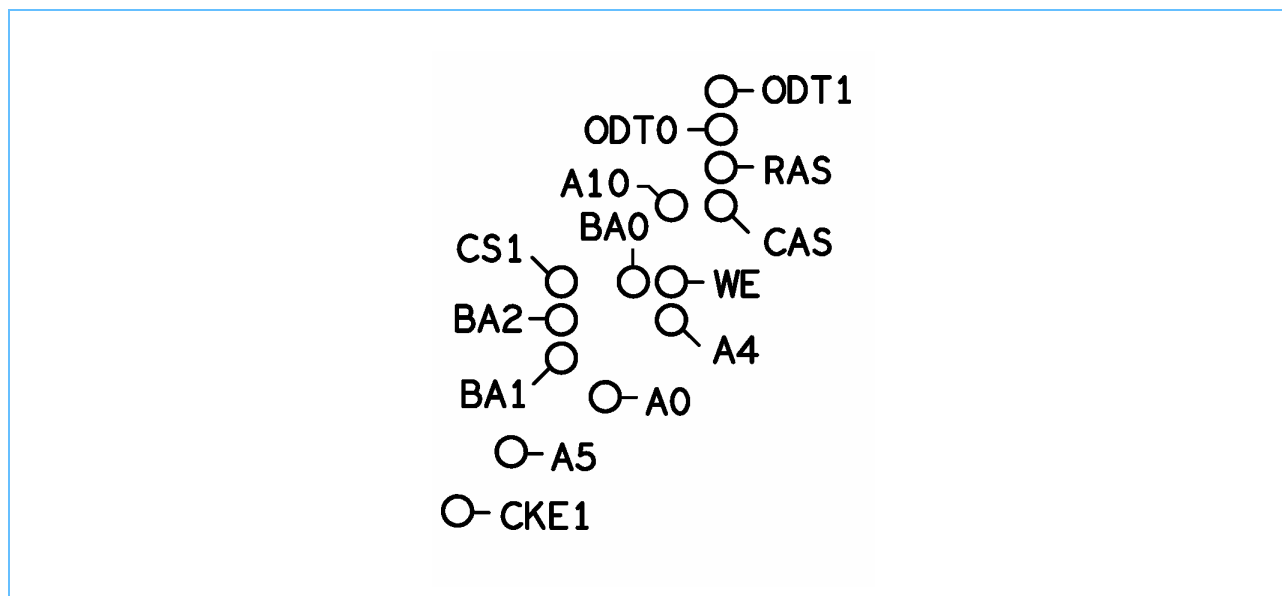


Figure 59 — Test Point Identification (Raw Card Version E): Front Side View  
Test Points Near the First DRAM

6 DIMM Wiring Details (Cont'd)

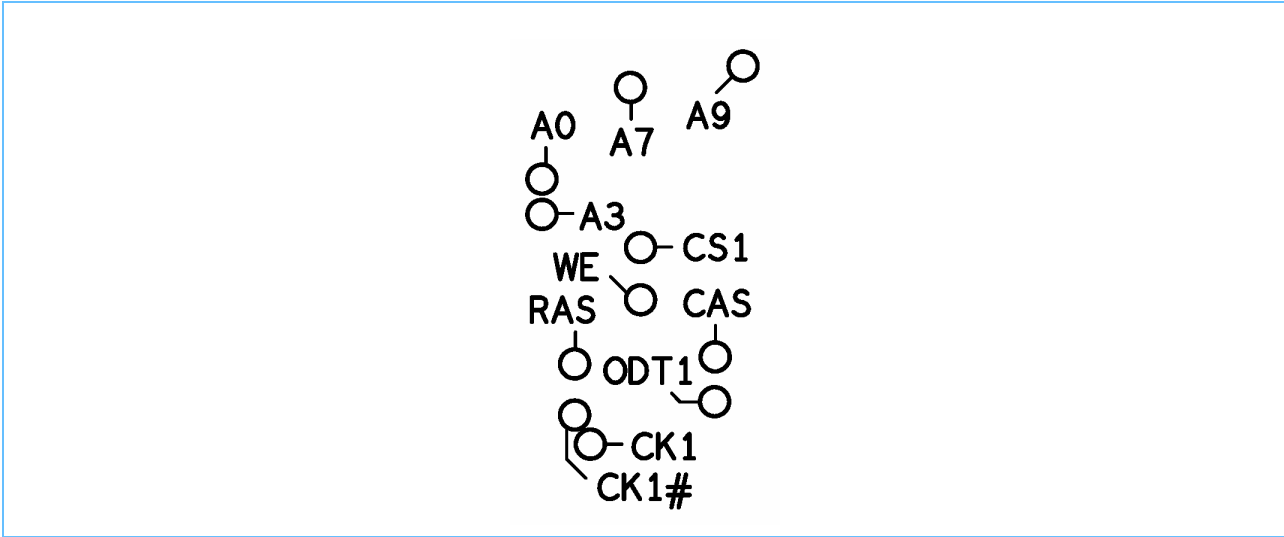


Figure 60 — Test Point Identification (Raw Card Version E): Front Side View  
Test Points Between the Fifth and Sixth DRAM Sites

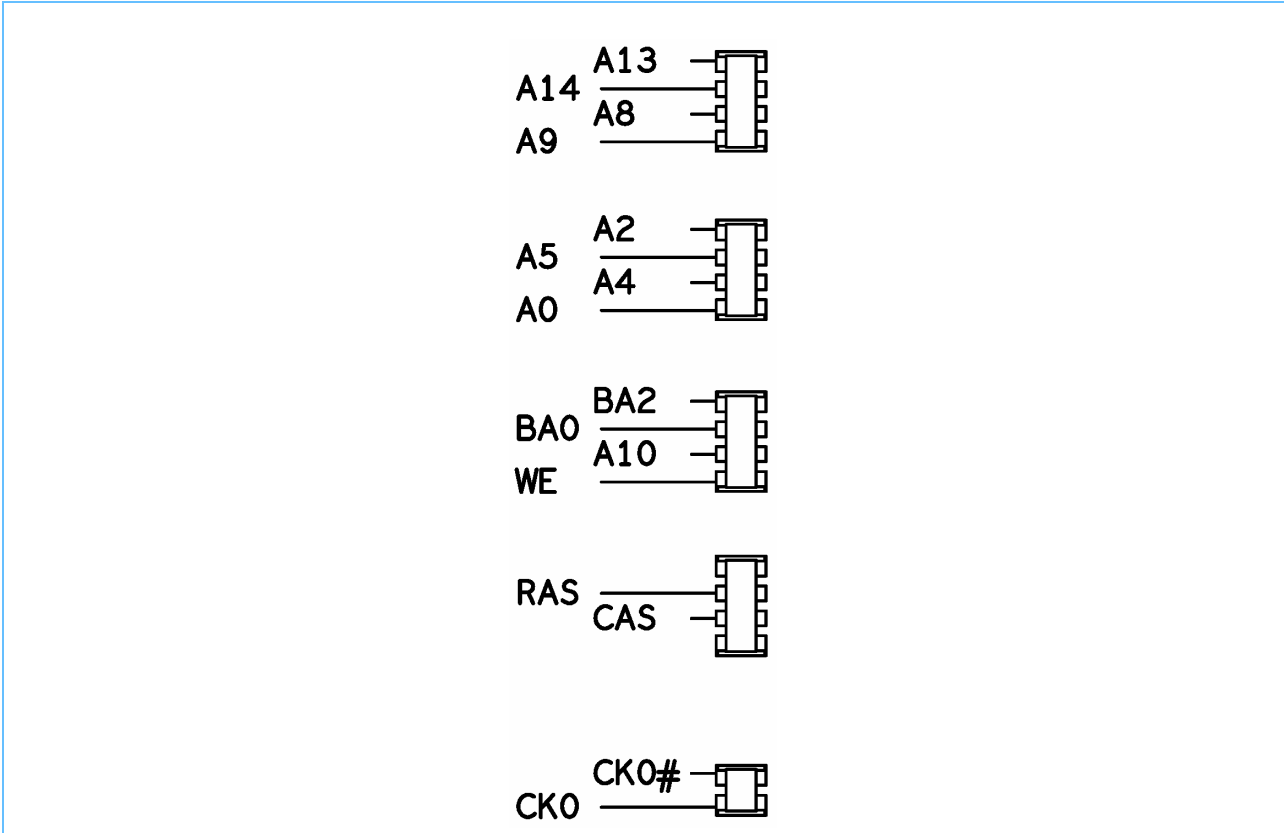


Figure 61 — Test Point Identification (Raw Card Version E): Front Side View  
Test Points at the Terminations

## 6 DIMM Wiring Details (Cont'd)

Raw Card E3 contains DRAMs on either side of the module, which limits the availability of test points. The available test points accessible from the front side of the module are detailed in Figures 62–65.

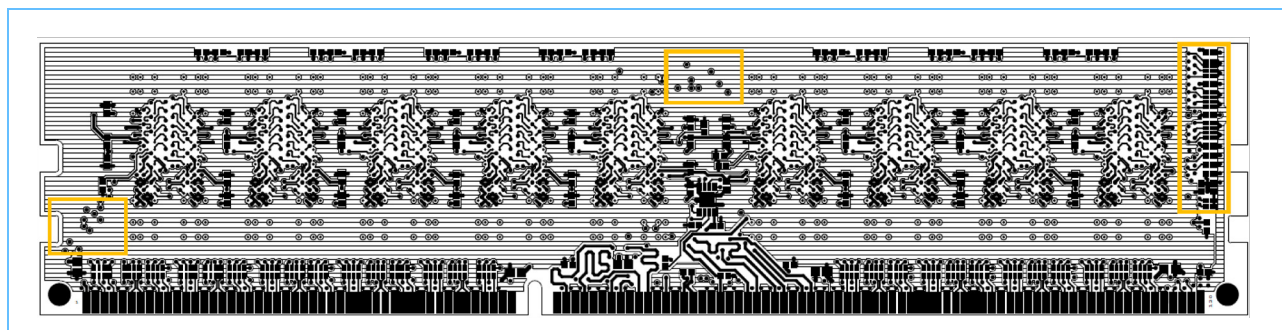


Figure 62 — Test Point Identification (Raw Card Version E3): Front Side View, Full Board

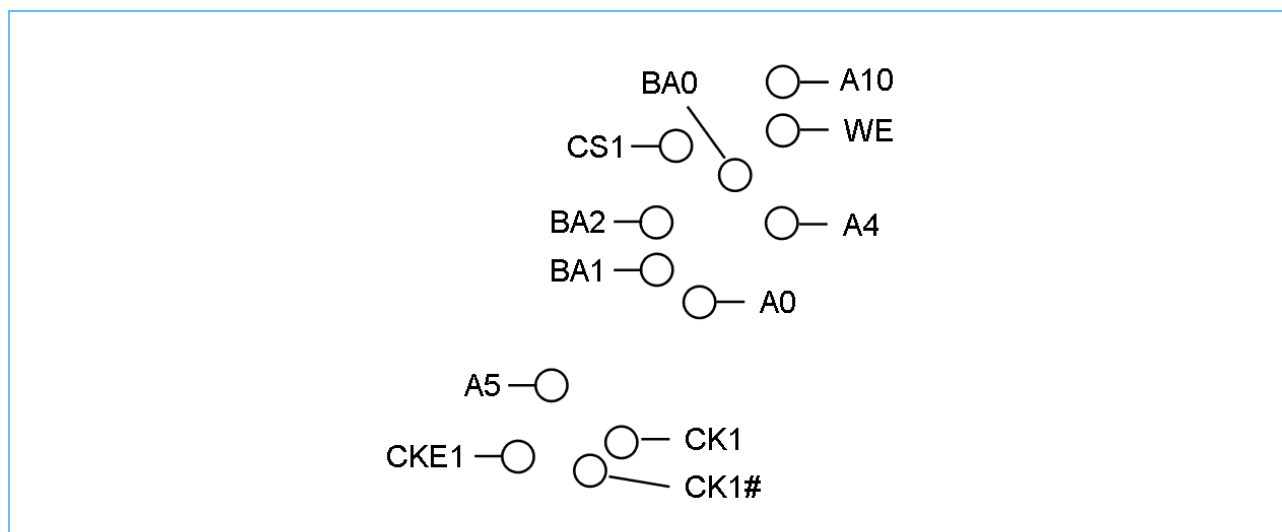


Figure 63 — Test Point Identification (Raw Card Version E3): Front Side View  
Test Points Near the First DRAM

6 DIMM Wiring Details (Cont'd)

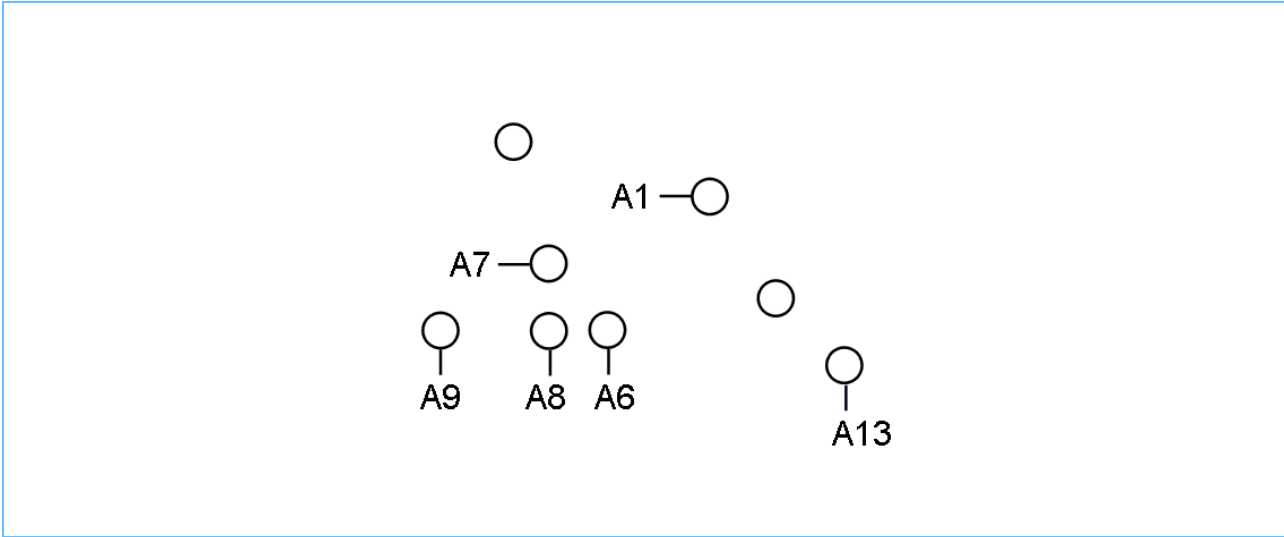


Figure 64 — Test Point Identification (Raw Card Version E3): Front Side View  
Test Points Between the Fifth and Sixth DRAM Sites

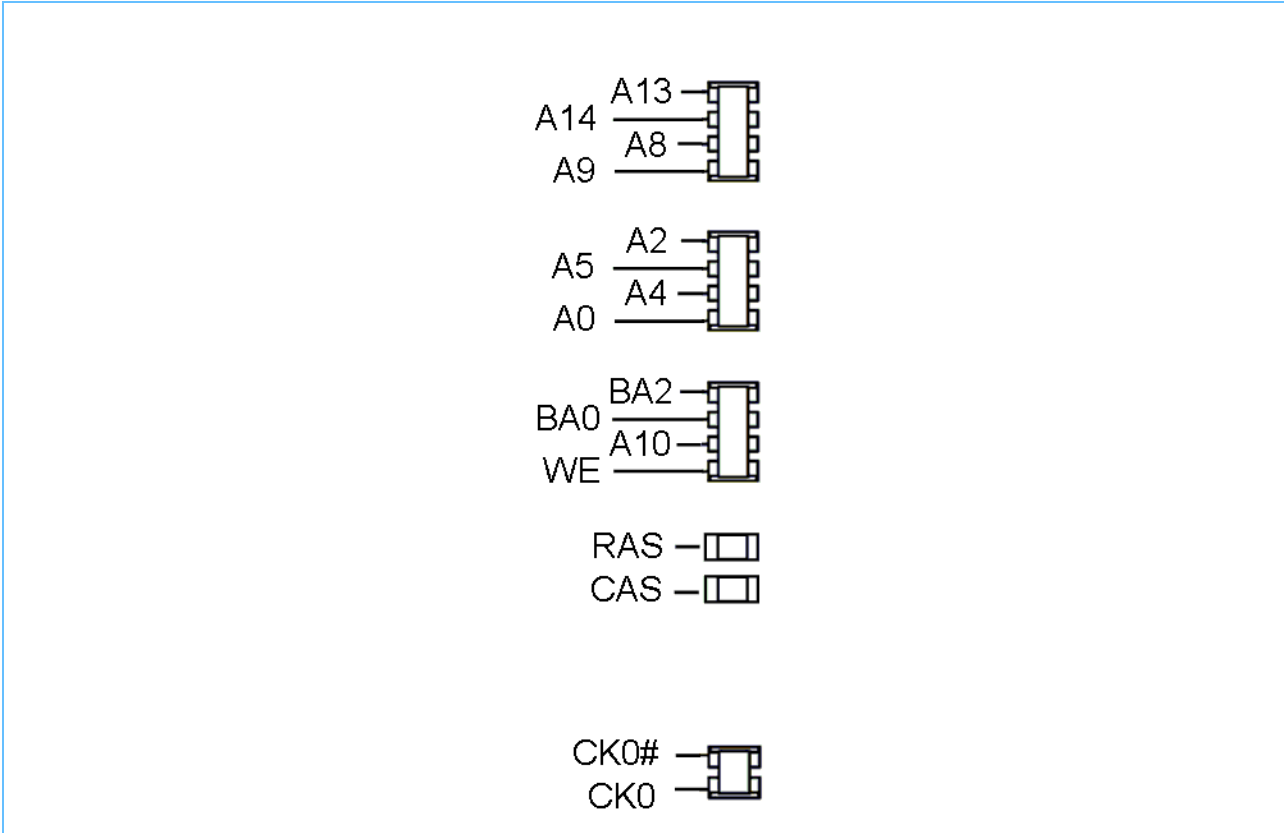
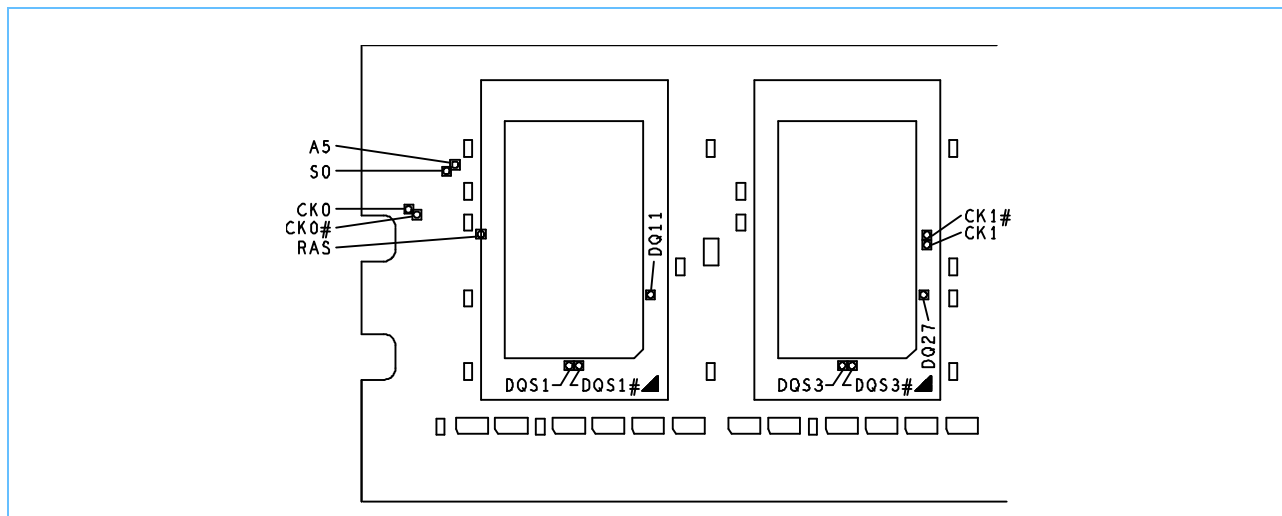


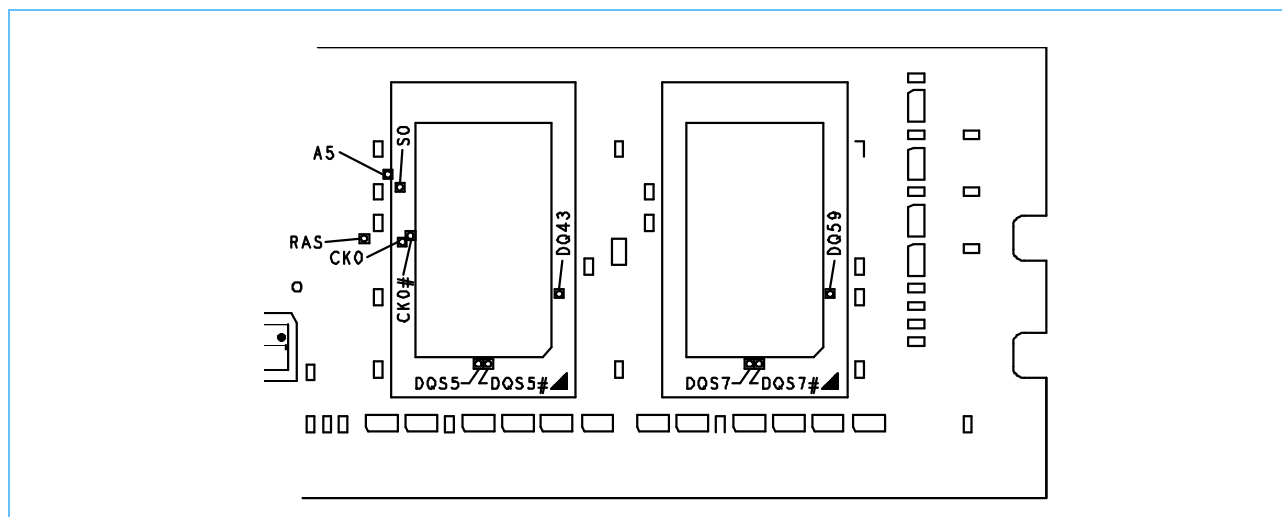
Figure 65 — Test Point Identification (Raw Card Version E3): Front Side View  
Test Points at the Terminations

## 6 DIMM Wiring Details (Cont'd)

Raw Card F is a two-sided module which prevents convenient access to test points. Other via locations can also be used (these will be identified) but they are further away from the DRAM pins. Additional vias have been added to provide additional test points. This compromises the timing, but availability of the test points is considered important enough that this trade-off has been made. Figure 66 shows the location of the test points on the left side of the module (not all test points will be available when a large DRAM is installed). Figure 67 shows the location of the test points for the right side of the module.



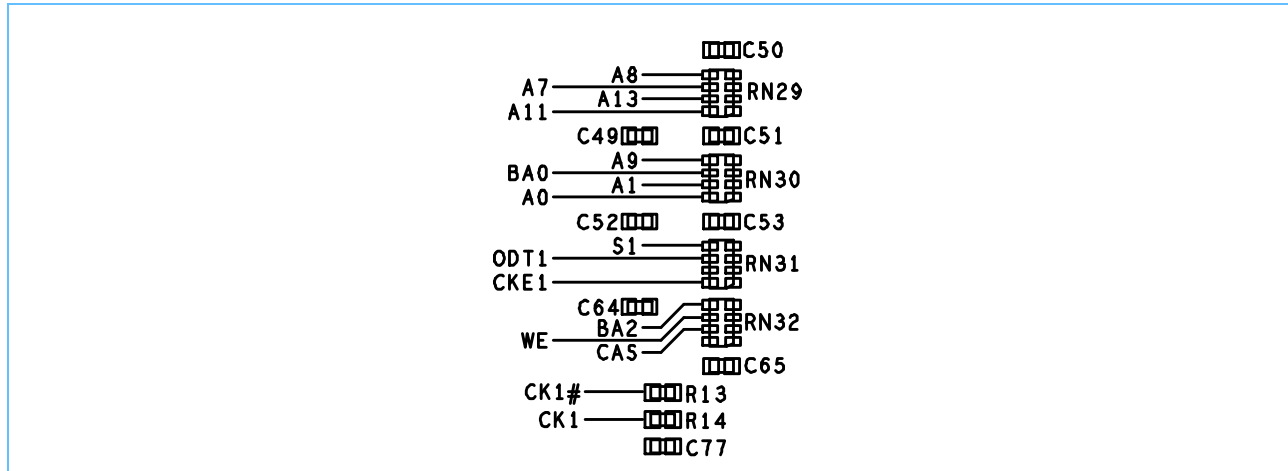
**Figure 66 — Test Point Identification (Raw Card Version F): Front, Left Side View**



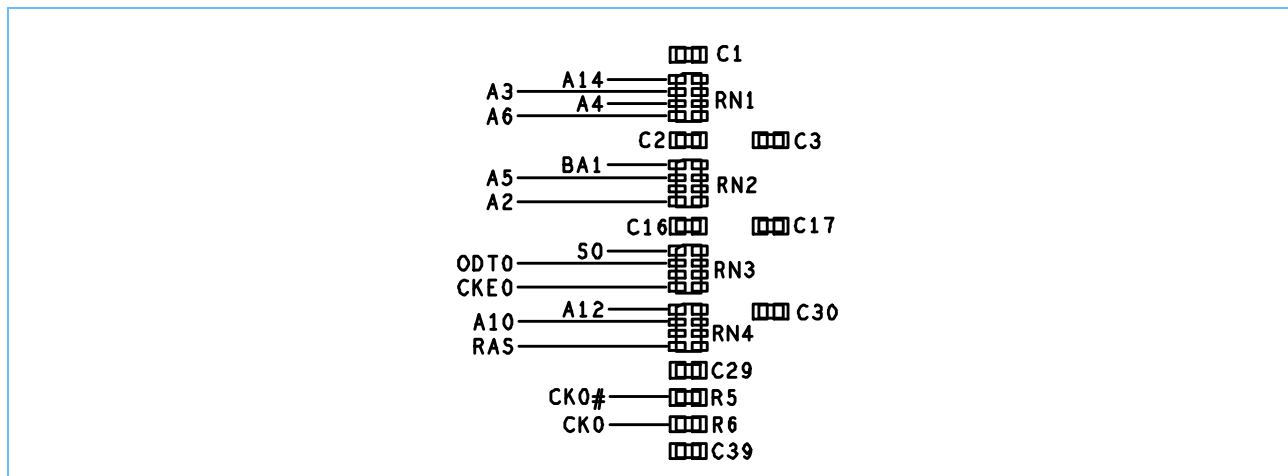
**Figure 67 — Test Point Identification (Raw Card Version F): Front, Right Side View**

## 6 DIMM Wiring Details (Cont'd)

Termination resistors also provide a good point to access the signals. Maps of these signal assignments are shown in Figures 68 and 69.



**Figure 68 — Test Point Identification (Raw Card Version F): Front Side View Signal Locations at the Termination Resistors**



**Figure 69 — Test Point Identification (Raw Card Version F): Back Side View Signal Locations at the Termination Resistors**

Raw Card F has a ground plane on the outside layers. This will provide reasonable access to ground for the ground side of any probe. Use caution: there is a  $V_{TT}$  plane on the other side of the resistor networks. The decoupling capacitors are between the  $V_{TT}$  and  $V_{DD}$  and can not be used for probe ground.

## 7 Serial Presence Detect

### 7.1 Serial Presence Detect Component Specification

The contents of the lower 128 bytes (Bytes 0–127) of the SPD EEPROM must be software write protected by the DIMM vendor, using one of the two methods standardized by JEDEC JC-45: either the permanent software write protect method, or the reversible software write protect method.

### 7.2 Serial Presence Detect Definition

The Serial Presence Detect function MUST be implemented on the DDR3 SDRAM Unbuffered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR3 Module Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices.

The following table is intended to be an **example** of the SPD data for a PC3-8500, double-sided 2GB (2 x 128 Meg x 64) non-ECC, 240-pin unbuffered DDR3 SDRAM DIMM. This example shows a module comprised of sixteen 128 Meg x 8 DRAM components.

**Table 44 — Serial Presence Detect, Example Raw Card Version B (Part 1 of 2)**

Byte Number	Byte Attribute Description	SPD Entry Value	Hexadecimal Byte Value
0	CRC range, EEPROM bytes, bytes used	Bytes 0–116/256/176	92
1	SPD revision	Rev 0.0	00
2	DRAM device type	DDR3 SDRAM	0B
3	Module type (form factor)	UDIMM	02
4	SDRAM Device density and banks	1Gb, 8 banks	02
5	SDRAM device row and column count	14 rows, 10 columns	11
6	Byte 6 reserved	None	00
7	Module ranks and device DQ count	2 Ranks, x8 DQs	09
8	ECC tag and module memory Bus width	Non-ECC, 64-bit Bus	03
9	Fine timebase dividend/divisor (in pico seconds)	5/2 = 2.5ps	52
10	Medium timebase dividend	1ns	01
11	Medium timebase divisor	8ns	08
12	Minimum SDRAM cycle time ( $t_{CKMIN}$ )	1.875ns	0F
13	Byte 13 reserved	None	00
14	CAS latencies supported (CL4 ≥ CL11)	CAS 8, 7, and 6	1C
15	CAS latencies supported (CL12 ≥ CL18)	None	00
16	Minimum CAS latency time ( $t_{AA_{MIN}}$ )	13.125ns	69
17	Minimum write recovery time ( $t_{WR_{MIN}}$ )	15ns	78
18	Minimum RAS <sub>n</sub> -to-CAS <sub>n</sub> delay ( $t_{RCD_{MIN}}$ )	13.125ns	69
19	Minimum row ACTIVE-to-ROW ACTIVE delay ( $t_{RRD_{MIN}}$ )	7.5ns	3C
20	Minimum row PRECHARGE delay ( $t_{RP_{MIN}}$ )	13.125ns	69
21	Upper nibble for $t_{RAS}$ and $t_{RC}$	1(2C) and 1(A4)	11
22	Minimum ACTIVE-to-PRECHARGE delay ( $t_{RAS_{MIN}}$ )	0x12C = 37.5ns	2C

7 Serial Presence Detect (Cont'd)

Table 44 — Serial Presence Detect, Example Raw Card Version B (Part 2 of 2)

Byte Number	Byte Attribute Description	SPD Entry Value	Hexadecimal Byte Value
23	Minimum ACTIVE-to-ACTIVE/REFRESH delay ( <sup>4</sup> RC <sub>MIN</sub> )	0x1A4 = 52.5ns	A4
24	Minimum refresh recovery delay ( <sup>4</sup> RFC <sub>MIN</sub> ) LSB	(combo bytes 24, 25)	70
25	Minimum refresh recovery delay ( <sup>4</sup> RFC <sub>MIN</sub> ) MSB	0x370=110ns <sup>4</sup> RFC <sub>MIN</sub>	03
26	Minimum internal WRITE-TO-READ command delay ( <sup>4</sup> WTR <sub>MIN</sub> )	7.5ns	3C
27	Minimum internal READ-to-PRECHARGE command delay ( <sup>4</sup> RTP <sub>MIN</sub> )	7.5ns	3C
28	Minimum four active window delay ( <sup>4</sup> FAW <sub>MIN</sub> ) LSB	(combo bytes 28, 29)	01
29	Minimum four active window delay ( <sup>4</sup> FAW <sub>MIN</sub> ) MSB	0x12C = 37.5ns	2C
30	SDRAM device output drivers supported	RZQ/7 supported	02
31	SDRAM device thermal and refresh options	ASR, extended temperature	05
32–59	Bytes 32–59 reserved	None	00000000000000000000
60	Module height (NOMINAL)	30 mm	0F
61	Module thickness (MAX)	DR, 4 mm MAX	11
62	Raw card ID reference	Raw Card B	01
63	DRAM address mapping edge connector	Standard	00
64–116	Bytes 64–116 reserved	None	00000000000000000000
117	Module manufacturer ID (LSB)	Manufacturer specific	80
118	Module manufacturer ID (MSB)	Manufacturer specific	2C
119	Module manufacturer location ID	Variable data	00
120	Module manufacturer year	Variable data	00
121	Module manufacturer week	Variable data	00
122–125	Module serial number	Variable data	00000000
126–127	CRC	Calculated value	027B
128–145	Module part number	ASCII values	16JTF25664AY-1G1A1
146–147	Module revision code	Variable data	41
148	DRAM Device manufacturer ID (LSB)	Manufacturer specific	80
149	DRAM device manufacturer (MSB)	Manufacturer specific	2C
150–175	Manufacturer-reserved bytes 150–175	Reserved	00000000000000000000
176–255	Customer-reserved bytes 176–255	Reserved	FFFFFFFFFFFFFFFFFFFFFF

## 8 Product Label

### DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

Voltage options in field 'v' describe the nominal voltage VDD of the SDRAMs and support components (excluding the SPD). Values for these voltages are 'operable' which means the device characteristics such as timing are supported at this voltage, or 'endurant' which means that the device may be powered to that voltage level without damage, however should not be used as operation is not guaranteed at the higher voltage.

ggggg eRxff PC3v-wwwwm-aa-bb-ccd

#### Where:

- ggggg = Module total capacity, in bytes  
256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed
  - 1R = 1 rank of DDR3 SDRAM installed
  - 2R = 2 ranks
  - 4R = 4 ranks
- xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly
  - x4 = x4 organization (4 DQ lines per SDRAM)
  - x8 = x8 organization
  - x16 = x16 organization
- v = SDRAM and support component supply voltage (VDD)
  - Blank = 1.5 V operable
  - L = 1.35 V operable, 1.5 V operable
  - U = 1.TBD V operable, 1.TBD V endurant
- wwww = Module bandwidth in MB/s
  - 6400 = 6.40 GB/s (DDR3-800 SDRAMs, 8 byte primary data bus)
  - 8500 = 8.53 GB/s (DDR3-1066 SDRAMs, 8 byte primary data bus)
  - 10600 = 10.66 GB/s (DDR3-1333 SDRAMs, 8 byte primary data bus)
  - 12800 = 12.80 GB/s (DDR3-1600 SDRAMs, 8 byte primary data bus)
  - 14900 = 14.93 GB/s (DDR3-1866 SDRAMs, 8 byte primary data bus)
  - 17000 = 17.06 GB/s (DDR3-2133 SDRAMs, 8 byte primary data bus)
- m = Module Type
  - E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
  - F = Fully Buffered DIMM ("FBDIMM")
  - L = Load Reduction DIMM ("LRDIMM")
  - M = Micro-DIMM
  - N = Mini-RDIMM
  - R = Registered DIMM("RDIMM")
  - S = Small Outline DIMM ("SODIMM")
  - U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
  - W = Mini-UDIMM, with ECC (x72 bit module data bus)
- aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency
- bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
- cc = Reference design file used for this design (if applicable)
  - A = Reference design for Raw Card "A" is used for this assembly
  - B = Reference design for Raw Card "B" is used for this assembly

## 8 Product Label (Cont'd)

AC = Reference design for raw card 'AC' is used for this assembly  
ZZ = None of the reference designs were used for this assembly  
d = Revision number of the reference design used  
0 = Initial release  
1 = First revision  
2 = Second revision  
P = Pre-release or Engineering sample  
Z = To be used when field cc= ZZ

### Examples:

2GB 2Rx4 PC3-10600R-7-10-D2

is a 2 GB DDR3 RDIMM using 2 ranks of x4 SDRAMs operational to DDR3-1333 performance with CAS Latency = 7 using JEDEC DDR3 SPD revision 1.0, raw card reference design file D revision 2 used for the assembly

1GB 1Rx4 PC3L-10600R-8-10-C1

is a 1 GB DDR3 RDIMM using 1 rank of x4 low voltage SDRAMs, operable at 1.35 V and 1.5 V operable, operational to DDR3-1333 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, raw card reference design file C revision 1 used for the assembly

1GB 2Rx8 PC3-12800E-10-10-BP

is a 2 GB DDR3 UDIMM with x72 data bus (ECC) using 2 ranks of x8 SDRAMs operational to DDR3-1600 performance with CAS Latency = 10 using JEDEC DDR3 SPD revision 1.0, raw card reference design file B pre-release revision used for the assembly

4GB 2Rx8 PC3-8500N-8-10-ZZZ

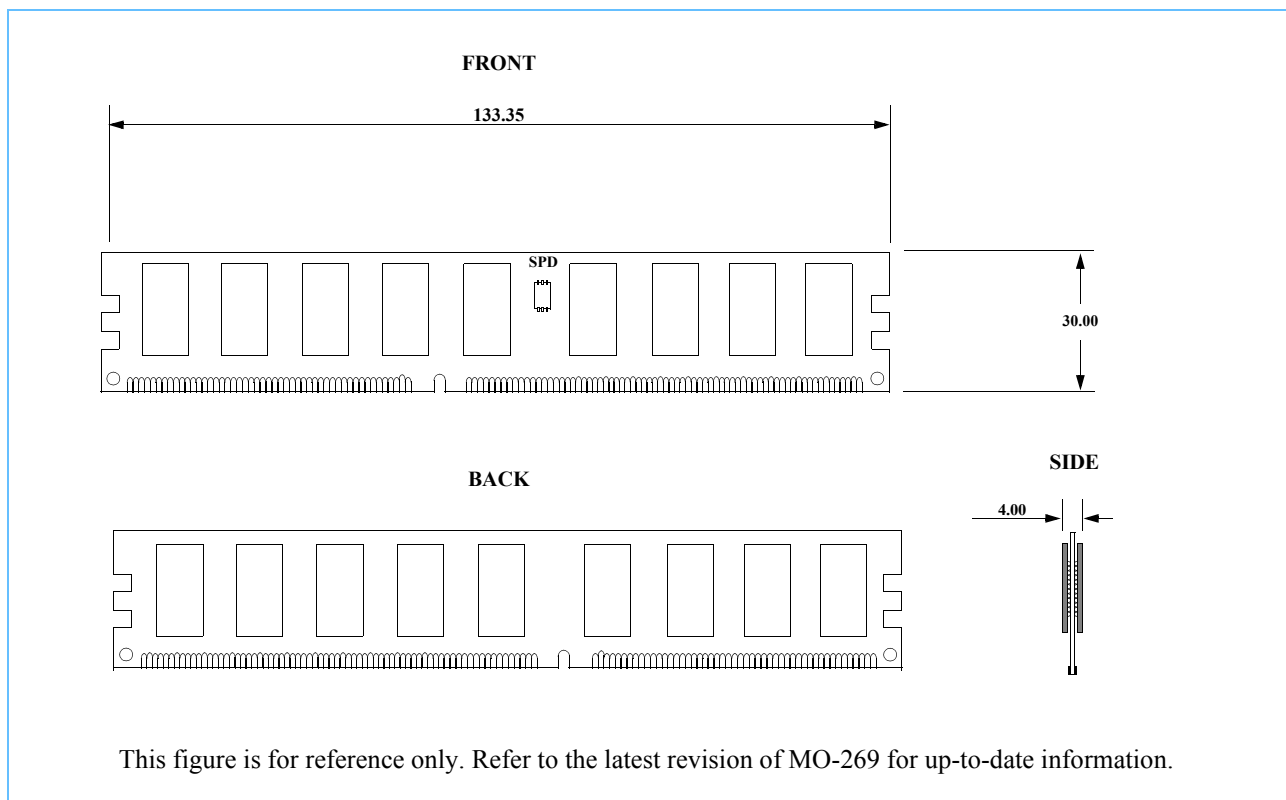
is a 4 GB DDR3 Mini-RDIMM using 2 ranks of x8 SDRAMs operational to DDR3-1066 performance with CAS Latency = 8 using JEDEC DDR3 SPD revision 1.0, no JEDEC standard raw card reference design file used for the assembly

Note: The Gerber reference designs provide as foundations for a module PCB. Manufacturers may make modifications to the designs as long as the signal integrity and timing is maintained.

## 9 DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to <http://www.jedec.org>
2. Click on 'Standards Publications'
3. Click on "Search Standards and Publications"
4. Use the search box "By Document Number"
5. Enter MO-269 to download



**Figure 70 — Mechanical Drawing with Keying Positions**

## 10 DDR3 240-Pin Connector S-Parameters

This specification is published as JESD21C, Section 4.8. Please refer to this specification for details and testing methodology.

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