

4.20.19 - 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM
Unbuffered DIMM Design Specification

PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM
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1 Product Description

This specification defines the electrical and mechanical requirements for 240-pin, 1.5 Volt (V_{DD})/1.5 Volt (V_{DDQ}), Unbuffered, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR3 SDRAM DIMMs). These DDR3 DIMMs are intended for use as main memory when installed in PCs.

Reference design examples are included which provide an initial basis for Unbuffered DDR3 DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC3-6400, PC3-8500, PC3-10600, and PC3-12800 support. All Unbuffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification follows the JEDEC standard DDR3 component specification (refer to JEDEC standard JESD79-3, at www.jedec.org).

Table 1 — Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (NOM)	133.35 mm x 30.00 mm x 4 mm	Refer to MO 269
Pin Count	240	
DDR3 SDRAMs Supported	512Mb, 1Gb, 2Gb, 4Gb, 8Gb	78/106-ball FBGA package for x8 and 96/112-ball FBGA for x16 devices.
Capacity	256MB–16GB	
Serial PD	Consistent with JEDEC JC 45 SPD publication	
Voltage Options	1.5 Volt V_{DD}/V_{DDQ}	All DDR3 modules use a common $V_{DD}-V_{DDQ}$ power plane. They are tied together on the DIMM, but by standard definition are supported on the pinout to accommodate future enhancements.
	3.0 Volt to 3.6 Volt V_{DDSPD}	This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 3.0V to 3.6V.
Interface	1.5V signaling	
1. V_{DDSPD} is not tied to V_{DD} or V_{DDQ} on the DDR3 DIMM.		

2 Environmental Requirements

240-pin Unbuffered DDR3 SDRAM DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Table 2 — Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T _{OPR}	Operating Temperature (ambient)	0 to +55	°C	3
H _{OPR}	Operating Humidity (relative)	10 to 90	%	
T _{STG}	Storage Temperature	-50 to +100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (T_{CASE}) shall not exceed the value specified in the DDR3 DRAM component specification.

3 Architecture

Table 3 — Pin Definition

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I ² C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I ² C serial bus data line for EEPROM
$\overline{\text{RAS}}$	SDRAM row address strobe	SA0–SA2	I ² C slave address select for EEPROM
$\overline{\text{CAS}}$	SDRAM column address strobe	V _{DD*}	SDRAM core power supply
$\overline{\text{WE}}$	SDRAM write enable	V _{DDQ*}	SDRAM I/O Driver power supply
$\overline{\text{S0}}\text{--}\overline{\text{S1}}$	DIMM Rank Select Lines	V _{REFDQ}	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	V _{REFCA}	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V _{SS}	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V _{DDSPD}	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
$\overline{\text{DQS0}}\text{--}\overline{\text{DQS8}}$	SDRAM data strobes (negative line of differential pair)	$\overline{\text{RESET}}$	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	$\overline{\text{EVENT}}$	Reserved for optional temperature-sensing hardware
CK0–CK1	SDRAM clocks (positive line of differential pair)	V _{TT}	SDRAM I/O termination supply
$\overline{\text{CK0}}\text{--}\overline{\text{CK1}}$	SDRAM clocks (negative line of differential pair)	RSVD	Reserved for future use

*The V_{DD} and V_{DDQ} pins are tied common to a single power-plane on these designs.

Table 4 — Input/Output Functional Description

Symbol	Type	Polarity	Function
A0–A15	1.5V	—	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
BA0–BA2	1.5V	—	Selects which SDRAM bank of eight is activated.
CK0–CK1 CK0–CK1	1.5V	Differential crossing	CK and CK are differential clock inputs. All the DDR3 SDRAM addr/cnt inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossing of CK and CK (Both directions of crossing).
CKE0–CKE1	1.5V	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
DM0–DM8	1.5V	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
DQ0–DQ63, CB0–CB7	1.5V	—	Data and Check Bit Input/Output pins.
DQS0–DQS8 DQS0–DQS8	1.5V	Differential crossing	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are associated with the LDQS and LDQS pins and Pins DQ8–DQ15 are associated with UDQS and UDQS pins.
ODT0–ODT1	1.5V	Active High	When high, termination resistance is enabled for all DQ, DQS, DQS and DM pins, assuming this function is enabled on the DRAM.
RAS, CAS, WE	1.5V	Active Low	RAS, CAS, and WE (along with S) define the command being entered.
RESET	1.5V		The RESET pin is connected to the RESET pin on each DRAM. When low, all DRAMs are set to a known state.
S0–S1	1.5V	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
VDD, VSS	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
VDDQ	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.
VREFDQ	Supply		Reference voltage for I/O inputs.
VREFCA	Supply		Reference voltage for command/address inputs.
SA0–SA2		—	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to VDDSPD to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
EVENT	Output (Open Drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT pin on the TS/SPD part.

Table 5 — 240-Pin DDR3 SDRAM Pin Assignment (Part 1 of 2)

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V _{REFDQ}	121	V _{SS}	31	DQ25	151	V _{SS}	61	A2	181	A1	91	DQ41	211	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3, DQS12, TDQS12	62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5, DQS14, TDQS14
3	DQ0	123	DQ5	33	$\overline{\text{DQS3}}$	153	NC, $\overline{\text{DQS12}}$, TDQS12	63	NC, CK1	183	V _{DD}	93	$\overline{\text{DQS5}}$	213	NC, $\overline{\text{DQS14}}$, TDQS14
4	DQ1	124	V _{SS}	34	DQS3	154	V _{SS}	64	NC, $\overline{\text{CK1}}$	184	CK0	94	DQS5	214	V _{SS}
5	V _{SS}	125	DM0, DQS9, TDQS9	35	V _{SS}	155	DQ30	65	V _{DD}	185	$\overline{\text{CK0}}$	95	V _{SS}	215	DQ46
6	$\overline{\text{DQS0}}$	126	NC, $\overline{\text{DQS9}}$, TDQS9	36	DQ26	156	DQ31	66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
7	DQS0	127	V _{SS}	37	DQ27	157	V _{SS}	67	V _{REFCA}	187	$\overline{\text{EVENT}}$, NC	97	DQ43	217	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	CB4, NC	68	PAR_IN, NC	188	A0	98	V _{SS}	218	DQ52
9	DQ2	129	DQ7	39	CB0, NC	159	CB5, NC	69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
10	DQ3	130	V _{SS}	40	CB1, NC	160	V _{SS}	70	A10/AP	190	BA1	100	DQ49	220	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	DM8, DQS17, TDQS17, NC	71	BA0	191	V _{DD}	101	V _{SS}	221	DM6, DQS15, TDQS15
12	DQ8	132	DQ13	42	$\overline{\text{DQS8}}$	162	NC, $\overline{\text{DQS17}}$, TDQS17	72	V _{DD}	192	$\overline{\text{RAS}}$	102	$\overline{\text{DQS6}}$	222	NC, $\overline{\text{DQS15}}$, TDQS15
13	DQ9	133	V _{SS}	43	DQS8	163	V _{SS}	73	$\overline{\text{WE}}$	193	$\overline{\text{S0}}$	103	DQS6	223	V _{SS}
14	V _{SS}	134	DM1, DQS10, TDQS10	44	V _{SS}	164	CB6, NC	74	$\overline{\text{CAS}}$	194	V _{DD}	104	V _{SS}	224	DQ54
15	$\overline{\text{DQS1}}$	135	NC, $\overline{\text{DQS10}}$, TDQS10	45	CB2, NC	165	CB7, NC	75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	V _{SS}	46	CB3, NC	166	V _{SS}	76	$\overline{\text{S1}}$, NC	196	A13	106	DQ51	226	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC (TEST)	77	ODT1, NC	197	V _{DD}	107	V _{SS}	227	DQ60
18	DQ10	138	DQ15	48	V _{TT} , NC	168	$\overline{\text{RESET}}$	78	V _{DD}	198	$\overline{\text{S3}}$, NC	108	DQ56	228	DQ61
19	DQ11	139	V _{SS}	KEY				79	$\overline{\text{S2}}$, NC	199	V _{SS}	109	DQ57	229	V _{SS}
20	V _{SS}	140	DQ20	49	V _{TT} , NC	169	CKE1, NC	80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7, DQS15, TDQS16
21	DQ16	141	DQ21	50	CKE0	170	V _{DD}	81	DQ32	201	DQ37	111	$\overline{\text{DQS7}}$	231	NC, $\overline{\text{DQS16}}$, TDQS16
22	DQ17	142	V _{SS}	51	V _{DD}	171	A15, NC	82	DQ33	202	V _{SS}	112	DQS7	232	V _{SS}
23	V _{SS}	143	DM2, DQS11, TDQS11	52	BA2	172	A14	83	V _{SS}	203	DM4, DQS13, TDQS13	113	V _{SS}	233	DQ62
24	$\overline{\text{DQS2}}$	144	NC, $\overline{\text{DQS11}}$, TDQS11	53	$\overline{\text{ERR_OUT}}$, NC	173	V _{DD}	84	$\overline{\text{DQS4}}$	204	NC, $\overline{\text{DQS13}}$, TDQS13	114	DQ58	234	DQ63
25	DQS2	145	V _{SS}	54	V _{DD}	174	A12/ $\overline{\text{BC}}$	85	DQS4	205	V _{SS}	115	DQ59	235	V _{SS}

Table 5 — 240-Pin DDR3 SDRAM Pin Assignment (Part 2 of 2)

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
26	V _{SS}	146	DQ22	55	A11	175	A9	86	V _{SS}	206	DQ38	116	V _{SS}	236	V _{DDSPD}
27	DQ18	147	DQ23	56	A7	176	V _{DD}	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V _{SS}	57	V _{DD}	177	A8	88	DQ35	208	V _{SS}	118	SCL	238	SDA
29	V _{SS}	149	DQ28	58	A5	178	A6	89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
30	DQ24	150	DQ29	59	A4	179	V _{DD}	90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}
				60	V _{DD}	180	A3								

Table 6 — Pinout Comparison Based on Module Type

Pin	RDIMM		UDIMM	
	Signal	Notes	Signal	Notes
48, 49	V _{TT}	Additional connection for termination voltage for address/command/control/clock nets	NC	Not used on DIMMs
120, 240	V _{TT}	Termination voltage for address/command/control/clock nets	V _{TT}	Termination voltage for address/command/control/clock nets
53	$\overline{\text{ERR_OUT}}$	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
63	NC, CK1	CK1 terminated but not used on RDIMMs	CK1	Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated
64	NC, $\overline{\text{CK1}}$			
68	Par_In	Connected to the register on all RDIMMs	NC	Not used on UDIMMs
76	$\overline{\text{S1}}$	Connected to the register on all RDIMMs	$\overline{\text{S1}}$	Used for dual-rank UDIMMs; NC on single-rank UDIMMs
77	ODT1, NC	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	ODT1, NC	Used for dual-rank UDIMMs; NC on single-rank UDIMMs
79	$\overline{\text{S2}}$, NC	Connected to the register on quad-rank RDIMMs; NC on single- or dual-rank RDIMMs	NC	Not used on UDIMMs
167	NC	TEST input used only on bus analysis probes	NC	TEST input used only on bus analysis probes
169	CKE1	Connected to the register on dual- and quad-rank RDIMMs; NC on single-rank RDIMMs	CKE1, NC	Used for double-rank UDIMMs; NC on single-rank UDIMMs
171	A15	Connected to the register on all DIMMs	A15, NC	Depending on device density, may not be connected to SDRAMs on UDIMMs; however, these signals are terminated on UDIMMs; A15: not routed on some raw cards
175	A14		A14	
196	A13		A13	
198	$\overline{\text{S3}}$, NC	Connected to the register on quad-rank RDIMMs; NC on single- or dual-rank RDIMMs	NC	Not used on UDIMMs
39, 40, 45, 46, 158, 159, 164, 165	CB _n	Used on all RDIMMs ($n = 0...7$)	NC, CB _n	Used on x72 UDIMMs ($n = 0...7$); not used on x64 UDIMMs
125, 134, 143, 152, 161, 203, 212, 221, 230	DQS _n , TDQS _n	Connected to $\overline{\text{DQS}}$ on x4 DRAMs; $\overline{\text{TDQS}}$ on x8 RDIMM SDRAMs ($n = 9...17$)	DM _n	Connected to DM on x8 DRAMs; UDM or LDM on x16 UDIMM DRAMs ($n = 0...8$); DM8 is not used on x64 UDIMMs

Table 6 — Pinout Comparison Based on Module Type (Cont'd)

Pin	RDIMM		UDIMM	
	Signal	Notes	Signal	Notes
126, 135, 144, 153, 162, 204, 213, 222, 231	$\overline{DQS}_n, \overline{TDQS}_n$	Connected to \overline{DQS} on x4 DRAMs; \overline{TDQS} on x8 RDIMM SDRAMs ($n = 9...17$)	NC	$\overline{DQS}_9-\overline{DQS}_{17}$ and \overline{TDQS}_n are not used on UDIMMs.
187	\overline{EVENT}	Connected to thermal sensing component	\overline{EVENT} , NC	Connected to the thermal sensing component on ECC DIMMs. No connection on nonECC DIMMs

3.1 Address Mirroring Feature

There is a via grid located under the SDRAMs for wiring the CA signals (address, bank address, command, and control lines) to the SDRAM pins. The length of the traces from the vias to the SDRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.

The pins on the SDRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 SDRAM pins are wired straight, with no mismatch between the connector pin assignment and the SDRAM pin assignment. Some of the Rank 1 SDRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

Table 7 — SDRAM Pin Wiring for Mirroring

Connector Pin	SDRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

Figure 1 illustrates the wiring in both the mirrored and non-mirrored case. The lengths of the traces to the SDRAM pins, is obviously shorter. The via grid is smaller as well.

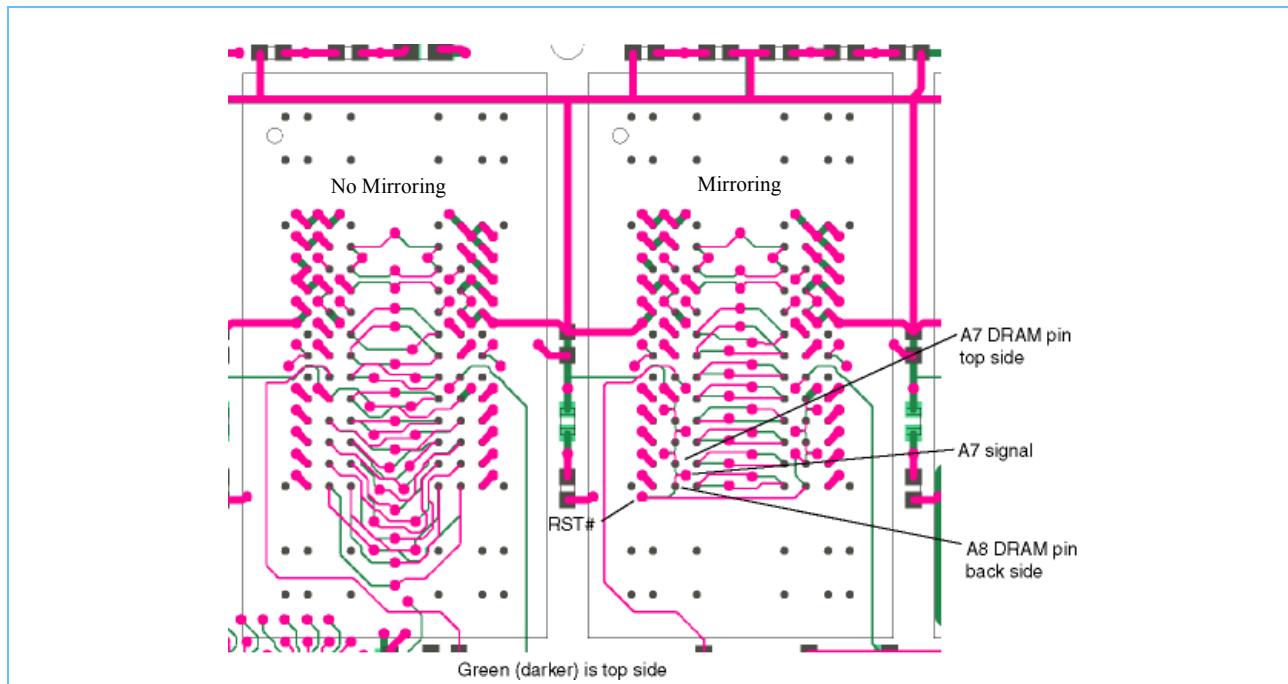


Figure 1 — Wiring Differences for Mirrored and Non-Mirrored Addresses

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a few rules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

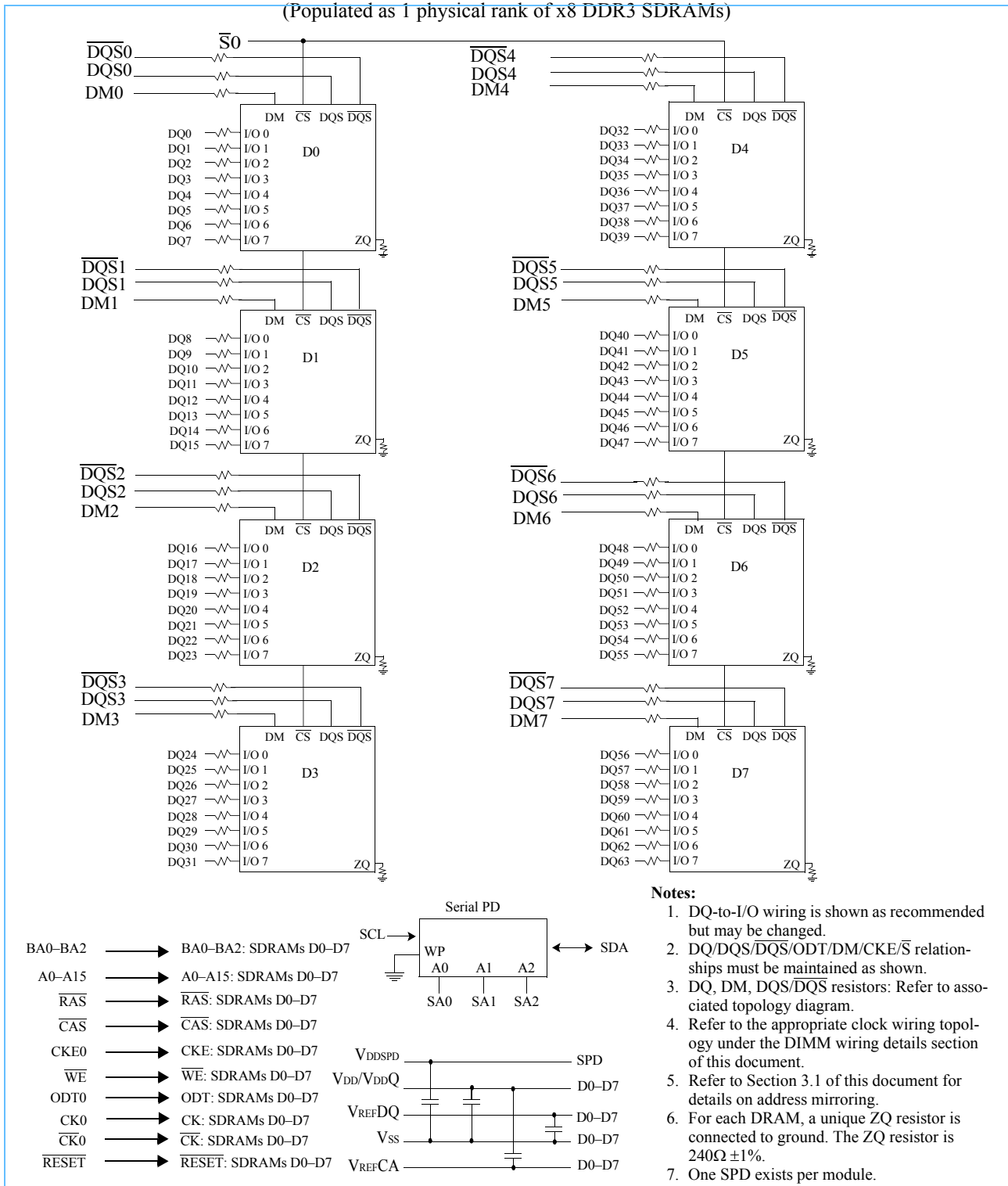


Figure 2 — Block Diagram: Raw Card Version A, x64

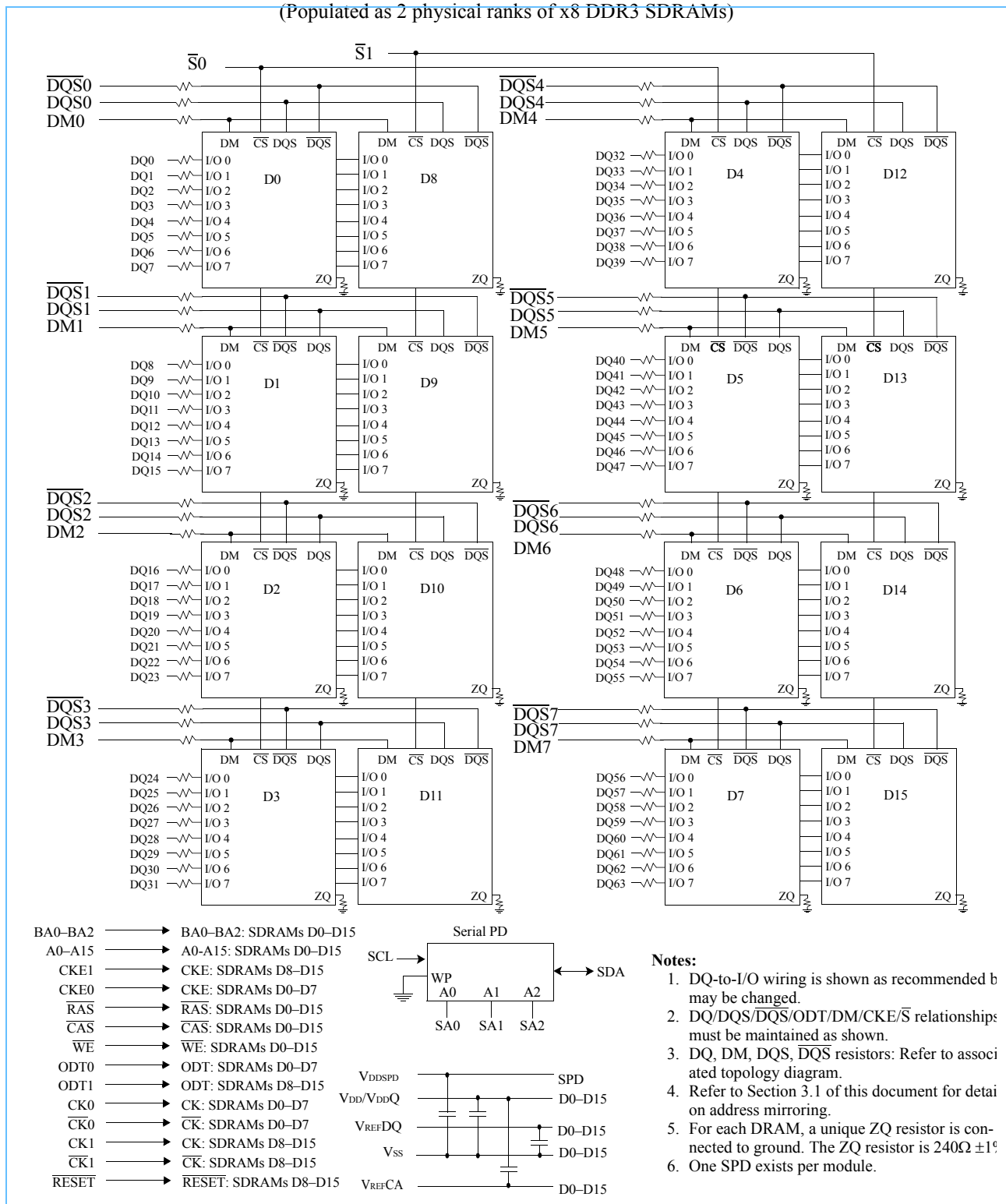


Figure 3 — Block Diagram: Raw Card Version B, x64

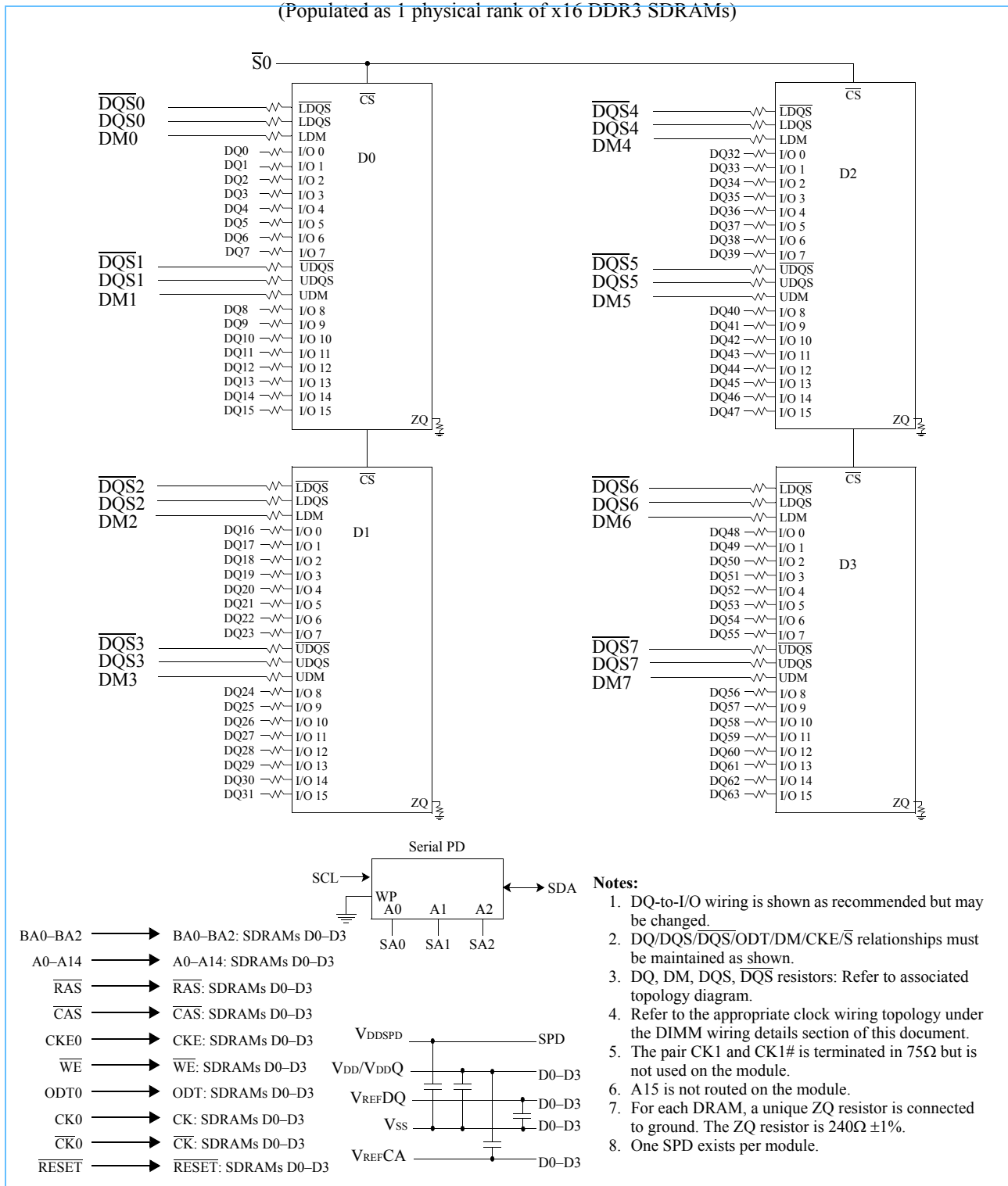


Figure 4 — Block Diagram: Raw Card Version C, x64

(Populated as 1 physical rank of x8 DDR3 SDRAMs)

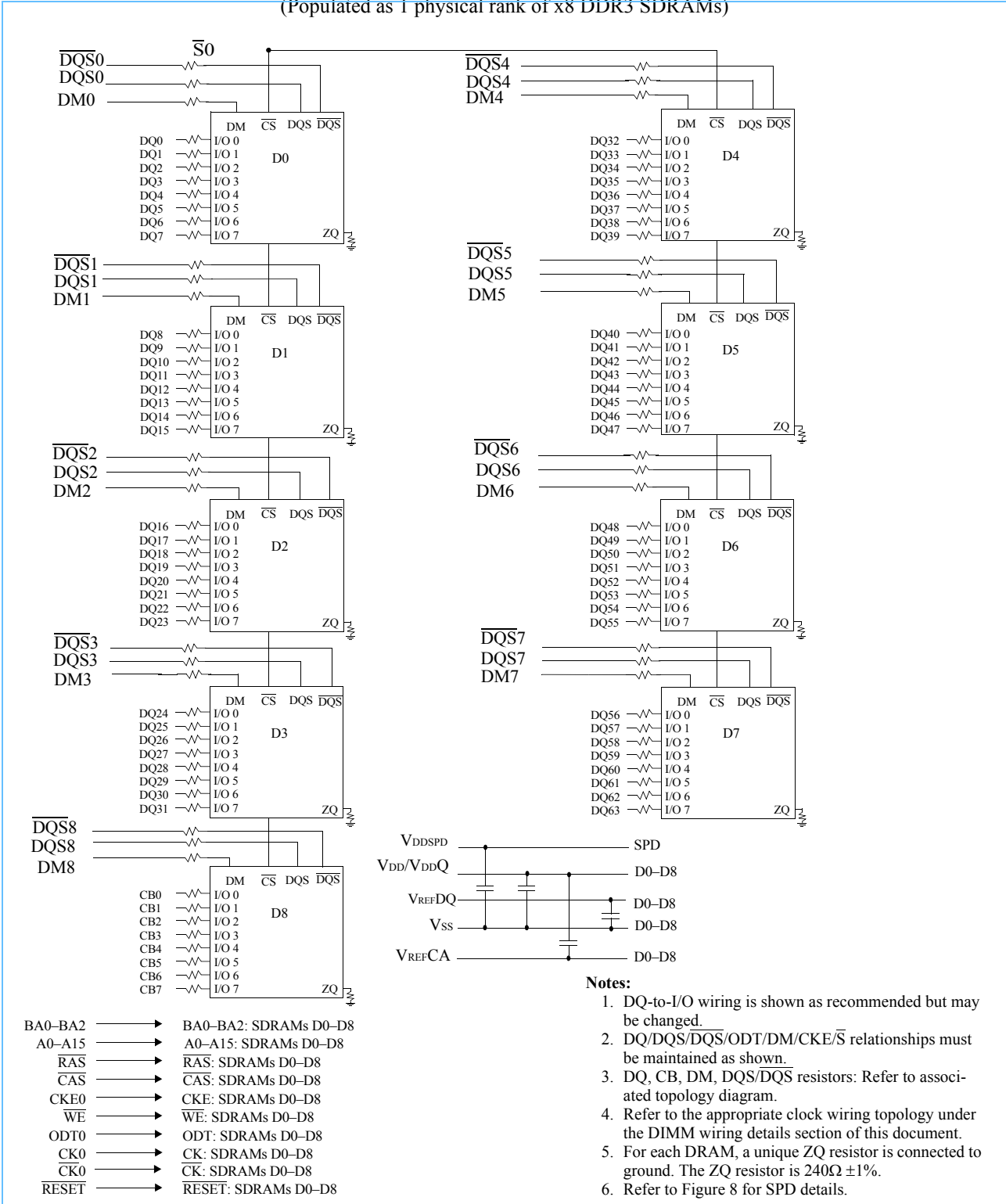


Figure 5 — Block Diagram: Raw Card Version D, x72

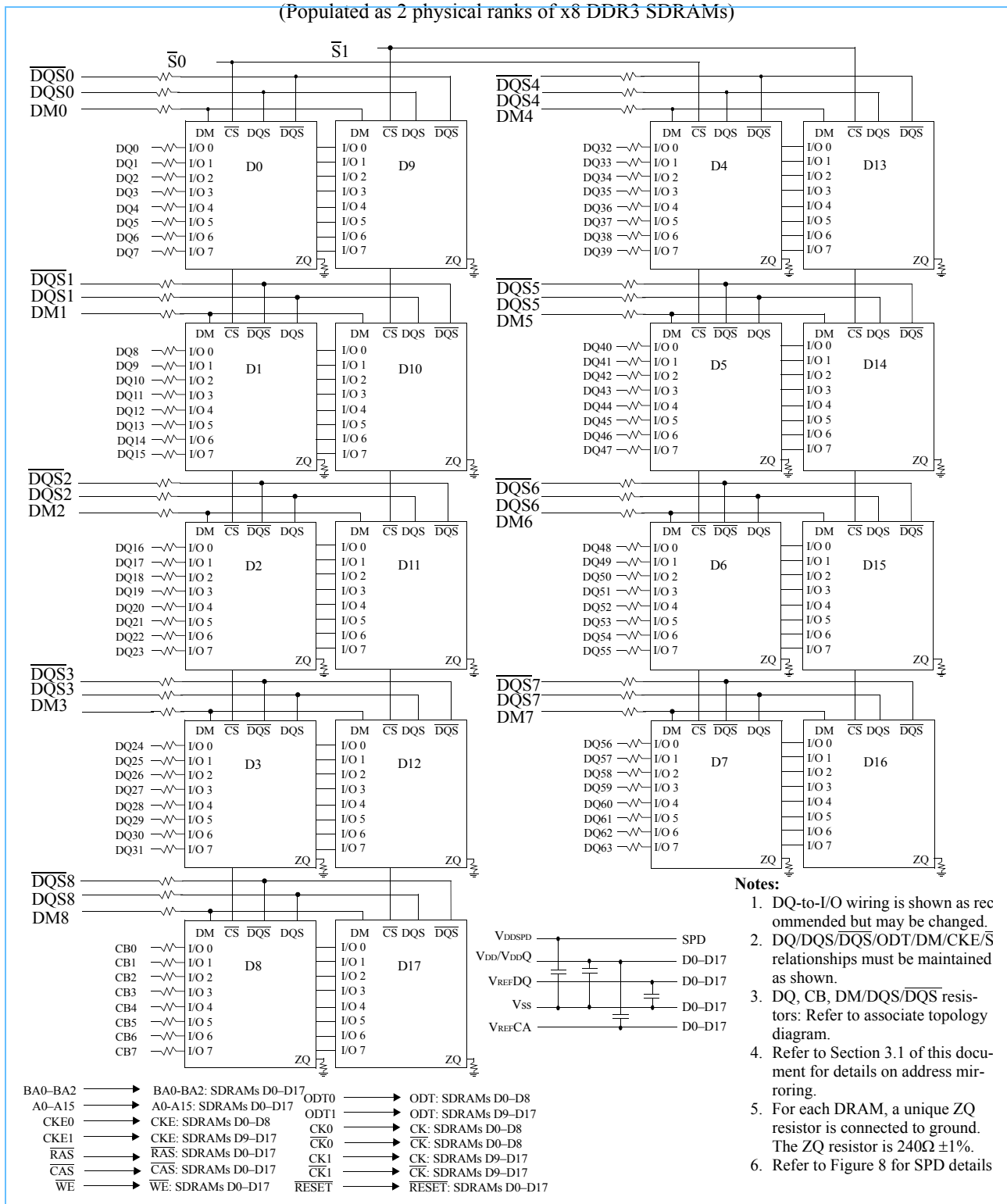


Figure 6 — Block Diagram: Raw Card Version E, x72

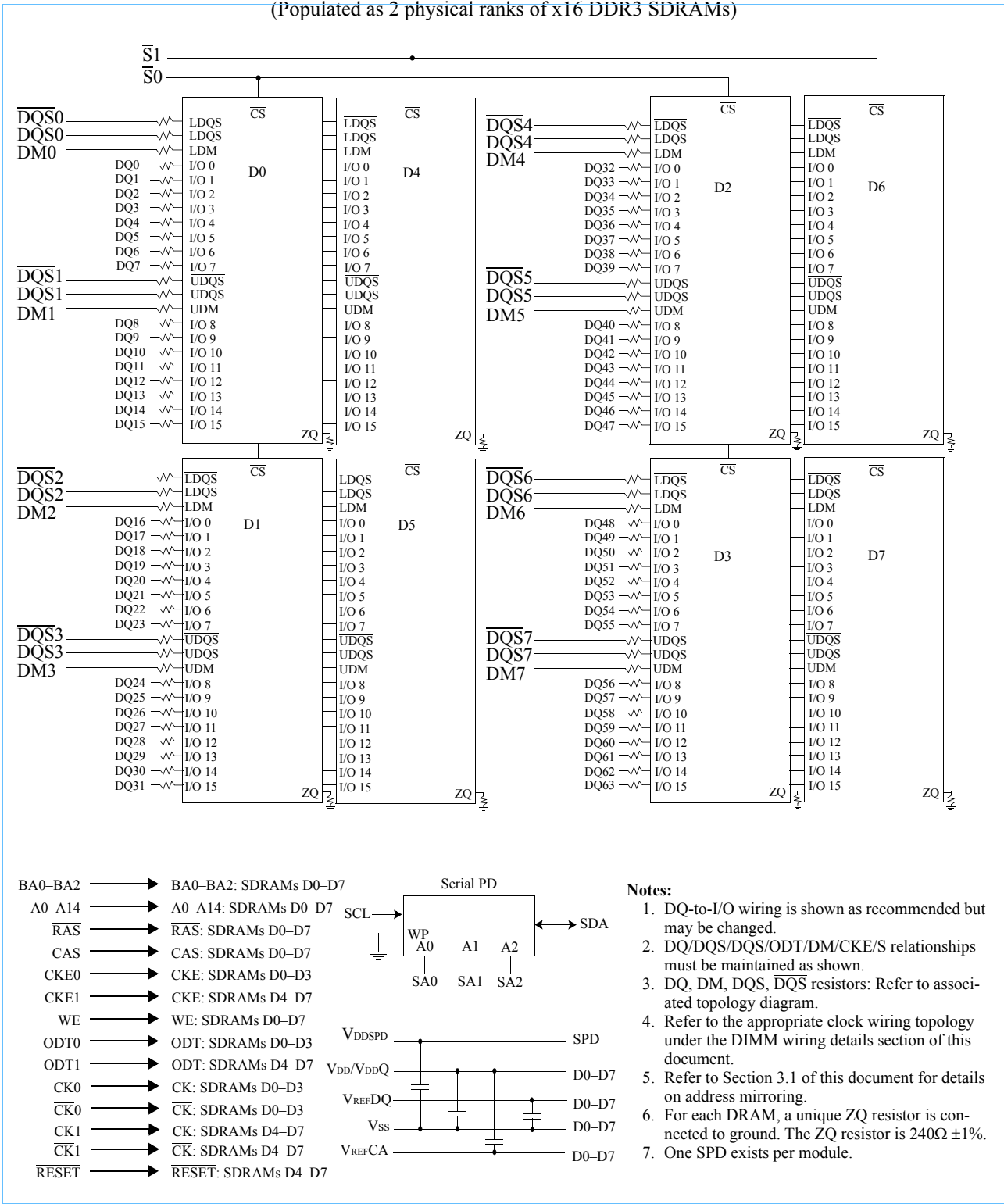


Figure 7 — Block Diagram: Raw Card Version F, x64

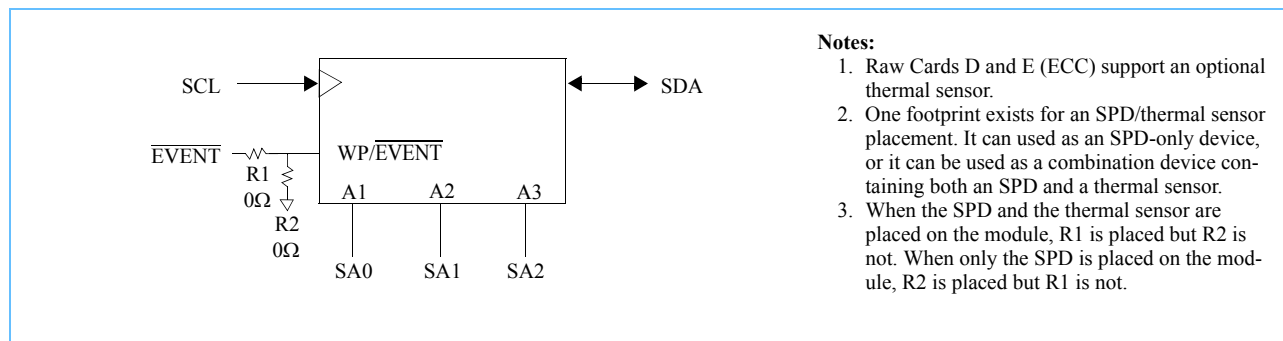


Figure 8 — Block Diagram: SPD and Thermal Sensor for Raw Cards D and E

An optional on-DIMM thermal sensor will provide DRAM temperature readout through a discrete or integrated thermal sensor.

On low-profile, 30mm DIMMs, the thermal sensor and serial presence-detect footprint will be placed near the center of the DIMM, both vertically and horizontally (refer to MO-269 for placement requirements). TDFN packages are used for the thermal sensor and the serial presence-detect. MO-229C, variations VCED-3 or VEED-7 will be referenced for the thermal sensor and serial presence-detect part. Raw Card D complies with the thermal sensor placement requirement on MO-269. Raw Card E complies with the thermal sensor placement requirement of MO-269.

4 Component Details

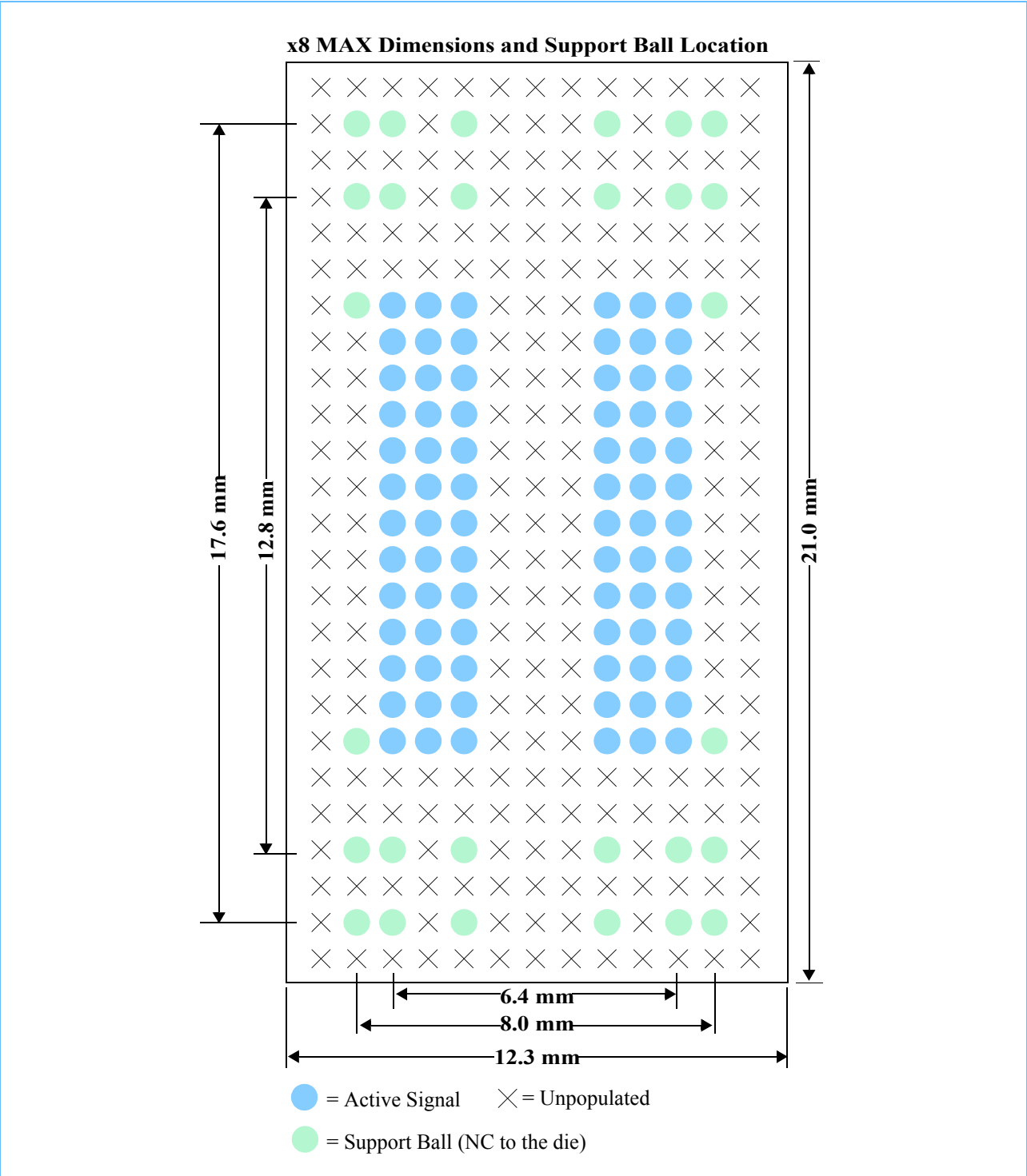


Figure 9 — DIMM Ball Pattern for x8 - 512Mb, 1Gb, 2Gb, 4Gb, and 8Gb DDR3 SDRAM Planar Components (Top View)

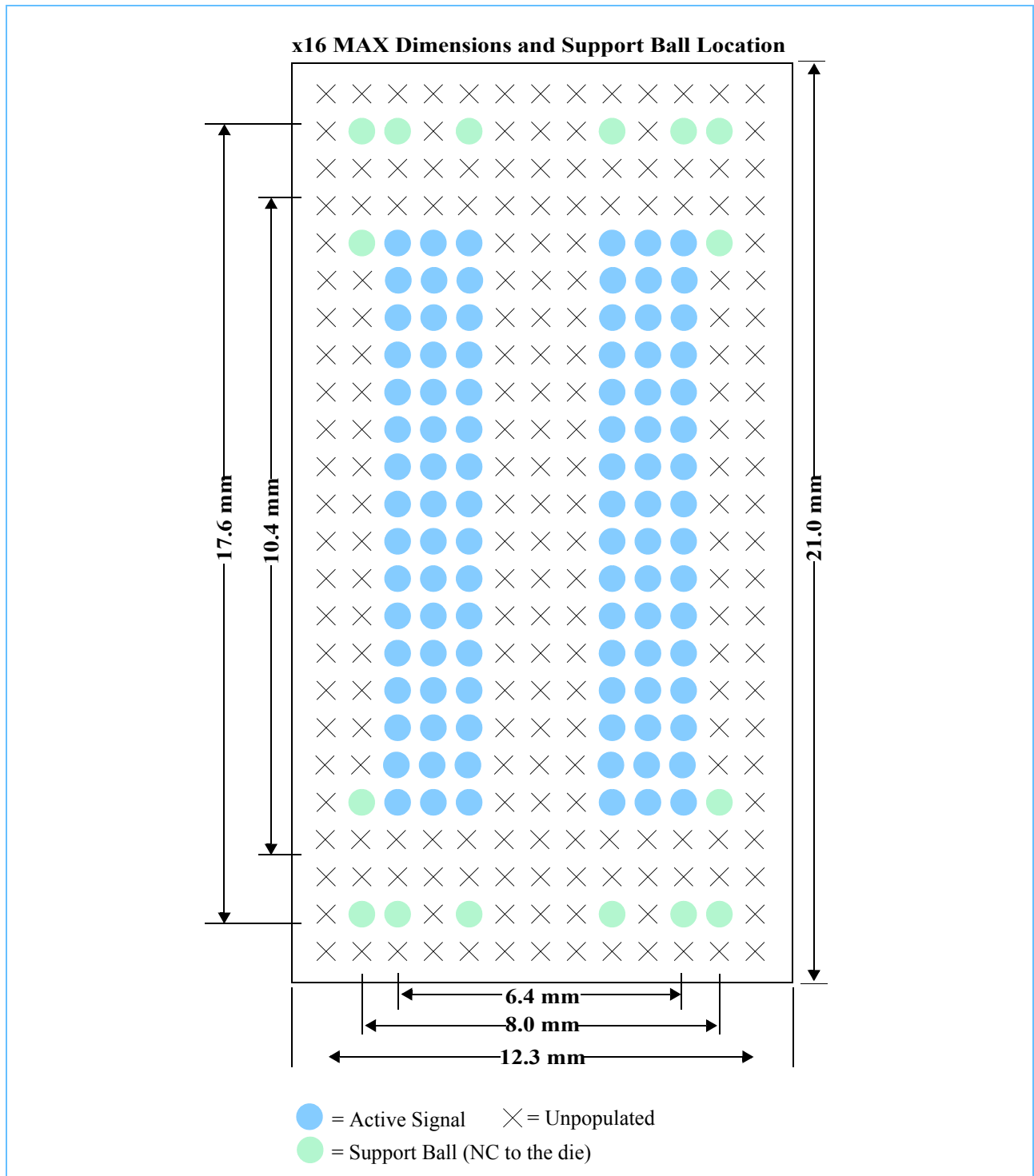


Figure 10 — DIMM Ball Pattern for x16 - 512Mb, 1Gb, 2Gb, 4Gb, and 8Gb DDR3 SDRAM Planar Components (Top View)

5 Unbuffered DIMM Details

Table 8 — SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM Capacity	DIMM Organization	SDRAM Density	SDRAM Organization	Number of SDRAMs	Number of Physical Ranks	Number of Banks in SDRAM	Number of Address Bits Row/Column
A	512MB	64 Meg x 64	512 Megabit	64 Meg x 8	8	1	8	13/10
	1GB	128 Meg x 64	1 Gigabit	128 Meg x 8	8	1	8	14/10
	2GB	256 Meg x 64	2 Gigabit	256 Meg x 8	8	1	8	15/10
	4GB	512 Meg x 64	4 Gigabit	512 Meg x 8	8	1	8	16/10
	8GB	1 Gig x 64	8 Gigabit	1 Gig x 8	8	1	8	16/11
B	1GB	128 Meg x 64	512 Megabit	64 Meg x 8	16	2	8	13/10
	2GB	256 Meg x 64	1 Gigabit	128 Meg x 8	16	2	8	14/10
	4GB	512 Meg x 64	2 Gigabit	256 Meg x 8	16	2	8	15/10
	8GB	1 Gig x 64	4 Gigabit	512 Meg x 8	16	2	8	16/10
	16GB	2 Gig x 64	8 Gigabit	1 Gig x 8	16	2	8	16/11
C ¹	256MB	32 Meg x 64	512 Megabit	32 Meg x 16	4	1	8	12/10
	512MB	64 Meg x 64	1 Gigabit	64 Meg x 16	4	1	8	13/10
	1GB	128 Meg x 64	2 Gigabit	128 Meg x 16	4	1	8	14/10
	2GB	256 Meg x 64	4 Gigabit	256 Meg x 16	4	1	8	15/10
D	512MB	64 Meg x 72	512 Megabit	64 Meg x 8	9	1	8	13/10
	1GB	128 Meg x 72	1 Gigabit	128 Meg x 8	9	1	8	14/10
	2GB	256 Meg x 72	2 Gigabit	256 Meg x 8	9	1	8	15/10
	4GB	512 Meg x 72	4 Gigabit	512 Meg x 8	9	1	8	16/10
	8GB	1 Gig x 72	8 Gigabit	1 Gig x 8	9	1	8	16/11
E	1GB	128 Meg x 72	512 Megabit	64 Meg x 8	18	2	8	13/10
	2GB	256 Meg x 72	1 Gigabit	128 Meg x 8	18	2	8	14/10
	4GB	512 Meg x 72	2 Gigabit	256 Meg x 8	18	2	8	15/10
	8GB	1 Gig x 72	4 Gigabit	512 Meg x 8	18	2	8	16/10
	16GB	2 Gig x 72	8 Gigabit	1 Gig x 8	18	2	8	16/11
F ¹	512MB	32 Meg x 64	512 Megabit	32 Meg x 16	8	2	8	12/10
	1GB	64 Meg x 64	1 Gigabit	64 Meg x 16	8	2	8	13/10
	2GB	128 Meg x 64	2 Gigabit	128 Meg x 16	8	2	8	14/10
	4GB	256 Meg x 64	4 Gigabit	256 Meg x 16	8	2	8	15/10

1. Registrations C0 and F0 do not wire A15 and therefore the 8Gb device is not supported on the registration.

Table 9 — Input Loading Matrix

Signal Names	Input Device	Raw Card Version A	Raw Card Version B	Raw Card Version C	Raw Card Version D	Raw Card Version E	Raw Card Version F
CK/ $\overline{\text{CK}}$	SDRAM	8	8	4	9	9	4
$\overline{\text{CS}}$ /CKE/ODT	SDRAM	8	8	4	9	9	4
Addr/ $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ /BA/ $\overline{\text{WE}}$	SDRAM	8	16	4	9	18	8
DQ/DQS/ $\overline{\text{DQS}}$ /DM	SDRAM	1	2	1	1	2	2
CB/DQS8/ $\overline{\text{DQS8}}$ /DM8	SDRAM	—	—	—	1	2	—
SCL/SDA/SA	EEPROM	1	1	1	1	1	1
$\overline{\text{RESET}}$	SDRAM	8	16	4	9	18	8

1. ODT1, CKE1, and CS1 have no loads on Raw Cards A, C, or D

5.1 DDR3 Unbuffered Design File Releases

"Reference" design file updates will be released as needed. This DDR3 Unbuffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

Note: Future design file releases will include both a date and a revision label. All changes to the design file are also documented within the 'read-me' file.

Table 10 — Design File Releases

Raw Card Version	Specification Revision	Applicable Gerber File	Notes
A			
B			
C			
D			
E			
F			

5.2 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins.

The following layouts suggest placement for raw card versions A, B, C, D, E, and F. Exact spacing is not provided but should be based on manufacturing constraints and signal routing constraints imposed by this design guide. For all dimensions, refer to MO-269.

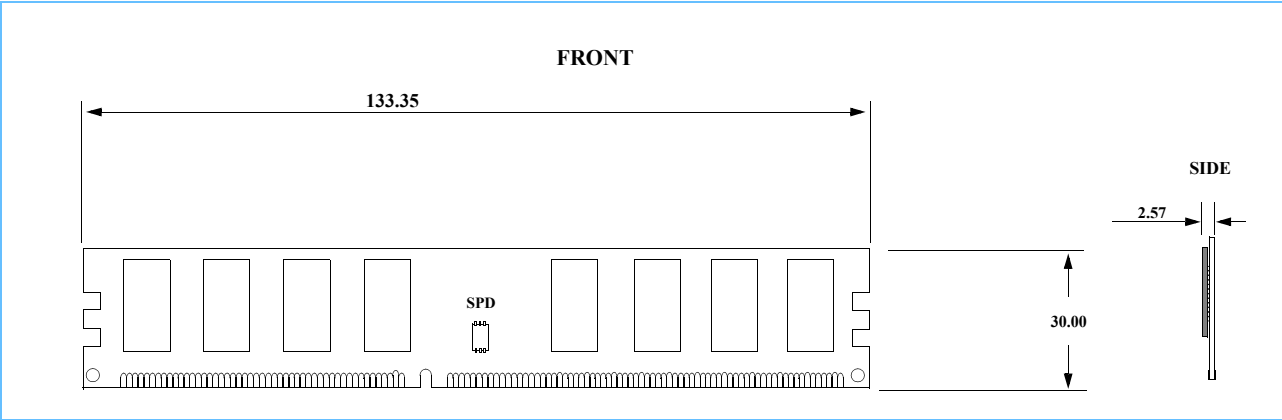


Figure 11 — Example Component Placement (Raw Card Version A)

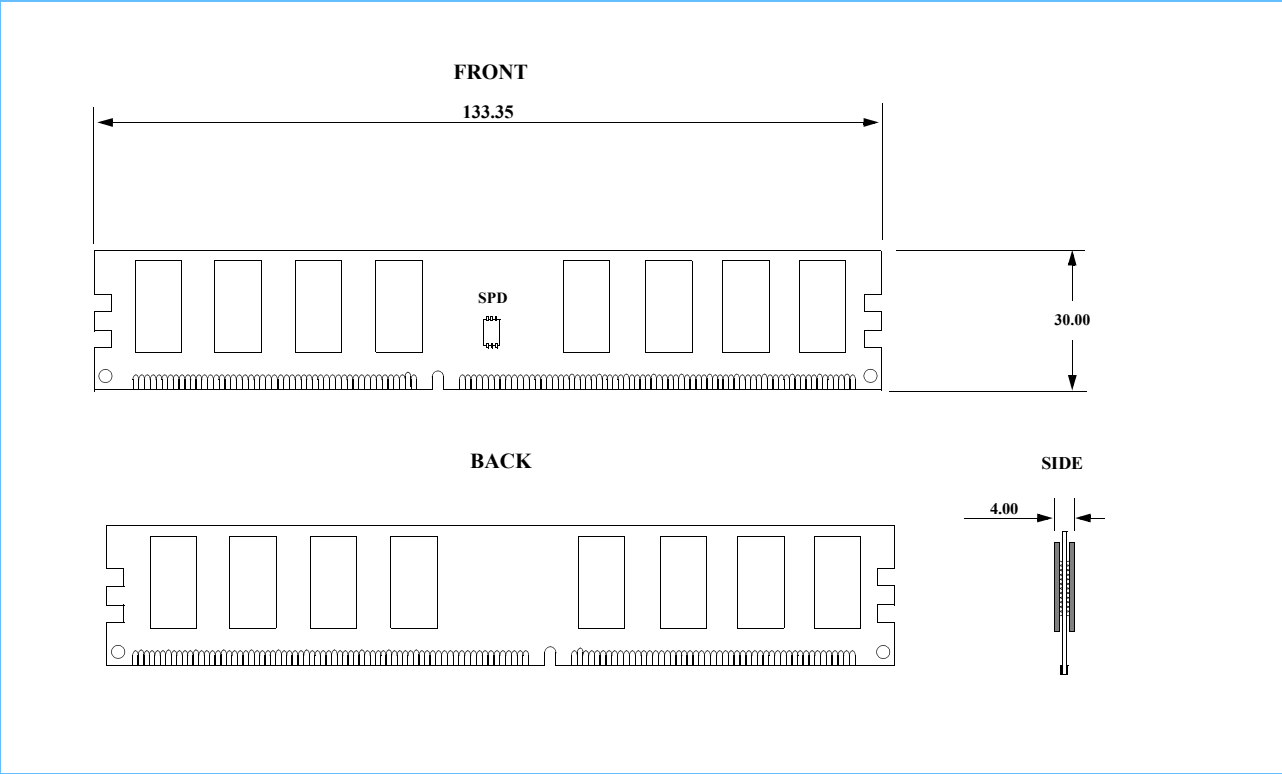


Figure 12 — Example Component Placement (Raw Card Version B)

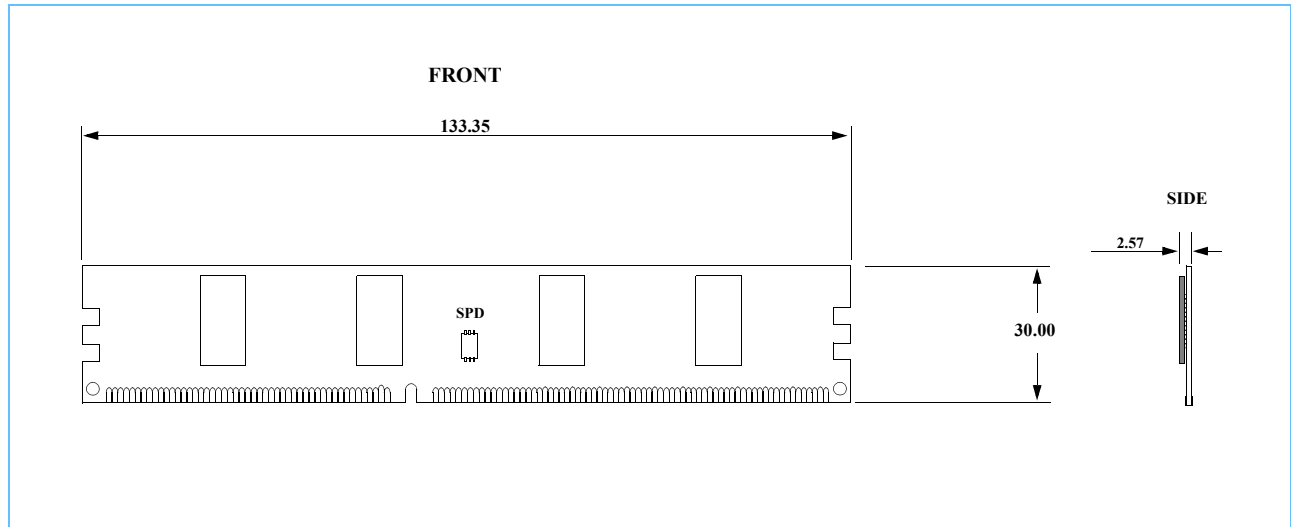


Figure 13 — Example Component Placement (Raw Card Version C)

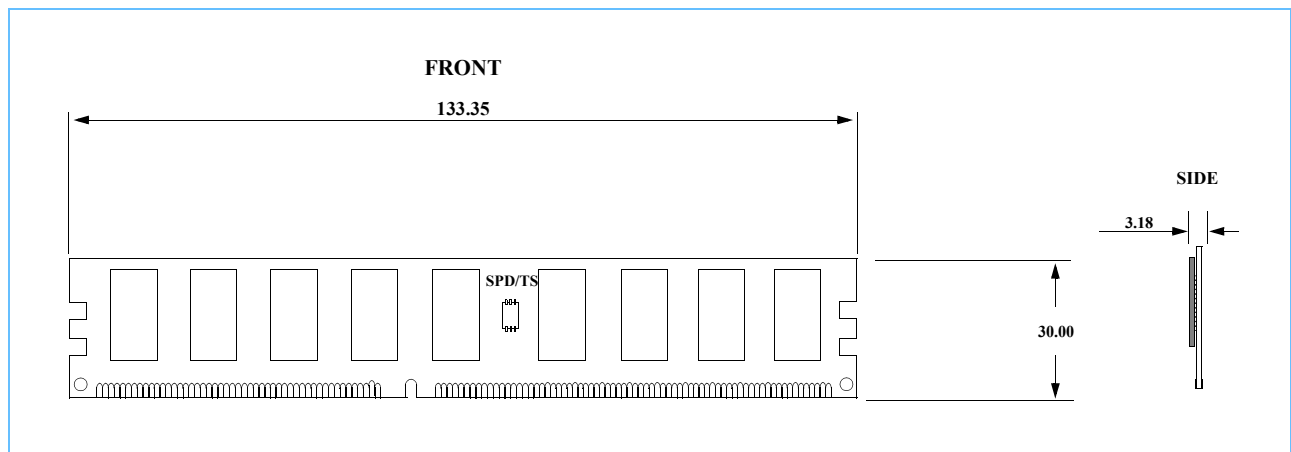


Figure 14 — Example Component Placement (Raw Card Version D)

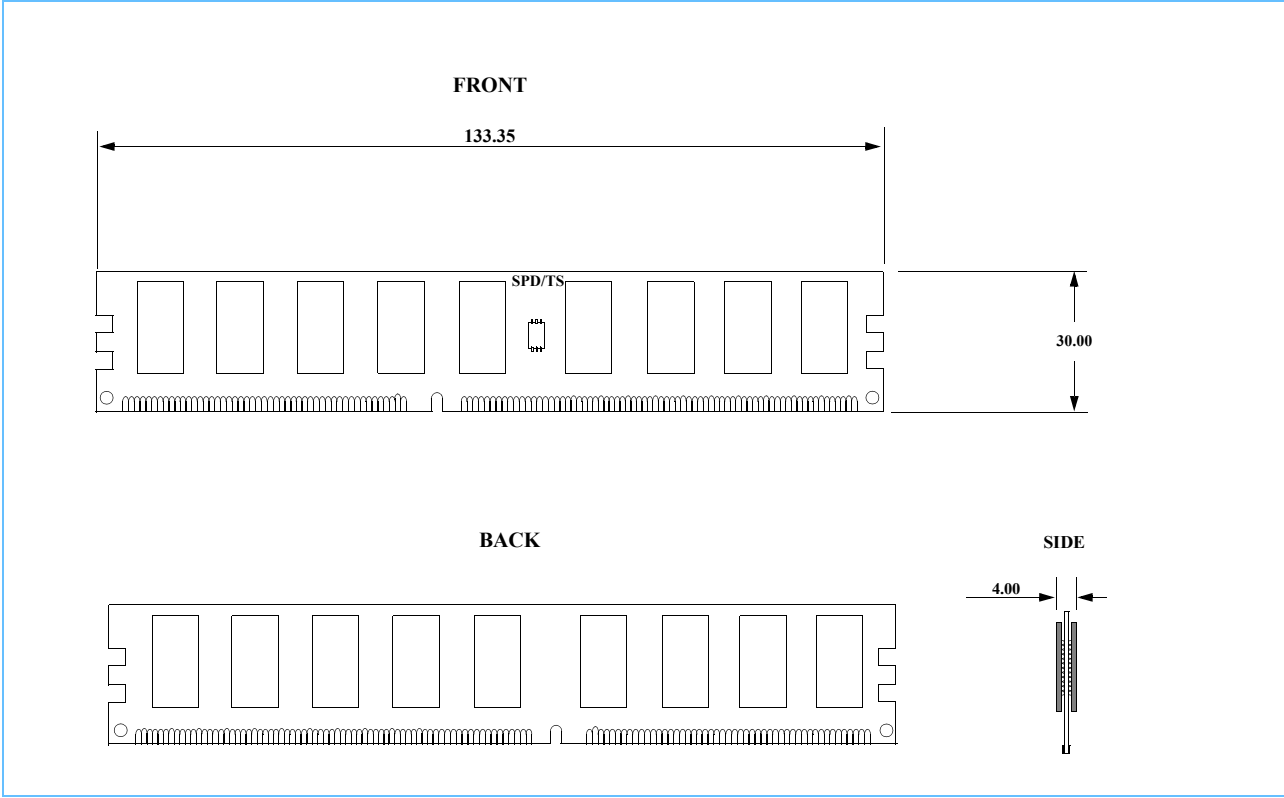


Figure 15 — Example Component Placement (Raw Card Version E)

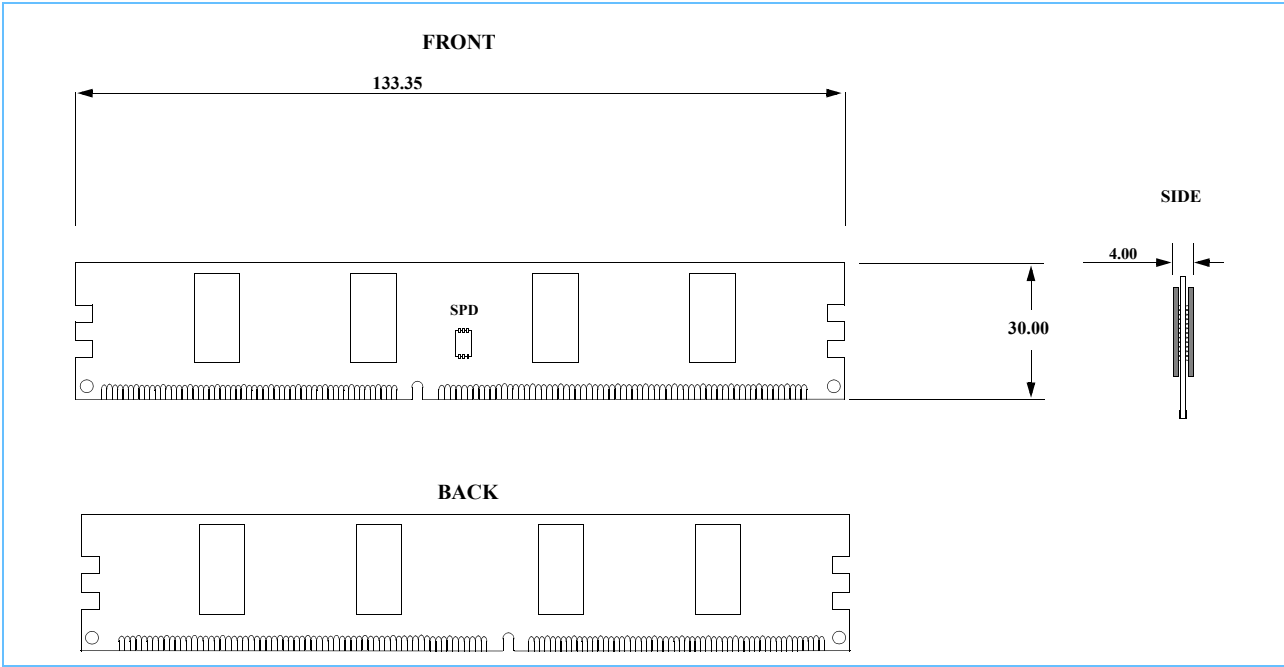


Figure 16 — Example Component Placement (Raw Card Version F)

5.3 Decoupling Guidelines

Table 11 — UDIMM Decoupling Capacitor Guidelines

	Value, Counts	Notes
V _{DD}	Minimum of two decoupling capacitors to V _{SS} per SDRAM	Should be placed as close as possible to the DRAM V _{DD} ball
	Minimum of four bulk decoupling capacitors to V _{SS} per module	
V _{TT}	Minimum of one decoupling capacitor to V _{DD} per every two termination resistors or a decoupling capacitor at both ends of each R _{PACK}	Should be placed as close as possible to the DRAM V _{DD} ball
	Minimum of one decoupling capacitor to V _{DD} (located near the card edge V _{TT} pin) or a decoupling capacitor at both ends of each R _{PACK}	
V _{REFCA}	Minimum of one decoupling capacitor to V _{DD} per DRAM	Should be placed as close as possible to the DRAM V _{REFCA} ball
	Minimum of one decoupling capacitor to V _{DD} (located near the card edge V _{REFCA} pin)	
V _{REFDQ}	Minimum of one decoupling capacitor to V _{SS} per DRAM	Should be placed as close as possible to the DRAM V _{REFDQ} ball
	Minimum of one decoupling capacitor to V _{SS} (located near the card edge V _{REFDQ} pin)	

1. Decoupling capacitor values vary by module and may be staggered to achieve best overall impedance vs. frequency response
2. Recommended values for decoupling are 0.01μf, 0.022μf, 0.047μf, 0.1μf, and 0.22μf
3. Recommended values for bulk decoupling are 1.0μf, 2.2μf, 3.3μf, and 4.7μf
4. Depending on the DRAM package size, all placements may not be possible

6 DIMM Wiring Details

6.1 Signal Groups

This specification categorizes DDR3 SDRAM timing-critical signals into four groups. The following table summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. They sweep from the left side of the module to the right.

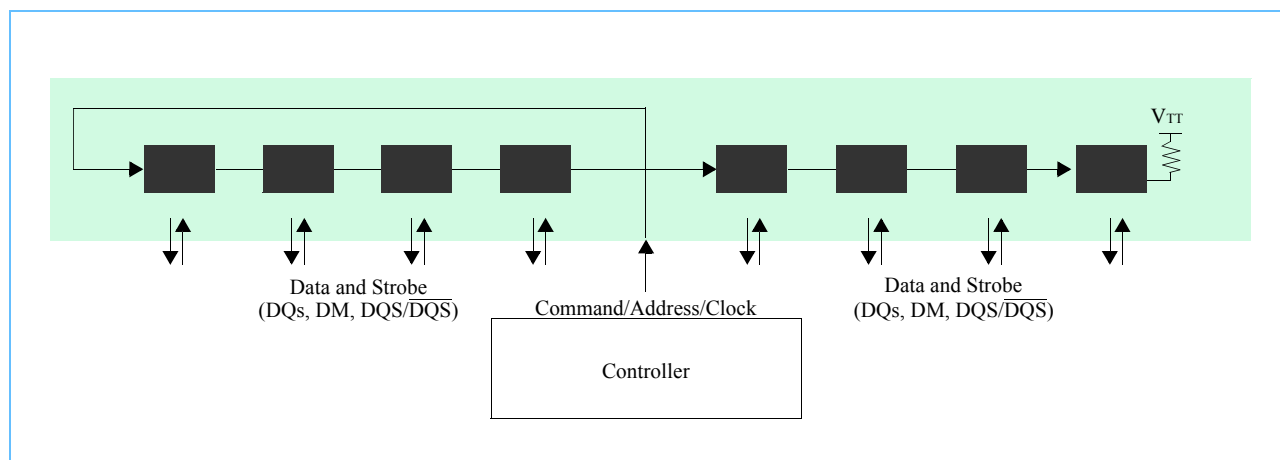


Figure 17 — Fly-By Topology

Table 12 — Timing-Critical Signals

Signal Group	Signals In Group	Raw Card Version	Page
Clock	CK0, $\overline{CK0}$	A, C, D	35, 37, 38
	CK0, $\overline{CK0}$, CK1, $\overline{CK1}$	B, E, F	36, 39, 40
Data	DQ, DM, DQS, \overline{DQS}	A, B, C, D, E, F	47, 49, 51, 53, 55, 57
Control	S0, ODT0, CKE0	A, C, D	41, 42, 42
	S0, S1, ODT0, ODT1, CKE0, CKE1	B, E, F	41, 43, 43
Address/Command	ADD, CMD	A, B, C, D, E, F	44, 44, 45, 45, 46, 46

6.2 General Net Structure Routing Rules

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that summarizes the minimum and maximum length for each trace segment in each signal group. The remainder of this section provides a general overview of DDR3 net structure concepts and documents the routing rules to be followed in the design of the DDR3 modules.

6.2.1 Clock, Control, and Address/Command Groups

Rather than the traditional tree structure utilized on legacy DDR modules, the DDR3 modules implement a fly-by topology for routing CK, CTRL, and ADD/CMD signal groups. Compared to legacy modules, the CTRL and ADD/CMD groups on DDR3 modules are length/delay matched to CK—between the connector and each SDRAM—resulting in a significantly reduced timing skew across these groups. This fundamental topology change is instrumental in enabling the higher operating speeds of DDR3. A summary table of the length/delay matching rules associated with these signal groups is provided below.

Table 13 — CK, CTRL, and ADD/CMD Group Length Matching Rules

Signal Group	Matching Rules
CK-to- $\overline{\text{CK}}$ Matching	Match TLx segment by TLx segment to within 0.1 mm
CK Pair-to-CK Pair Matching (Pair-to-Pair: Average Length)	Match total compensated length from connector to each SDRAM to within 0.25 mm
CTRL Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
CTRL-to-CK Matching	Match total compensated length of all CTRL signals from connector to each SDRAM to within CK ± 0.5 mm
ADR/CMD Group Matching	Match total compensated length from connector to each SDRAM to within 1.0 mm
ADR/CMD-to-CK Matching	Match total compensated length of all ADR/CMD signals from connector to each SDRAM to within CK ± 0.5 mm
TL2 Stub Length Matching	Match TL2 stub length at each SDRAM (top and bottom), on a given signal, to within 0.5 mm
TL2 MAX Stub Length Limits	TL2 ≤ 3.0 mm
CK First-to-Last Length	Maximum length from first SDRAM and last SDRAM = 153 mm
Neckdown Length	5.0 mm \leq length \leq 10.0 mm; match to within ± 1.0 mm
<ol style="list-style-type: none"> 1. All length matching is done using velocity compensated stripline equivalent lengths 2. A velocity compensation ratio of 1.1 will be used (MS length/1.1 = SL equivalent length) 3. Neckdown length is the trailing portion of the TL1 segment, which is routed at the standard 0.1 mm width 4. Maximum first-to-last length can be calculated by subtracting length to first SDRAM from length to last SDRAM 5. Via compensation is not required but is optional; via equivalent length is defined as 2.5 mm of microstrip 	

6.2.2 Lead-in vs. Loaded Sections

The CK, CTRL, and ADD/CMD topologies are conceptually divided into two topology sections. The segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section, while the segments that run between SDRAM node vias (TL3, TL4, TL5...), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section. The loaded section also contains the segments between the last SDRAM and the termination.

In order to reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, typically with the lead-in section routed at 40 ohms nominal, and the loaded section routed at 60 ohms nominal, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via, which is termed the neckdown length.

6.2.3 Length/Delay Matching to SDRAM Devices

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single-best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1 + TL2) be matched across the CK group, and then across the CTRL and ADD/CMD groups—as per the length matching guidelines—adjusting the CK length as needed to reach the length window of the CTRL and ADD/CMD groups. It is important to note that matching is done from connector to the SDRAM ball, and includes the TL2 segment. It is during this process that the breakout pattern dependent length variance in the TL2 stub on each signal will be tuned out.

Once length/delay matching to the first device is complete, the length matching to the remaining devices is straightforward and can be accomplished by simply length-matching the intra-node segments (TL3, TL4, TL5...), assuming the TL2 stub length for a given signal does not vary from SDRAM to SDRAM.

Note that it is recommended that the TL2 stub length on any given signal be closely matched on the top- and bottom-side pattern, and at each SDRAM. This will facilitate the most accurate overall length/delay matching.

The total compensated length from the connector to the first and last SDRAM is documented in the segment length tables for each module type, in the net structure definitions sections; however, it is assumed that the length matching rules are met at all SDRAM devices.

6.2.4 Velocity Compensation

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip (MS) and stripline (SL), the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnects. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

6.2.5 Data and Strobe Group

The DDR3 modules treat each byte lane as a separate signal sub-group, with each byte lane group length/delay matched with velocity compensation as previously described. The length of the individual byte lanes may vary substantially across the module, with the controller providing timing realignment circuitry. A summary table of the length/delay matching rules associated with the data signal group is provided below.

Table 14 — Data and Strobe Group Length Matching Rules

Signal Group	Matching Rules
DQS-to- $\overline{\text{DQS}}$ Matching	Match TLx segment by TLx segment to within 0.1 mm
DQ/DM to DQS within Byte Lane	Match total compensated length from the connector to each SDRAM of all DQ and DM signals within a byte lane to within $\text{DQS} \pm 0.2$ mm
Minimum Byte Lane Length	Minimum compensated length from the connector to the SDRAM shall not be less than 12.0 mm
Maximum Byte Lane Length	Maximum compensated length from the connector to the SDRAM shall not be greater than 32.0 mm
<ol style="list-style-type: none"> 1. All length matching is done using velocity compensated stripline equivalent lengths 2. A velocity compensation ratio of 1.1 will be used ($\text{MS length}/1.1 = \text{SL equivalent length}$) 3. Via compensation is required if the via count varies within a byte lane; via equivalent length = 2.5 mm 	

6.2.6 Via Compensation

Via compensation on the CK, CTRL, and ADD/CMD signal groups is not required but is to be implemented optionally at the discretion of the module designer. Via compensation is required on the DQ/DQS byte lanes, where the via count varies within a byte lane. This is the case on most single-sided modules. In all cases when via compensation is implemented, the via equivalent shall be defined as 2.5 mm of microstrip.

6.3 Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input.

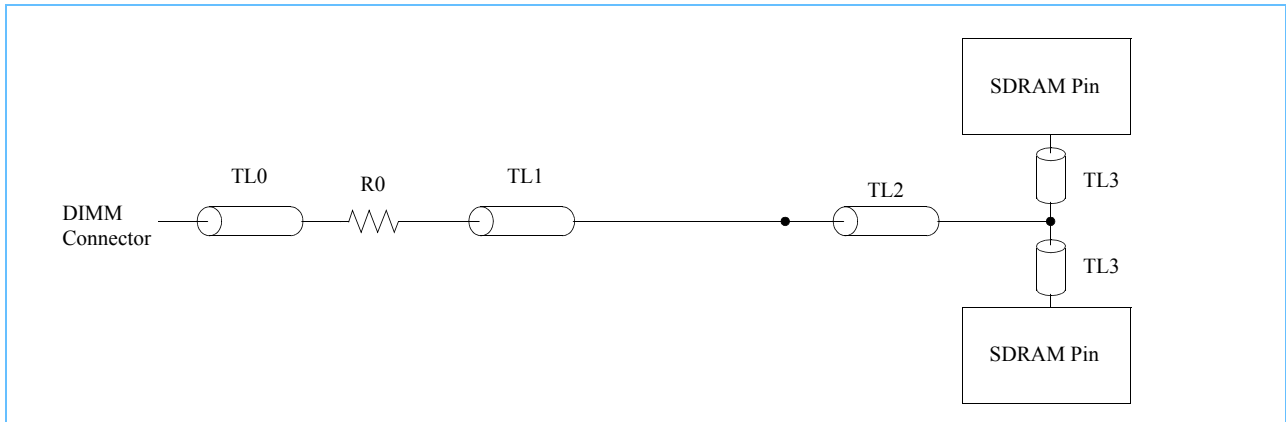


Figure 18 — Net Structure Example

A typical data net structure is shown in the following diagram.

6.4 Clock Net Structures

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

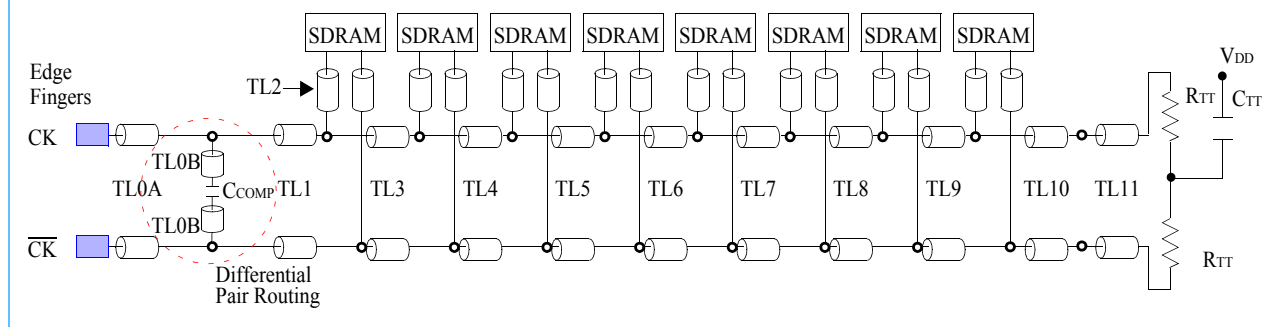


Figure 19 — Clock Net Structures (Raw Card Version A) CK0, $\overline{\text{CK0}}$

Table 15 — Trace Lengths for Clock Net Structures (Raw Card Version A) CK0, $\overline{\text{CK0}}$

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	First DRAM Compensated ²	Last DRAM Compensated ³	TL10	TL11	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL			MS				
MIN	4.2	1.1	94.0	1.0	15.3	15.3	15.3	24.8	15.3	15.3	15.3	98.9	215.5	11.7	0.7	2.2pF	36Ω	0.1μF
MAX	4.3	1.2	94.1	1.1	15.4	15.4	15.4	24.9	15.4	15.4	15.4	99.0	215.6	11.8	0.8	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL1 + TL2/1.1].
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9].
4. The pair CK1 and CK1# is routed to a 75Ω termination resistor but is not connected to any DRAM.

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

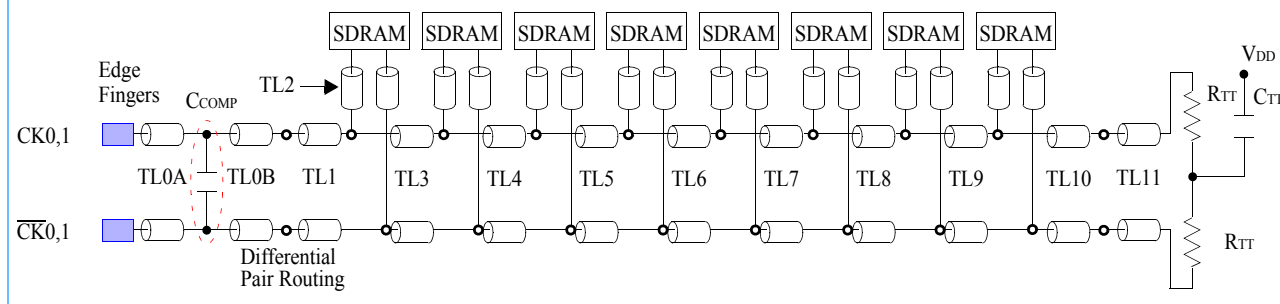


Figure 20 — Clock Net Structures (Raw Card Version B) CK0, $\overline{\text{CK0}}$, CK1, $\overline{\text{CK1}}$

**Table 16 — Trace Lengths for Clock Net Structures (Raw Card B)
CK0, CK0, CK1, CK1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated ²	Last DRAM Compensated ³	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	MS						
MIN	3.4	0.7	95.2	1.0	15.6	15.6	15.6	18.1	15.6	15.6	15.6	12.1	1.6	102.9	214.9	2.2pF	36Ω	0.1μF
MAX	3.4	4.0	95.9	1.2	15.7	15.7	15.7	18.1	15.7	15.7	15.7	13.0	1.8	103.0	215.0	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

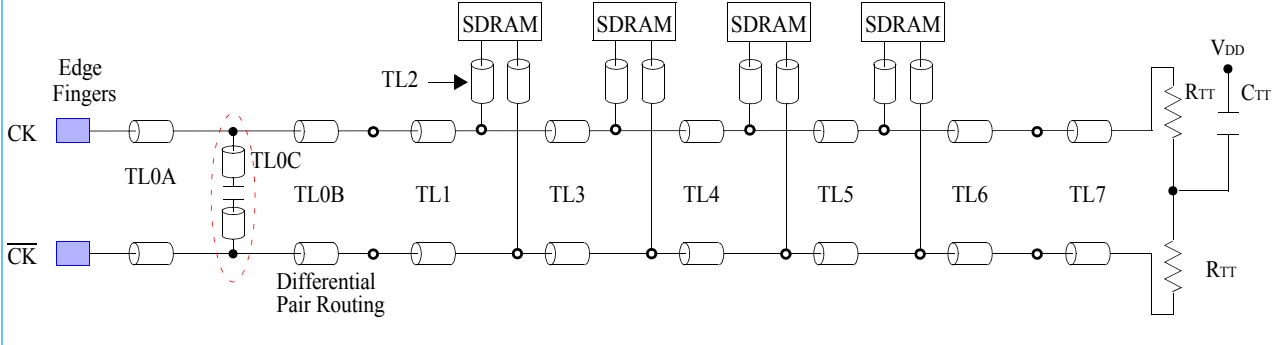


Figure 21 — Clock Net Structures (Raw Card Version C) CK0, CK0

Table 17 — Trace Lengths for Clock Net Structures (Raw Card C) CK0, CK0

Length (mm)	TL0A	TL0B	TL0C	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	MS	SL	MS	SL	SL	SL	SL	MS					
MIN	2.6	35.7	0.7	71.2	1.1	19.0	65.5	19.0	11.8	0.8	109.4	212.9	2.2pF	36Ω	0.1μF
MAX	2.6	35.7	0.8	71.2	1.1	19.0	65.5	19.0	11.8	0.8	109.4	212.9	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + 2.5/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + 2.5/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]
4. 2.5 mm of additional microstrip length is added to compensate for an extra via in the CK path
5. The pair CK1 and CK1# is routed to a 75Ω termination resistor but is not connected to any DRAM.

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

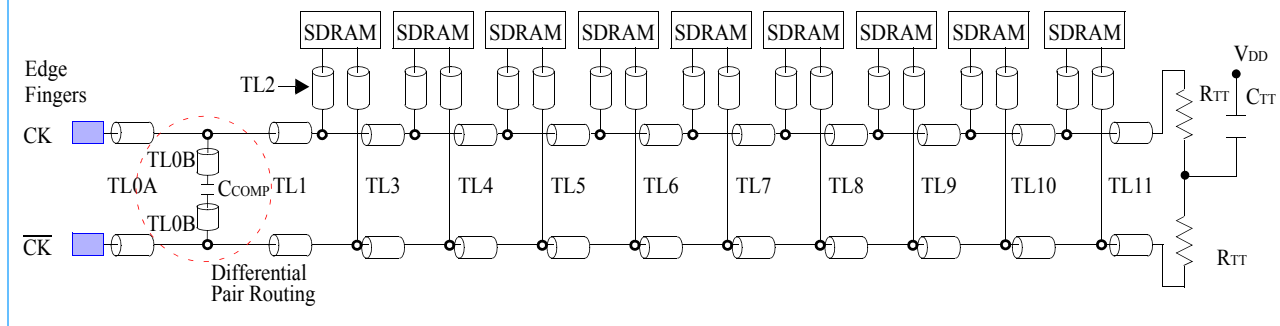


Figure 22 — Clock Net Structures (Raw Card Version D) CK0, $\overline{CK0}$

Table 18 — Trace Lengths for Clock Net Structures (Raw Card Version D) CK0, $\overline{CK0}$

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS						
MIN	2.0	1.3	92.5	2.1	14.0	14.0	14.0	14.0	16.6	14.0	14.0	14.0	10.4	1.4	96.2	210.9	2.2pF	36Ω	0.1μF
MAX	2.1	1.4	92.6	2.2	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	10.5	1.5	96.3	211.0	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10].
4. The pair CK1 and CK1# is routed to a 75Ω termination resistor but is not connected to any DRAM.

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

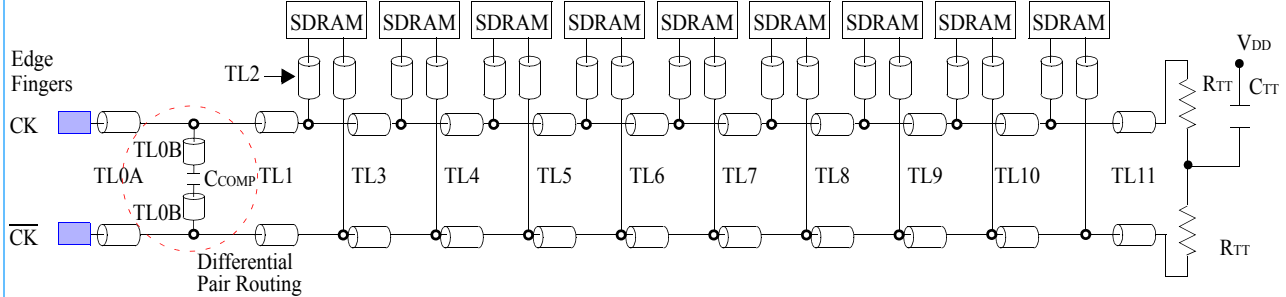


Figure 23 — Clock Net Structures (Raw Card Version E) $\overline{CK0}$, $\overline{CK1}$, $\overline{CK1}$

Table 19 — Trace Lengths for Clock Net Structures (Raw Card Version E) $\overline{CK0}$, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK1}$

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS						
MIN	2.1	0.8	95.0	1.9	14.0	14.0	14.0	14.0	18.2	14.0	14.0	14.0	9.1	2.0	100.5	216.8	2.2pF	36Ω	0.1μF
MAX	4.0	1.2	97.0	2.1	14.1	14.1	14.1	14.1	19.1	14.1	14.1	14.1	9.9	2.8	100.6	217.6	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]

SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality (slew rate and crossing point)
- Rise/fall time
- SDRAM component edge skew

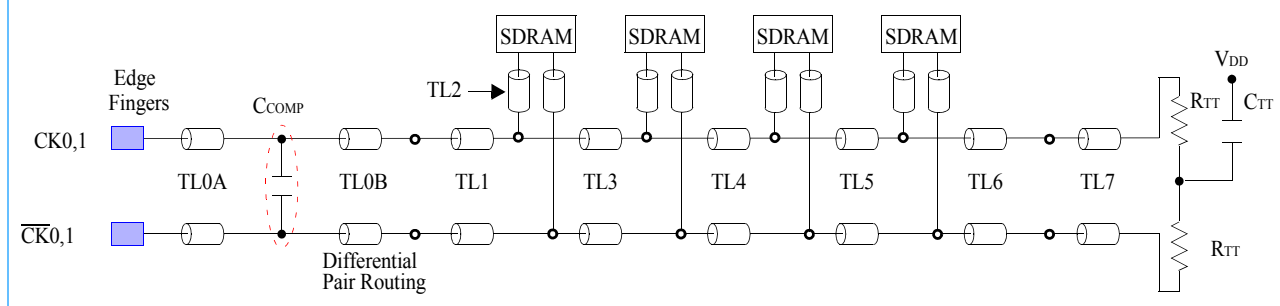


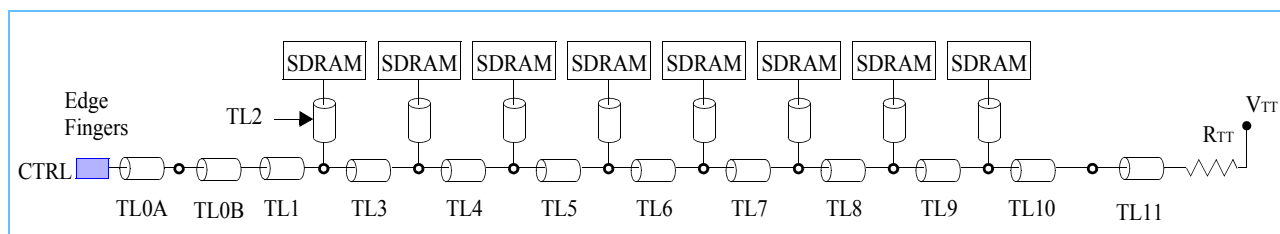
Figure 24 — Clock Net Structures (Raw Card Version F) $\overline{CK0}$, CK0, CK1, $\overline{CK1}$

Table 20 — Trace Lengths for Clock Net Structures (Raw Card Version F) $\overline{CK0}$, CK0, CK1, $\overline{CK1}$

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	C _{COMP}	R _{TT}	C _{TT}
	MS	MS	SL	MS	SL	SL	SL	MS						
MIN	3.4	30.4	78.9	1.0	19.6	67.8	19.6	16.2	0.8	112.8	219.8	2.2pF	36Ω	0.1μF
MAX	3.4	30.4	78.9	1.0	19.6	67.8	19.6	16.2	0.8	112.8	219.8	2.2pF	36Ω	0.1μF

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]

6.5 Net Structure Routing for Control

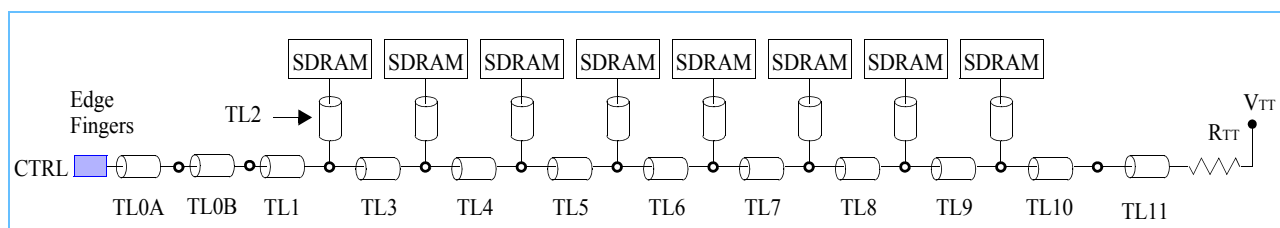


**Figure 25 — Net Structure Routing for Control (Raw Card Version A)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

**Table 21 — Trace Lengths for Control Net Structures (Raw Card Version A)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	2.0	0.0	92.0	0.5	15.3	15.3	15.3	24.8	15.3	15.3	15.3	4.3	0.7	98.7	215.5	39Ω
MAX	6.6	0.0	96.4	0.6	15.4	15.4	15.4	24.9	15.4	15.4	15.4	11.8	1.1	98.7	215.5	39Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

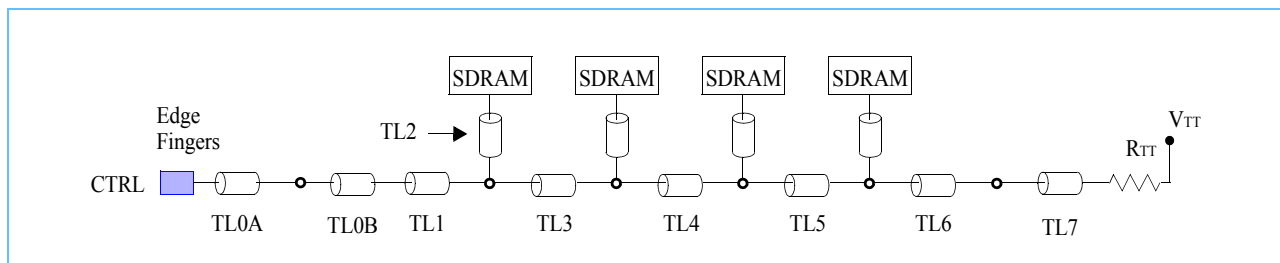


**Figure 26 — Net Structure Routing for Control (Raw Card Version B)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

**Table 22 — Trace Lengths for Control Net Structures (Raw Card Version B)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	1.6	0.0	91.9	0.6	15.6	15.6	15.6	18.1	15.6	15.6	15.6	6.0	0.9	102.9	215.0	39Ω
MAX	6.6	7.1	100.8	0.8	15.7	15.7	15.7	18.2	15.7	15.7	15.7	14.9	1.8	103.0	215.1	39Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

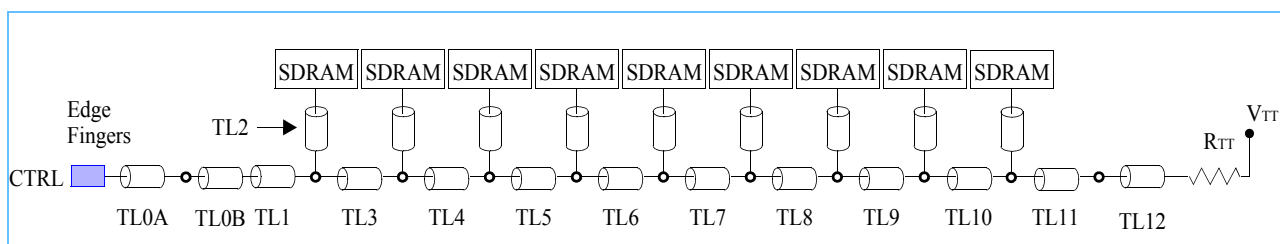


**Figure 27 — Net Structure Routing for Control (Raw Card Version C)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

**Table 23 — Trace Lengths for Control Net Structures (Raw Card Version C)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	34.1	0.0	57.1	1.2	19.0	65.5	19.0	13.3	0.7	107.0	210.5	36Ω
MAX	53.6	0.0	74.8	1.4	19.0	65.5	19.0	13.8	1.3	107.0	210.5	36Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]

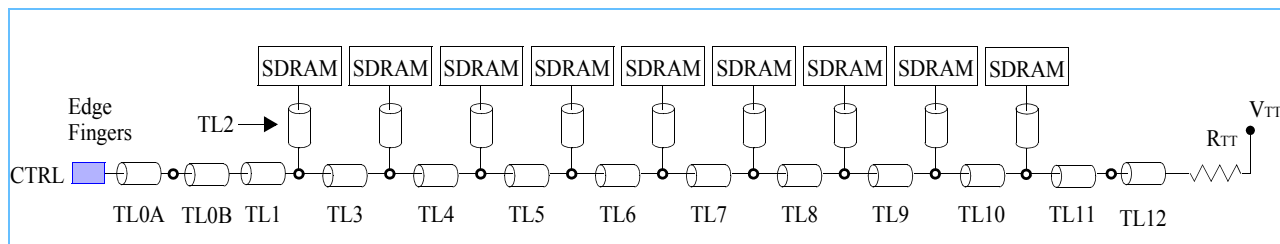


**Figure 28 — Net Structure Routing for Control (Raw Card Version D)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

**Table 24 — Trace Lengths for Control Net Structures (Raw Card Version D)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS				
MIN	2.0	0.0	0.0	0.5	13.9	13.9	13.9	13.9	16.6	13.9	13.9	13.9	4.0	2.0	96.1	210.7	39Ω
MAX	104.6	0.0	94.0	2.3	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	10.2	3.0	96.4	211.1	39Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
3. Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]

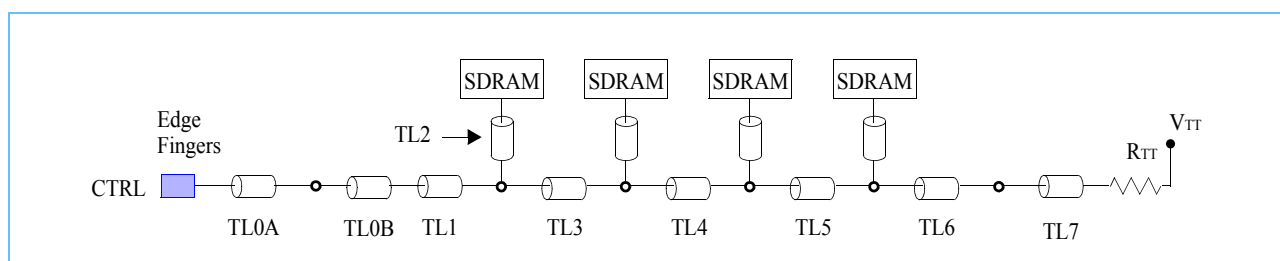


**Figure 29 — Net Structure Routing for Control (Raw Card Version E)
S0, S1, ODT0, ODT1, CKE0, CKE1**

**Table 25 — Trace Lengths for Control Net Structures (Raw Card Version E)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	9.7	0.0	17.4	0.5	14.0	14.0	14.0	14.0	18.9	14.0	14.0	14.0	2.8	1.3	100.5	216.2	39Ω
MAX	90.6	0.0	91.2	1.4	14.1	14.1	14.1	14.1	19.0	14.1	14.1	14.1	12.4	2.5	100.6	217.6	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]



**Figure 30 — Net Structure Routing for Control (Raw Card Version F)
S0, S1, ODT0, ODT1, CKE0, CKE1**

**Table 26 — Trace Lengths for Control Net Structures (Raw Card Version F)
S0, S1, ODT0, ODT1, CKE0, and CKE1**

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	1.9	0.0	64.8	2.2	19.6	67.8	19.6	13.3	0.7	112.8	219.7	39Ω
MAX	50.9	43.9	93.7	2.2	19.6	67.8	19.6	13.8	1.3	113.0	220.0	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]

6.6 Net Structure Routing for Address/Command

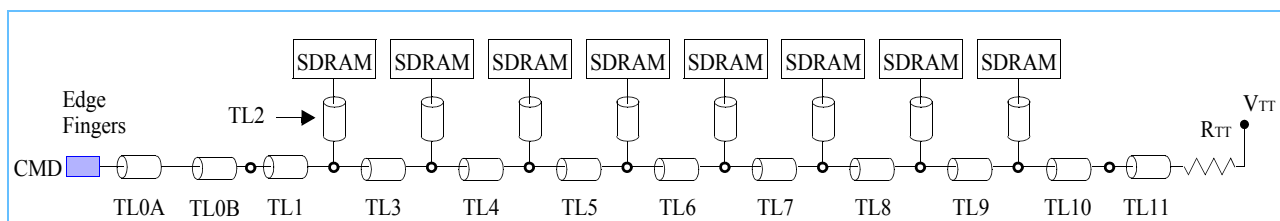


Figure 31 — Net Structure Routing for Address and Command (Raw Card Version A)

Table 27 — Trace Lengths for Address and Command Net Structures (Raw Card Version A)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	1.9	0.0	9.0	0.5	15.3	15.3	15.3	24.8	15.3	15.3	15.3	3.6	0.7	98.6	215.4	39Ω
MAX	98.1	0.0	95.7	2.3	15.4	15.4	15.4	24.9	15.4	15.4	15.4	12.5	1.9	98.7	216.0	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

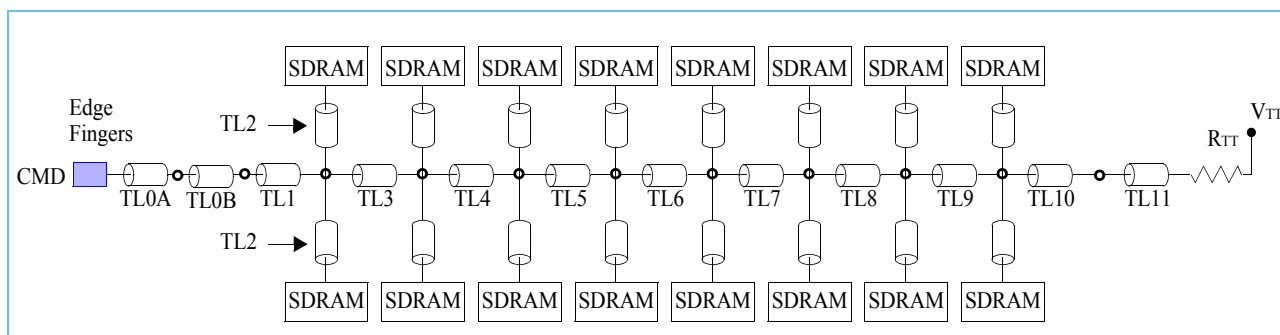


Figure 32 — Net Structure Routing for Address and Command (Raw Card Version B)

Table 28 — Trace Lengths for Address and Command Net Structures (Raw Card Version B)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	1.6	0.0	8.6	1.6	15.6	15.6	15.6	18.1	15.6	15.6	15.6	4.3	0.8	102.6	214.6	39Ω
MAX	102.0	97.3	79.6	2.4	15.7	15.7	15.7	18.2	15.7	15.7	15.7	13.2	1.7	103.5	215.5	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9]

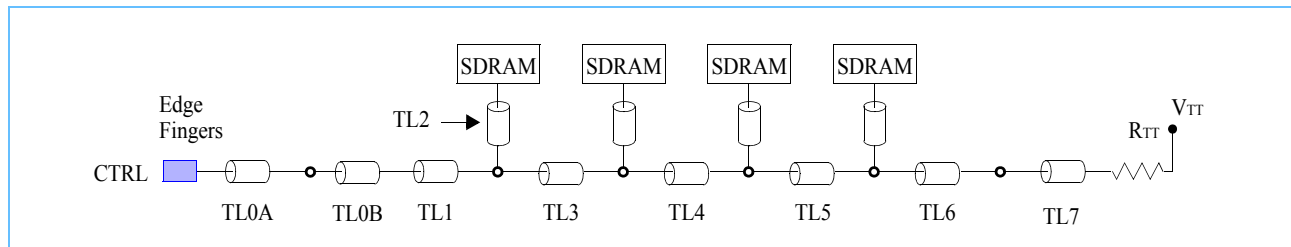


Figure 33 — Net Structure Routing for Address and Command (Raw Card Version C)

Table 29 — Trace Lengths for Address and Command Net Structures (Raw Card Version C)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	4.0	0.0	41.3	2.5	19.0	65.5	19.0	13.3	0.7	107.0	210.5	39Ω
MAX	69.8	0.0	100.6	3.0	19.0	65.5	19.0	13.8	1.3	107.0	210.5	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]
- A15 is not routed on the module

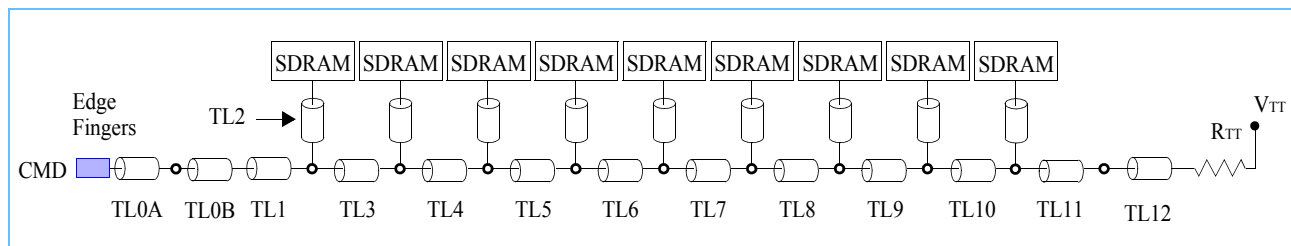


Figure 34 — Net Structure Routing for Address and Command (Raw Card Version D)

Table 30 — Trace Lengths for Address and Command Net Structures (Raw Card Version D)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	SL	MS			
MIN	2.0	0.0	0.0	0.5	13.9	13.9	13.9	13.9	16.6	13.9	13.9	13.9	5.3	1.0	96.1	210.7	39Ω
MAX	104.6	0.0	94.0	2.3	14.1	14.1	14.1	14.1	16.7	14.1	14.1	14.1	13.0	2.1	96.4	211.1	39Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to first DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].
- Equivalent stripline length to last DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10].
- R_{TT} resistor tolerance is 2 percent.

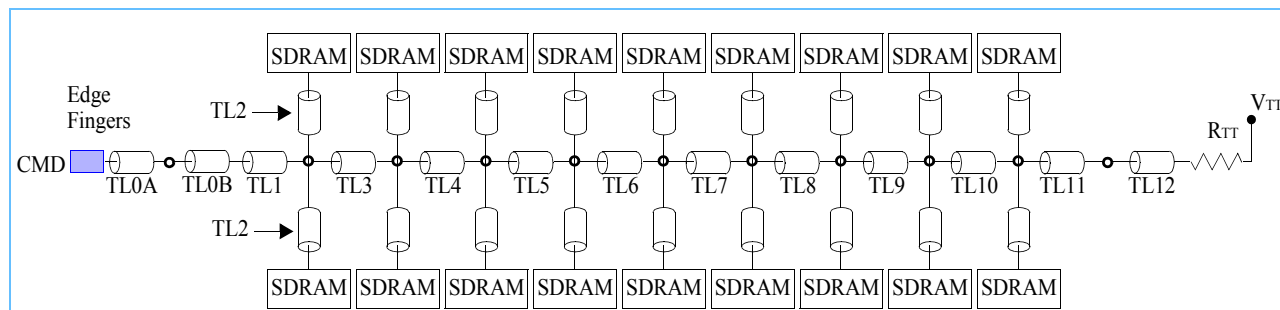


Figure 35 — Net Structure Routing for Address and Command (Raw Card Version E)

Table 31 — Trace Lengths for Address and Command Net Structures
(Raw Card Version E)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	TL8	TL9	TL10	TL11	TL12	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	SL	SL	SL	SL	MS				
MIN	9.7	0.0	17.4	0.5	14.0	14.0	14.0	13.9	18.9	14.0	14.0	14.0	5.2	1.2	100.5	216.2	39Ω
MAX	90.6	0.0	91.2	1.4	14.1	14.1	14.1	14.1	19.0	14.1	14.1	14.1	11.6	2.7	100.6	217.6	39Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.
3. Equivalent stripline length to last DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5 + TL6 + TL7 + TL8 + TL9 + TL10]$.
4. R_{TT} resistor tolerance is 2 percent.

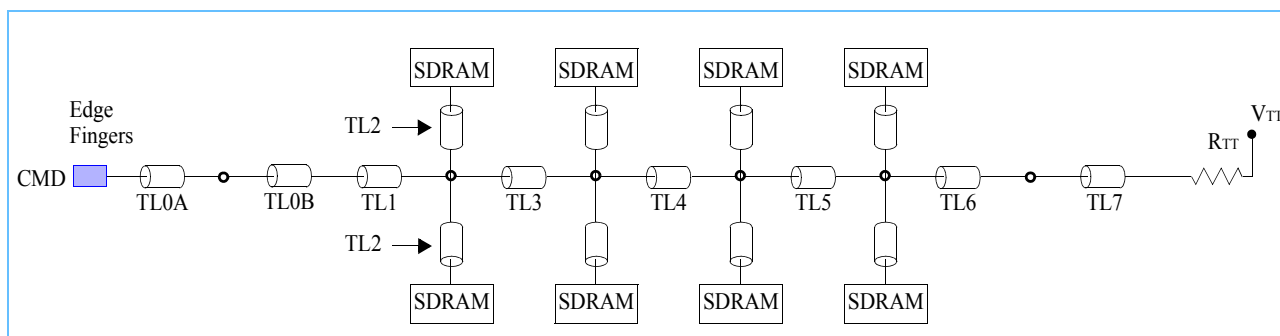


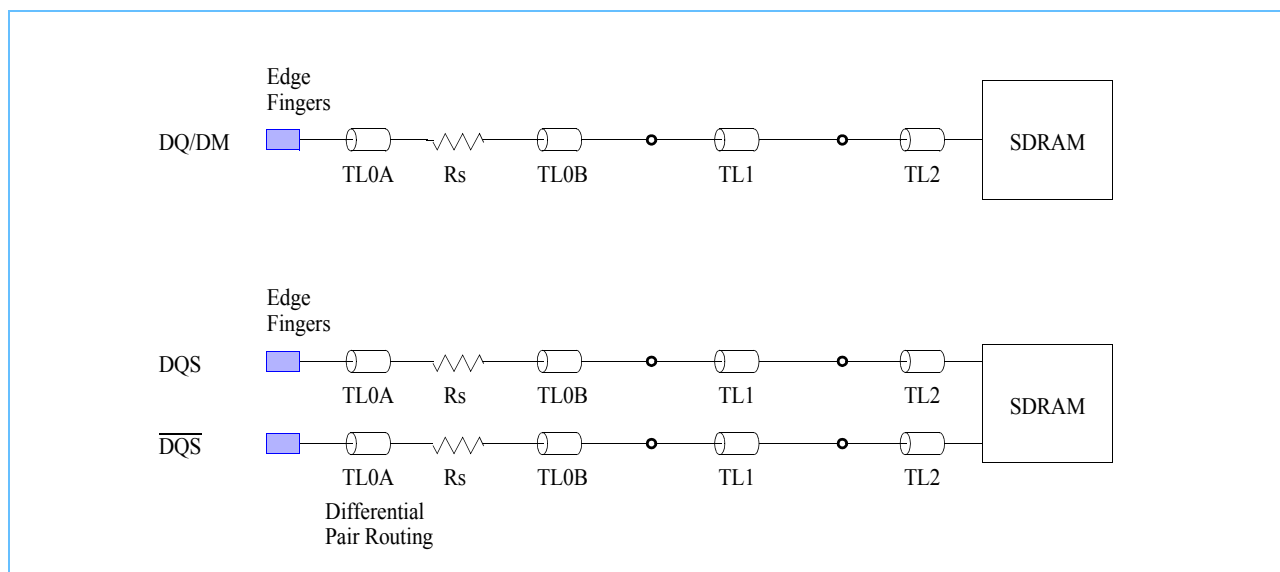
Figure 36 — Net Structure Routing for Address and Command (Raw Card Version F)

Table 32 — Trace Lengths for Address and Command Net Structures
(Raw Card Version F)

Length (mm)	TL0A	TL0B	TL1	TL2	TL3	TL4	TL5	TL6	TL7	First DRAM Compensated ²	Last DRAM Compensated ³	R _{TT}
	MS	MS	SL	MS	SL	SL	SL	SL	MS			
MIN	8.7	0.0	9.8	2.0	19.6	67.8	19.6	13.3	0.7	113.0	220.0	39Ω
MAX	111.5	0.0	102.6	2.8	19.6	67.8	19.6	13.8	1.3	113.0	220.0	39Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to first DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.
3. Equivalent stripline length to last DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1 + TL3 + TL4 + TL5]$.
4. A15 is not routed.

6.7 Net Structure Routing for Data



**Figure 37 — Net Structure Routing for Data (Raw Card Version A)
DQ/DM and DQS/DQS**

**Table 33 — Trace Lengths for Data Net Structures (Raw Card Version A)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS0}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	1.0	9.5	0.5	16.8	15Ω
MAX	3.2	1.6	12.6	1.1	16.8	15Ω
DQ8–DQ15, DM1, DQS1, $\overline{DQS1}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	0.9	12.2	0.5	19.8	15Ω
MAX	3.2	1.9	15.6	1.0	19.8	15Ω
DQ16–DQ23, DM2, DQS2, $\overline{DQS2}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.9	15.8	0.5	23.2	15Ω
MAX	3.2	1.8	19.2	1.1	23.2	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

**Table 33 — Trace Lengths for Data Net Structures (Raw Card Version A)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	1.1	20.8	0.5	28.1	15Ω
MAX	3.2	2.0	23.4	0.6	28.1	15Ω

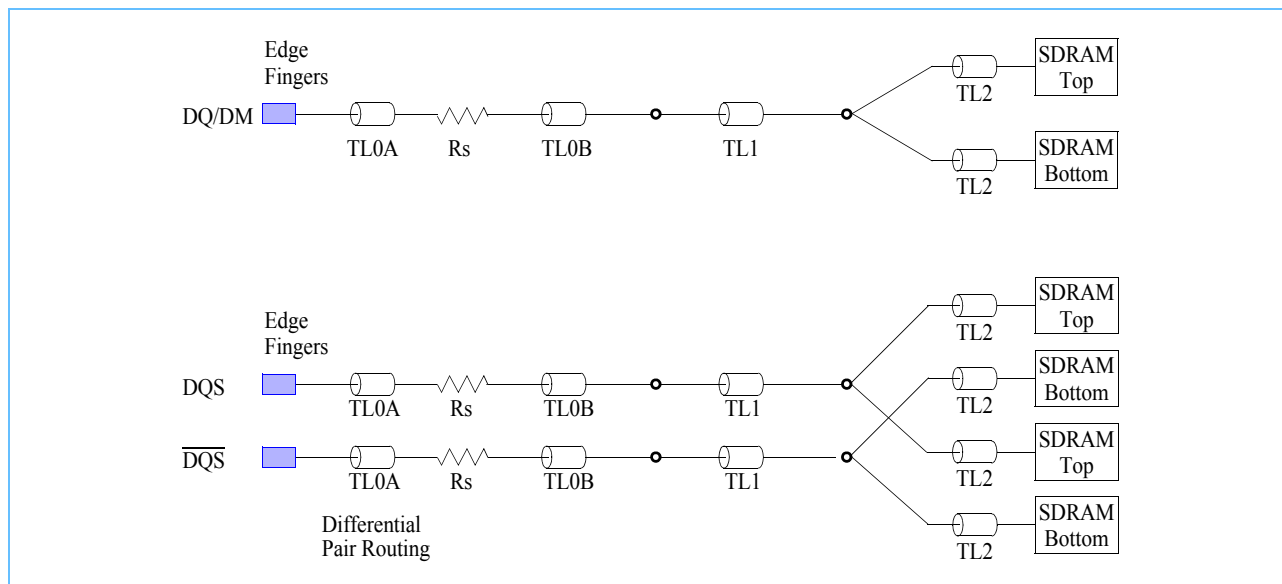
DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.9	19.2	0.5	26.7	15Ω
MAX	3.2	1.9	22.5	1.0	26.7	15Ω

DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	0.9	14.8	0.5	22.1	15Ω
MAX	3.2	2.0	17.9	1.0	22.1	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	1.0	11.1	0.5	18.5	15Ω
MAX	3.2	1.6	14.3	1.1	18.5	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.0	0.9	9.5	0.5	16.9	15Ω
MAX	3.2	1.6	12.7	1.0	16.9	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.



**Figure 38 — Net Structure Routing for Data (Raw Card Version B)
DQ/DM and DQS/DQS**

**Table 34 — Trace Lengths for Data Net Structures (Raw Card Version B)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS0}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	10.2	0.6	16.0	15Ω
MAX	3.9	1.7	11.9	1.8	16.1	15Ω

DQ8–DQ15, DM1, DQS1, $\overline{DQS1}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	13.5	0.6	19.3	15Ω
MAX	3.9	1.7	15.0	1.8	19.4	15Ω

DQ16–DQ23, DM2, DQS2, $\overline{DQS2}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	19.4	0.6	25.2	15Ω
MAX	3.9	1.7	20.9	1.8	25.3	15Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.

**Table 34 — Trace Lengths for Data Net Structures (Raw Card Version B)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	25.1	0.6	30.9	15Ω
MAX	3.9	1.7	26.7	1.8	31.0	15Ω

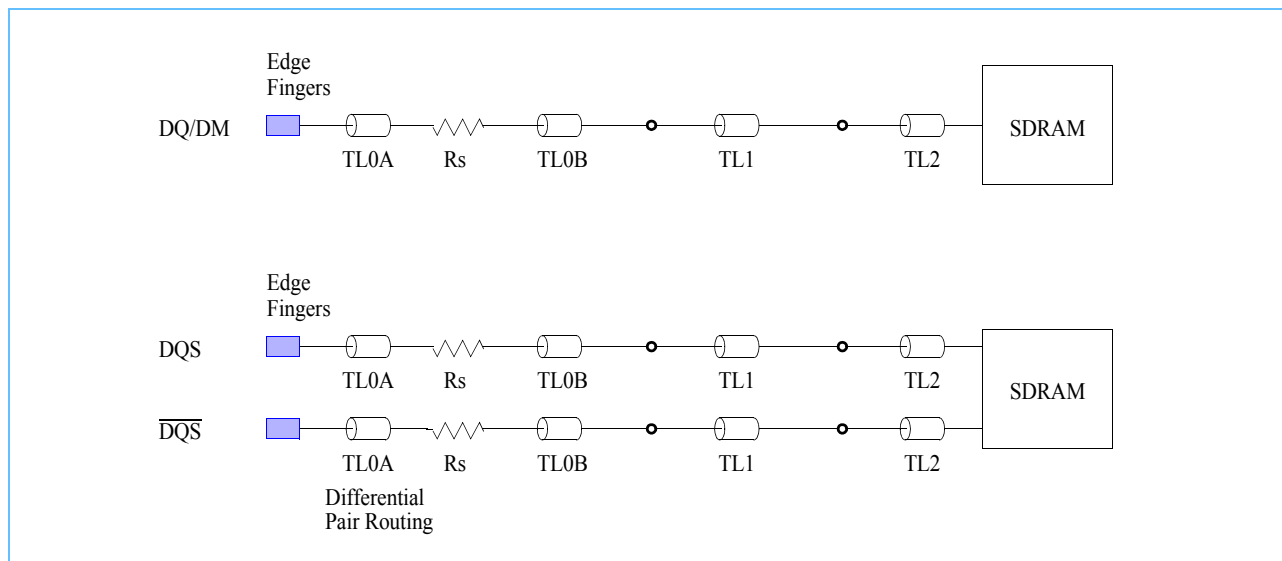
DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.7	23.2	0.6	29.0	15Ω
MAX	3.9	1.7	25.0	1.8	29.1	15Ω

DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	17.3	0.6	23.1	15Ω
MAX	3.9	1.7	18.9	1.8	23.2	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.3	0.7	11.6	0.6	17.4	15Ω
MAX	3.9	1.7	13.1	1.8	17.5	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	0.9	8.0	0.6	14.8	15Ω
MAX	3.9	1.7	10.9	1.8	15.1	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.



**Figure 39 — Net Structure Routing for Data (Raw Card Version C)
DQ/DM and DQS/DQS**

**Table 35 — Trace Lengths for Data Net Structures (Raw Card Version C)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS0}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ8–DQ15, DM1, DQS1, $\overline{DQS1}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

DQ16–DQ23, DM2, DQS2, $\overline{DQS2}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

**Table 35 — Trace Lengths for Data Net Structures (Raw Card Version C)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

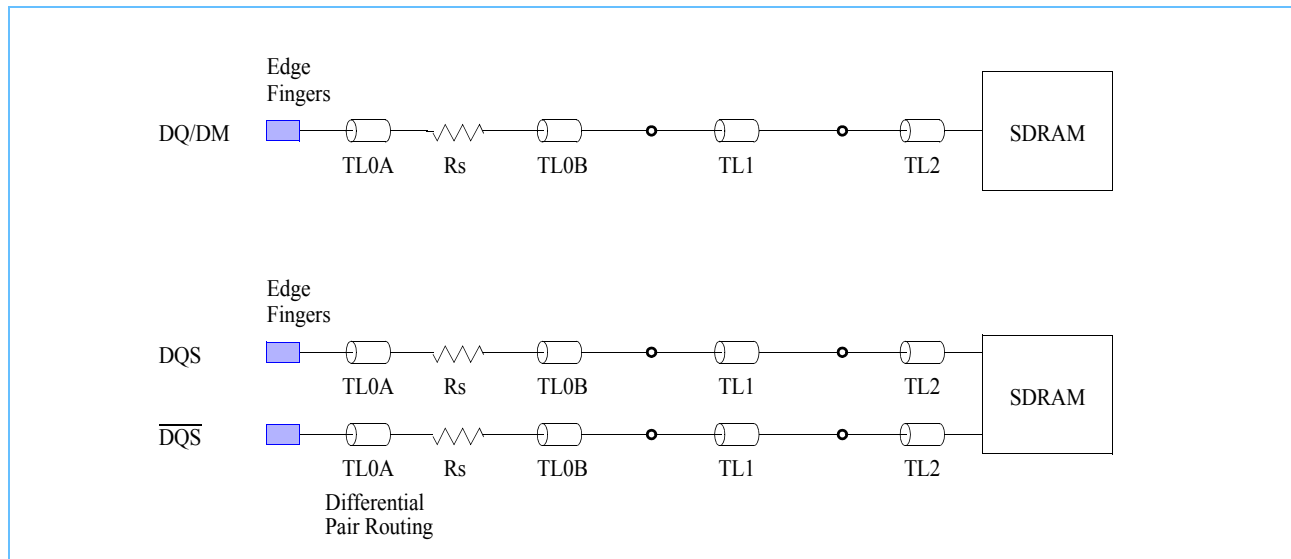
DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.3	0.6	19.2	15Ω
MAX	1.9	3.5	14.8	0.6	19.5	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	0.0	1.4	12.4	0.6	19.8	15Ω
MAX	1.9	3.5	15.8	0.6	20.2	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.



**Figure 40 — Net Structure Routing for Data (Raw Card Version D)
DQ/DM and DQS/DQS**

**Table 36 — Trace Lengths for Data Net Structures (Raw Card Version D)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS0}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	11.4	0.5	17.4	15Ω
MAX	3.9	1.5	13.3	1.9	17.5	15Ω

DQ8–DQ15, DM1, DQS1, $\overline{DQS1}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	13.5	0.5	19.4	15Ω
MAX	3.3	1.5	15.6	1.9	19.6	15Ω

DQ16–DQ23, DM2, DQS2, $\overline{DQS2}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	17.0	0.5	23.0	15Ω
MAX	3.3	1.5	19.1	1.9	23.1	15Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to DRAM [TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1].

**Table 36 — Trace Lengths for Data Net Structures (Raw Card Version D)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	20.7	0.5	26.7	15Ω
MAX	3.5	1.5	22.8	1.9	26.8	15Ω

DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	20.8	0.5	26.7	15Ω
MAX	4.4	1.8	22.9	1.9	26.9	15Ω

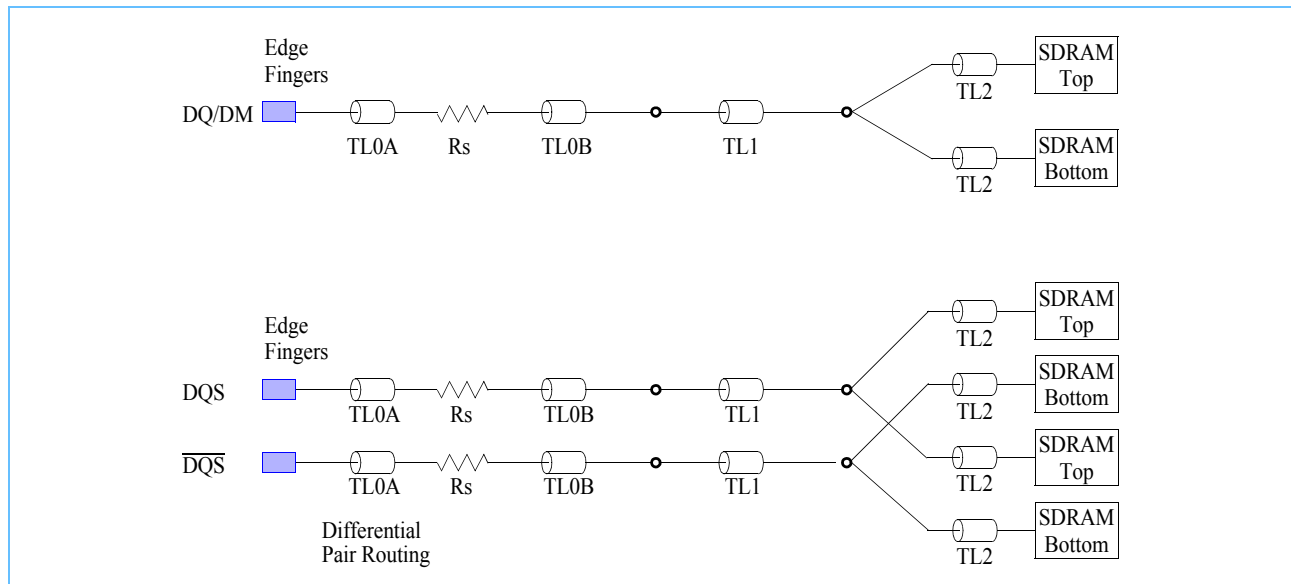
DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	17.0	0.5	23.0	15Ω
MAX	4.4	1.7	19.0	1.9	23.1	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	13.3	0.5	19.4	15Ω
MAX	4.4	2.8	15.6	1.9	19.6	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.8	11.5	0.5	17.4	15Ω
MAX	4.4	1.8	13.5	1.9	17.5	15Ω

CB0–DQ7, DM8, DQS8, $\overline{DQS8}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	24.4	0.5	30.4	15Ω
MAX	3.6	1.5	26.4	1.9	30.5	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.



**Figure 41 — Net Structure Routing for Data (Raw Card Version E)
DQ/DM and DQS/DQS**

**Table 37 — Trace Lengths for Data Net Structures (Raw Card Version E)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS0}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	11.4	0.5	17.3	15Ω
MAX	4.2	1.6	13.4	1.9	17.4	15Ω

DQ8–DQ15, DM1, DQS1, $\overline{DQS1}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	13.5	0.5	19.3	15Ω
MAX	3.3	1.5	15.5	1.9	19.5	15Ω

DQ16–DQ23, DM2, DQS2, $\overline{DQS2}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	17.0	0.5	22.9	15Ω
MAX	3.2	1.4	19.0	1.9	23.0	15Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.

**Table 37 — Trace Lengths for Data Net Structures (Raw Card Version E)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	20.8	0.5	26.6	15Ω
MAX	3.4	1.7	22.7	1.9	26.8	15Ω

DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	20.6	0.5	26.6	15Ω
MAX	4.3	1.5	22.8	1.9	26.8	15Ω

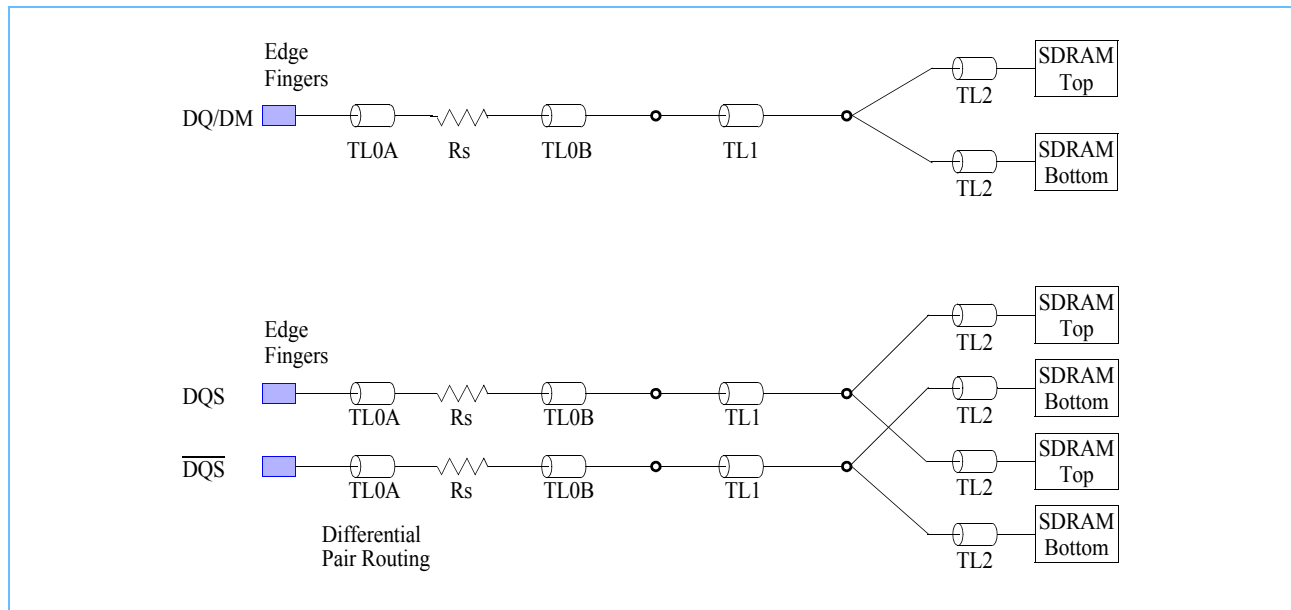
DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	16.9	0.5	22.9	15Ω
MAX	4.3	1.7	18.9	1.9	23.0	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	13.3	0.5	19.3	15Ω
MAX	4.3	1.8	15.5	1.9	19.5	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.7	11.2	0.5	17.3	15Ω
MAX	4.3	1.8	13.4	1.9	17.4	15Ω

CB0–CB7, DM8, DQS8, $\overline{DQS8}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	2.9	0.6	24.4	0.5	30.4	15Ω
MAX	3.6	1.5	26.4	1.9	30.5	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.



**Figure 42 — Net Structure Routing for Data (Raw Card Version F)
DQ/DM and DQS/DQS**

**Table 38 — Trace Lengths for Data Net Structures (Raw Card Version F)
DQ/DM and DQS/DQS**

DQ0–DQ7, DM0, DQS0, $\overline{DQS}0$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ8–DQ15, DM1, DQS1, $\overline{DQS}1$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ16–DQ23, DM2, DQS2, $\overline{DQS}2$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

- Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
- Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.

**Table 38 — Trace Lengths for Data Net Structures (Raw Card Version F)
DQ/DM and DQS/DQS (Cont'd)**

DQ24–DQ31, DM3, DQS3, $\overline{DQS3}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ32–DQ39, DM4, DQS4, $\overline{DQS4}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ40–DQ47, DM5, DQS5, $\overline{DQS5}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

DQ48–DQ55, DM6, DQS6, $\overline{DQS6}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.3	0.6	19.2	15Ω
MAX	3.5	1.9	14.8	0.6	19.5	15Ω

DQ56–DQ63, DM7, DQS7, $\overline{DQS7}$						
Length (mm)	TL0A	TL0B	TL1	TL2	DRAM Compensated ²	Rs
	MS	MS	SL	MS		
MIN	3.1	1.0	12.4	0.6	19.8	15Ω
MAX	3.8	1.8	15.8	0.6	20.2	15Ω

1. Columns which represent the sum of the other columns are expressed in equivalent stripline lengths with the conversion factor of 1.1 mm of microstrip = 1.0 mm of stripline.
2. Equivalent stripline length to DRAM $[TL0A/1.1 + TL0B/1.1 + TL1 + TL2/1.1]$.

6.8 Cross Section Recommendations

DIMM printed circuit board designs (Raw Cards A, B, C, D, and F) use six-layers of glass epoxy material. Raw Card E uses an eight-layer PCB.

Table 39 — Six-Layer Geometry and Impedance Targets

Layer	Single-Ended		Differential	
	Width	Target Z ₀	Width/Space	Target Z _{DIFF}
L1	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
L3	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
L4	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
	0.17 mm	49Ω ±15% ²		
L6	0.1 mm	60Ω ±10%	0.1 mm/0.1 mm	88Ω ±15%
	0.25 mm	40Ω ±15%	0.25 mm/0.1 mm	62Ω ±15%
	0.17 mm	49Ω ±15% ²		

1. All impedances other than the basic single-ended 60 ohms target are provided for reference only.
2. Due to the light load on Raw Card C (1 rank x 16), the impedance of the traces through the DRAM area is 49 ohms rather than 60 ohms.
3. Due to the light load on Raw Cards A, C, and D (1 rank), the impedance of the command and address traces through the DRAM area is 49 ohms rather than 60 ohms.

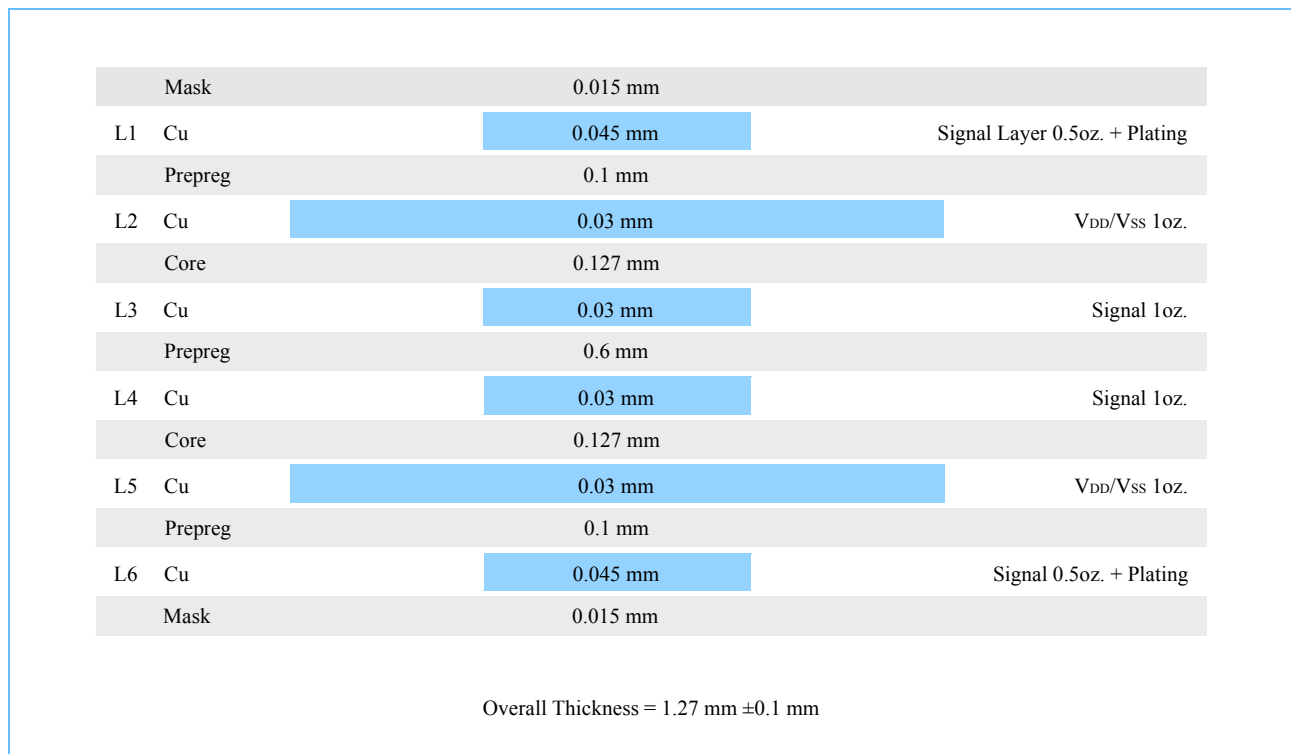


Figure 43 — Six-Layer Stackup (Example)

Table 40 — Eight-Layer Geometry and Impedance Targets

Layer	Single-Ended		Differential	
	Width	Target Z_0	Width/Space	Target Z_{DIFF}
L1	0.0825 mm	60Ω ±10%	0.0825 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L3	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L6	0.075 mm	60Ω ±10%	0.075 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%
L8	0.0825 mm	60Ω ±10%	0.0825 mm/0.1 mm	88Ω ±15%
	0.2 mm	40Ω ±15%	0.2 mm/0.1 mm	62Ω ±15%

1. All impedances other than the basic single-ended 60Ω target are provided for reference only.

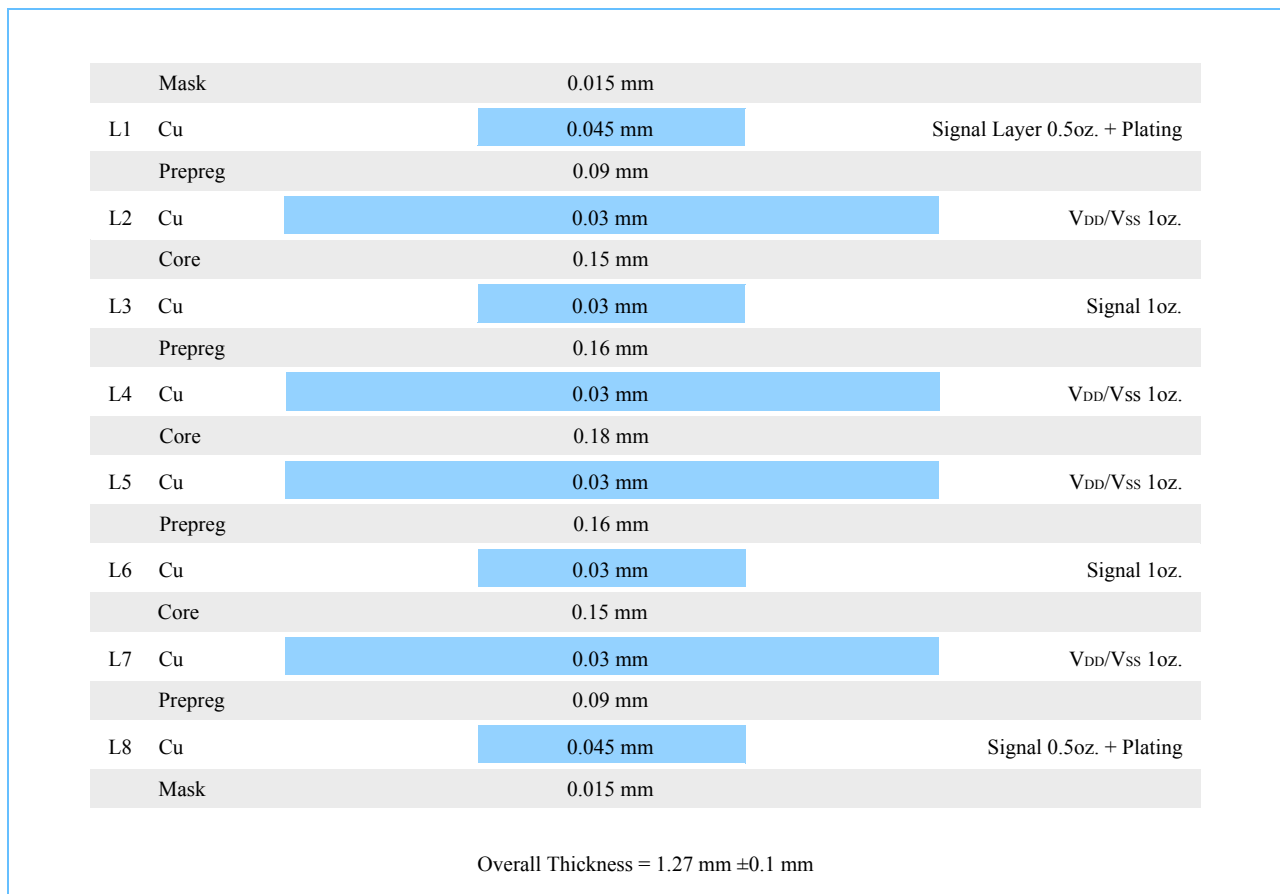


Figure 44 — Eight-Layer Stackup (Example)

6.9 Test Point Identification

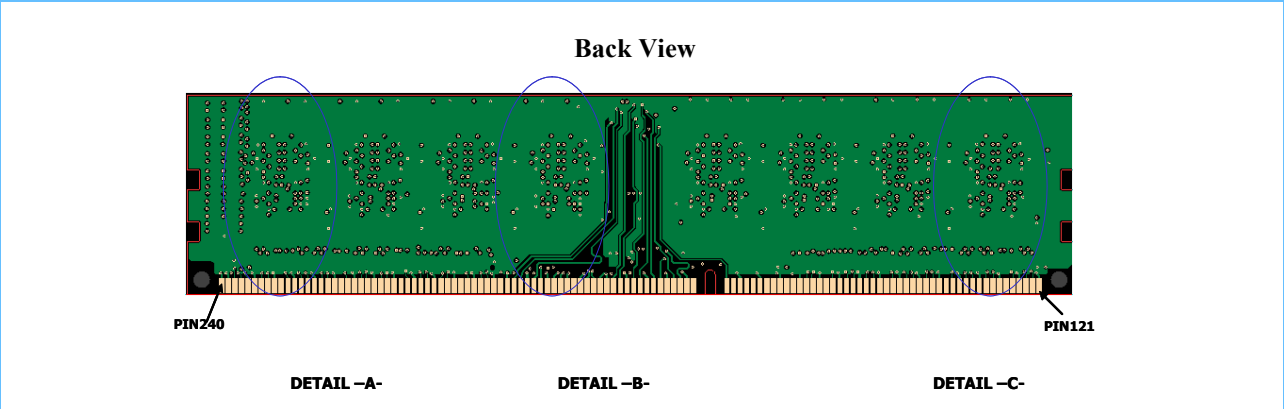


Figure 45 — Test Point Identification (Raw Card Version A): Back View

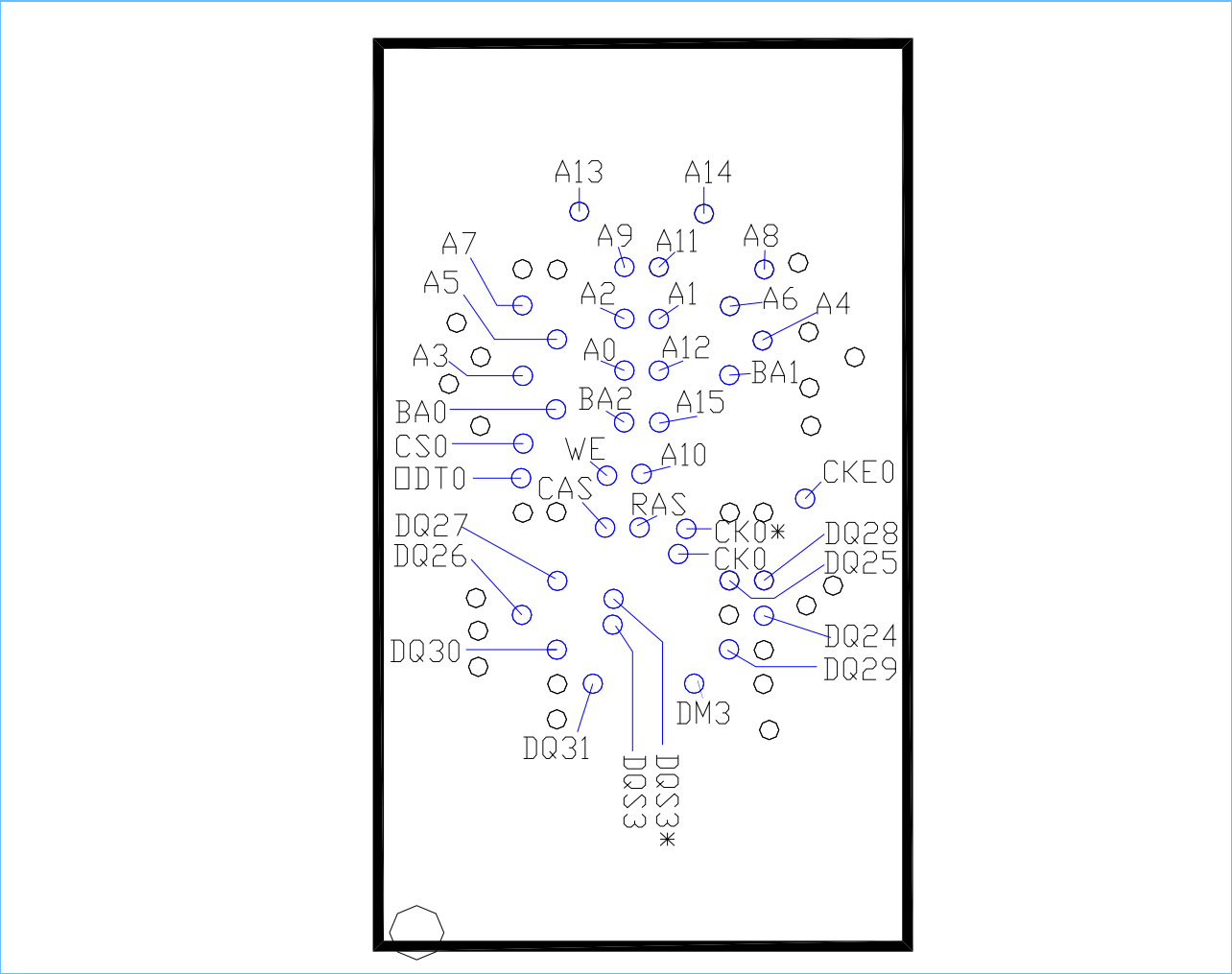


Figure 46 — Test Point Identification (Raw Card Version A): Bottom View

Raw Card B has DRAMs on either side of the module. All vias under the DRAM are not accessible. The points identified below are at via locations which are not under the DRAM and are not at optimal locations for determining timing or signal integrity at the DRAMs.

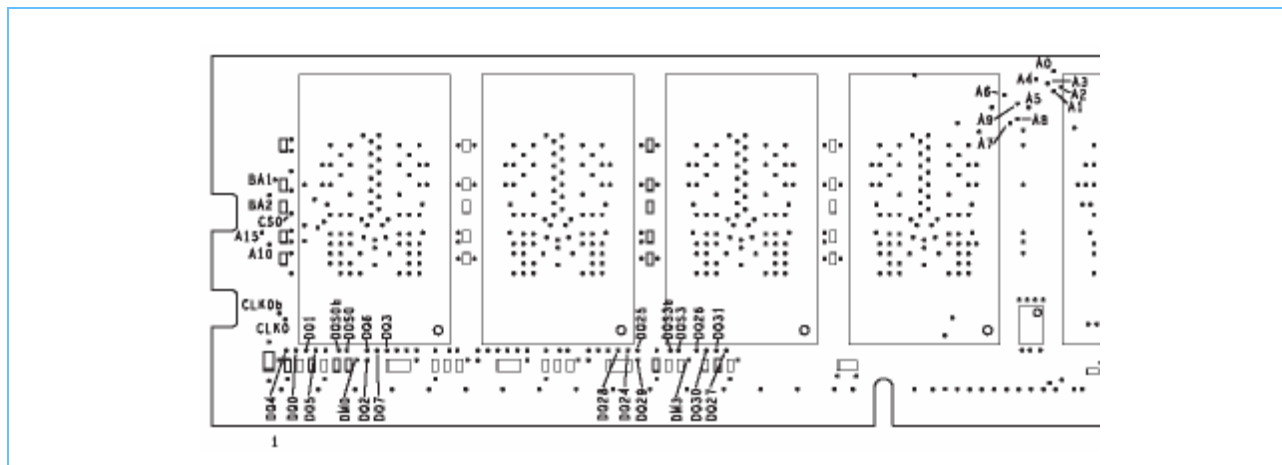


Figure 47 — Test Point Identification (Raw Card Version B): Front View, Left Side

Vias are located just before the first DRAM on the left side of the module. The location of the vias may provide a good indication of signaling at the first DRAM. The DQ and DQS signals can be measured at the via just after the stub resistor. This can be used for timing, but the signal at the DRAM will usually have better signal integrity. The address signals near the middle of the module are in the lead-in section. They will not be a good indicator of module performance.

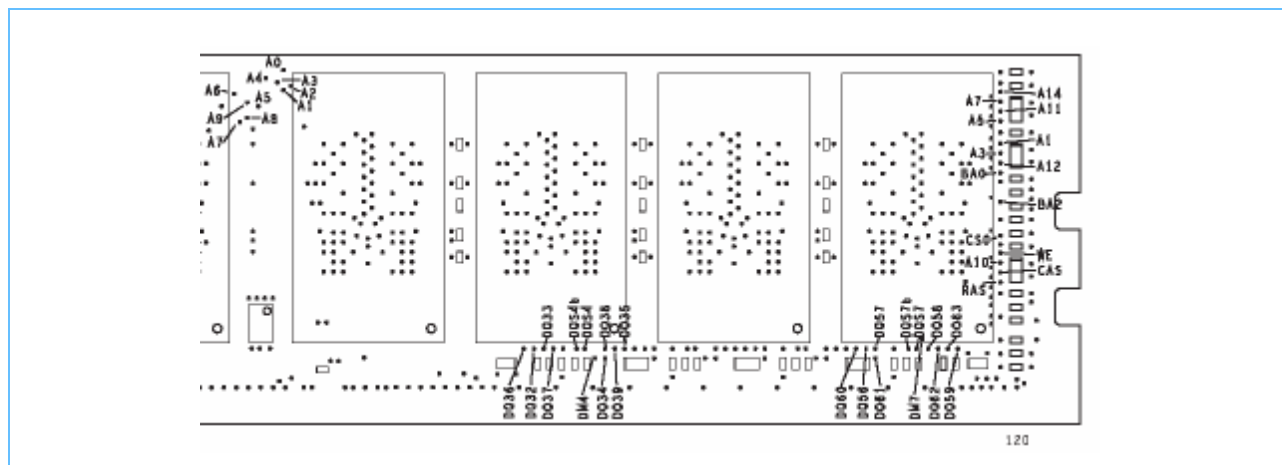


Figure 48 — Test Point Identification (Raw Card Version B): Front View, Right Side

The termination resistor on the right side of the module will provide some indication of signal integrity and timing at the last DRAM.

Raw Card C test points can be found in three locations: on the vias, on the termination resistors, and within the DQ group. First, because Raw Card C is a single-sided module, all test point vias can be accessed on the backside of the module, 2.5 mm from the edge of the DRAM pin (Figure 49 shows the via grid under each DRAM). This grid allows access to all command, address, control, and clock signals near the DRAM pins. After scraping through the soldermask, a ground plane can be connected to the ground side of the probe on the backside of the module.

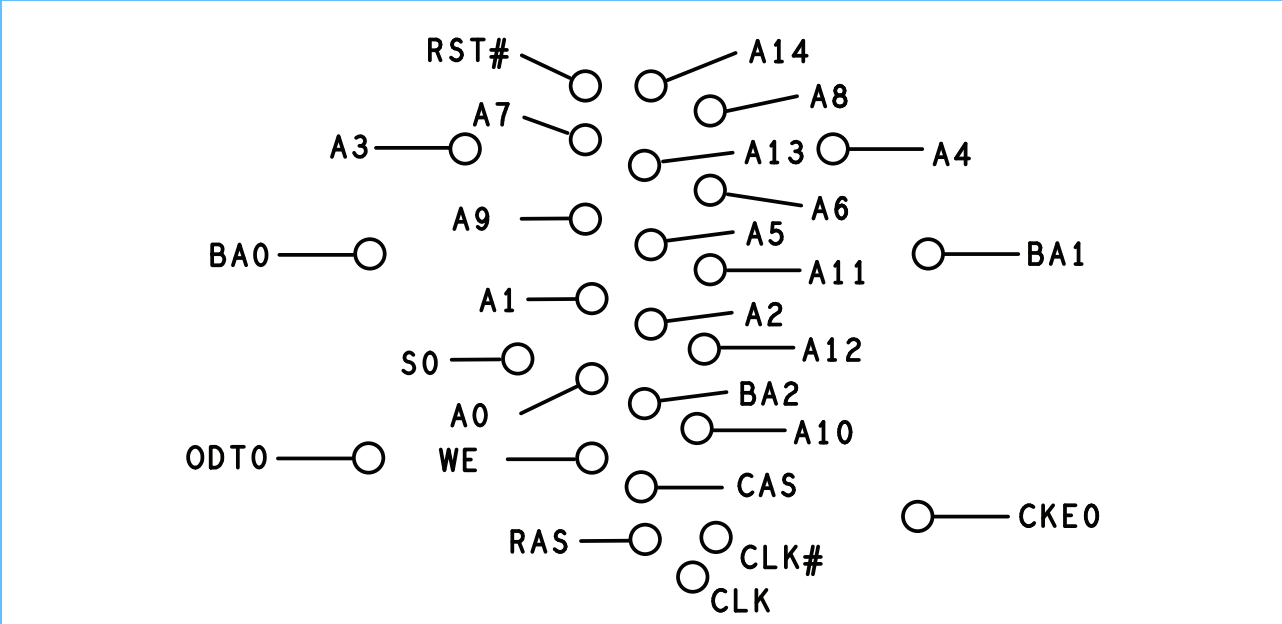


Figure 49 — Test Point Identification (Raw Card C): Backside View
The Address and Command, Control, and Clock Structure Pins

A map of the termination resistor signal assignments, shown in Figure 50, shows how test points can also be accessed on the component side of the module. The component side of the module consists of two planes: the V_{TT} rail plane—which is located to the right of the termination resistors—and the ground plane. Note: picking up a good ground point for the resistor in the right column may be difficult to do because the capacitors in this area are connected between V_{TT} and V_{DD} only.

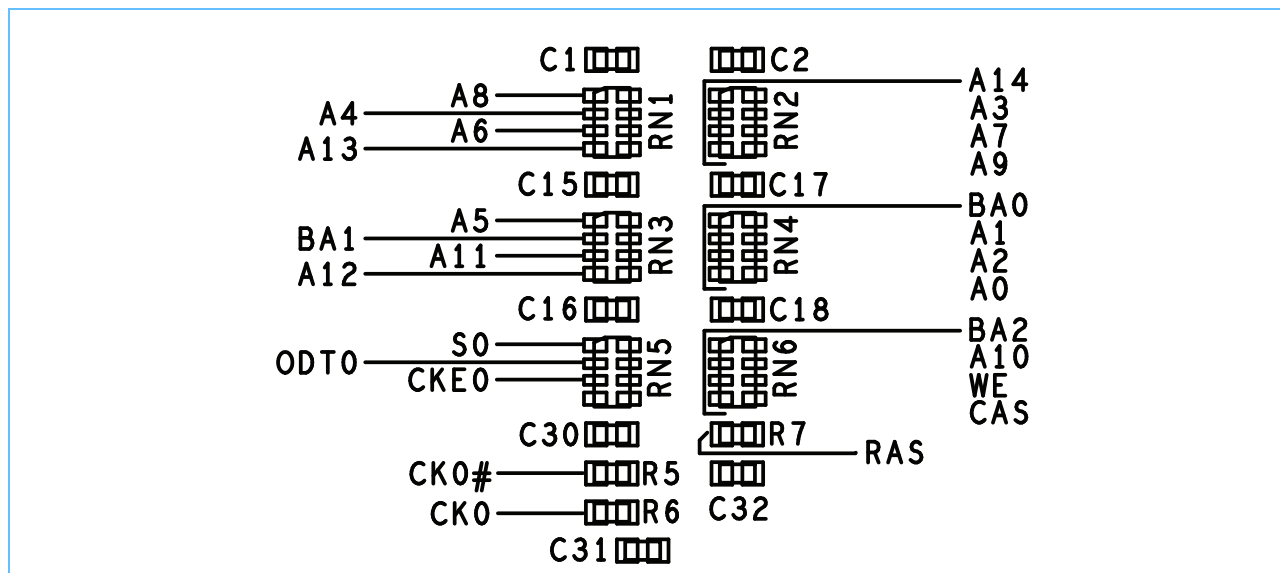


Figure 50 — Raw Card C Test Points (Raw Card C): The Termination Resistors

Finally, test points can be found on the DQ group. Figure 51 illustrates the location of the DQ test point vias located 0.6 mm from the edge of the DRAM pin (vias not shown are used for power and ground points). After scraping through the solder mask, a ground plane can be used to connect to the ground side of the probe on the backside of the module. Figure 51 references the signals for the first two byte groups (DQ0–DQ16 or DQ32 or DQ48), add increments of 16 to each subsequent reference designator.

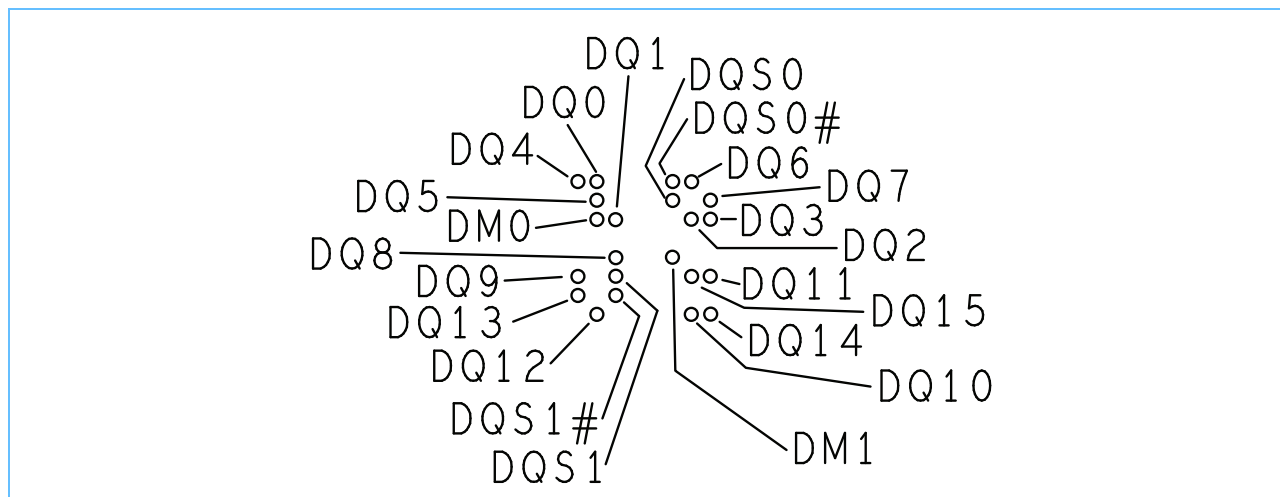


Figure 51 — Test Point Identification (Raw Card C): Backside View, The DQ Group

Raw Card D DRAMs exist only on the front side of the module. This allows access to the vias under the DRAMs from the back side. Some probe points are also available on the front side of the module (see Figures 52 and 53).

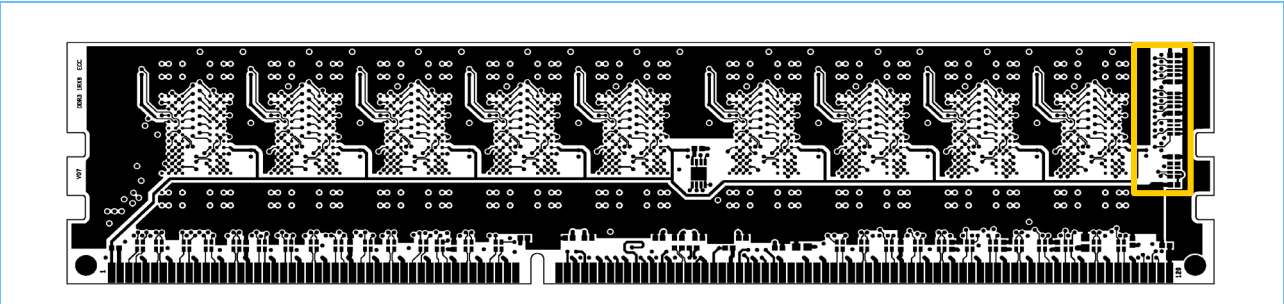


Figure 52 — Test Point Identification (Raw Card Version D): Front Side, Full Board View

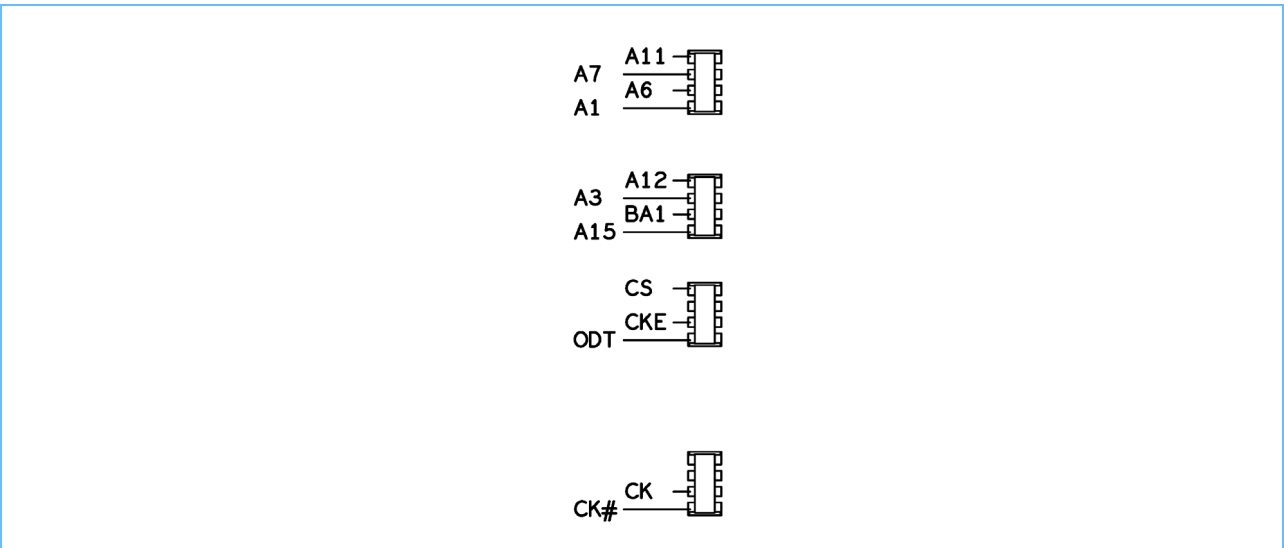


Figure 53 — Test Point Identification (Raw Card Version D): Front Side, Detailed View

Most of the test points of interest reside on the back side of the module. Figures 54–57 detail the locations of these test points.

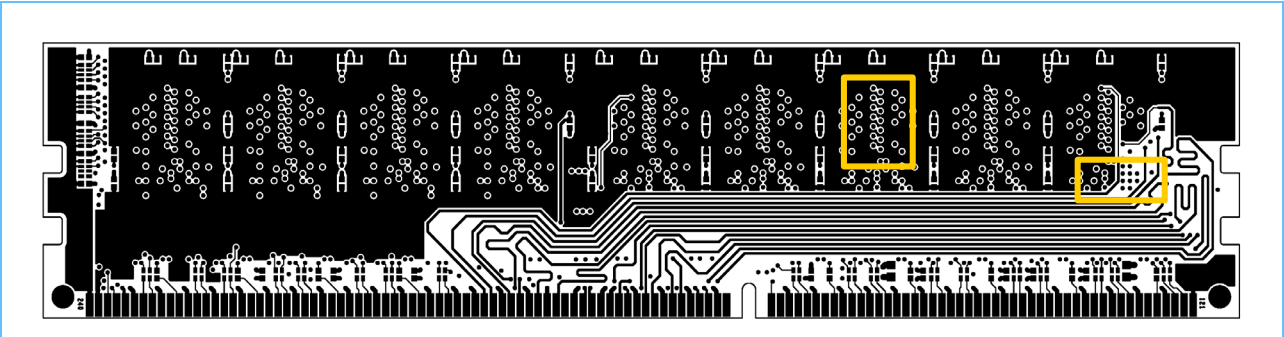


Figure 54 — Test Point Identification (Raw Card Version D): Back Side, Full Board View

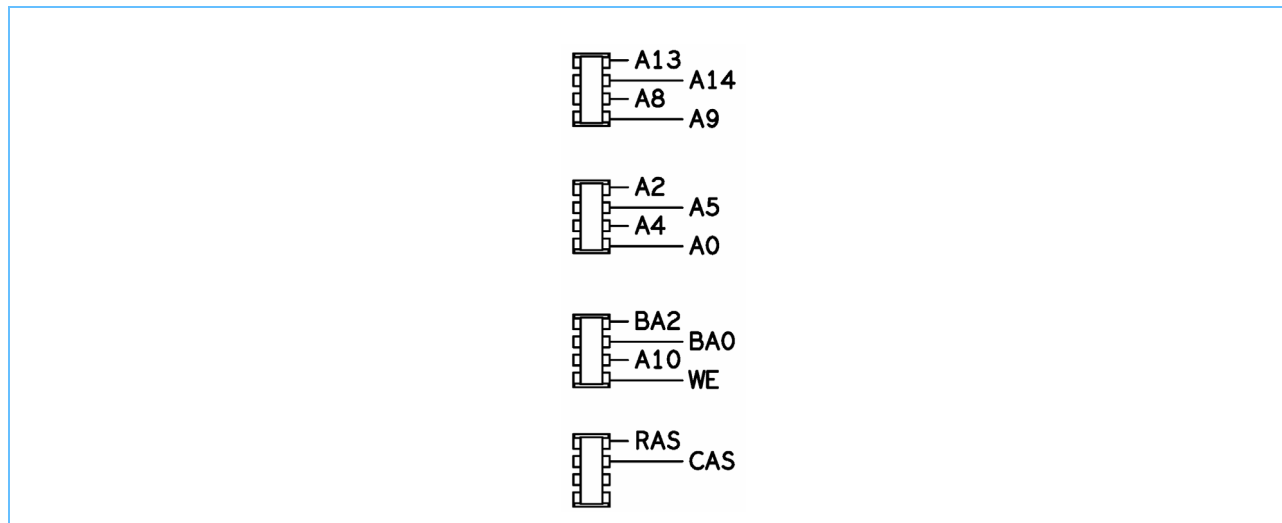


Figure 55 — Test Point Identification (Raw Card Version D): Back Side View Test Point Area at the Terminations

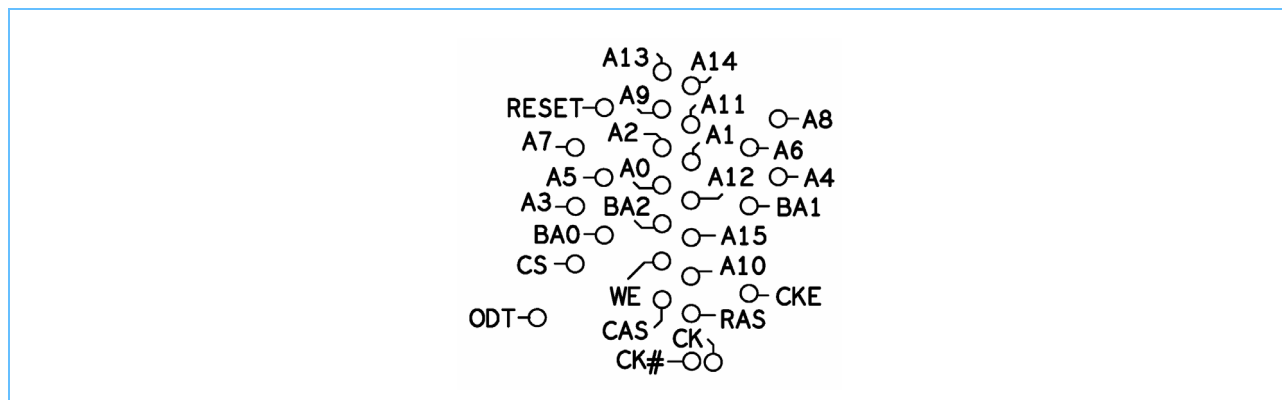


Figure 56 — Test Point Identification (Raw Card Version D): Back Side View Test Point Area Under the DRAMs

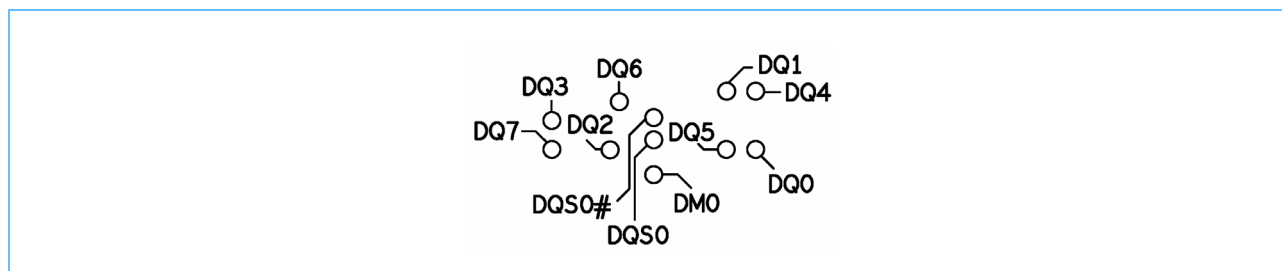


Figure 57 — Test Point Identification (Raw Card Version D): Back Side View Termination Area at the First DRAM

The detail for the via pattern behind the DRAM is valid for all DRAM locations.

Raw Card E contains DRAMs on either side of the module, which limits the availability of test points. The available test points accessible from the front side of the module are detailed in Figures 58–61.

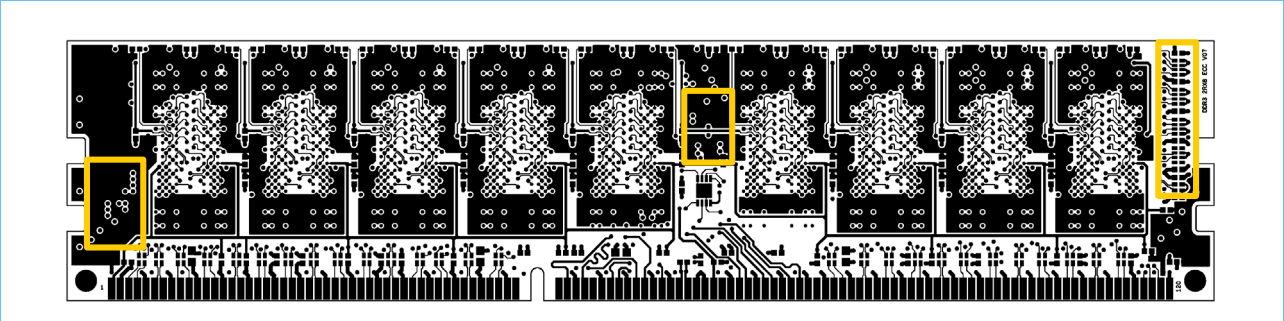


Figure 58 — Test Point Identification (Raw Card Version E): Front Side View, Full Board

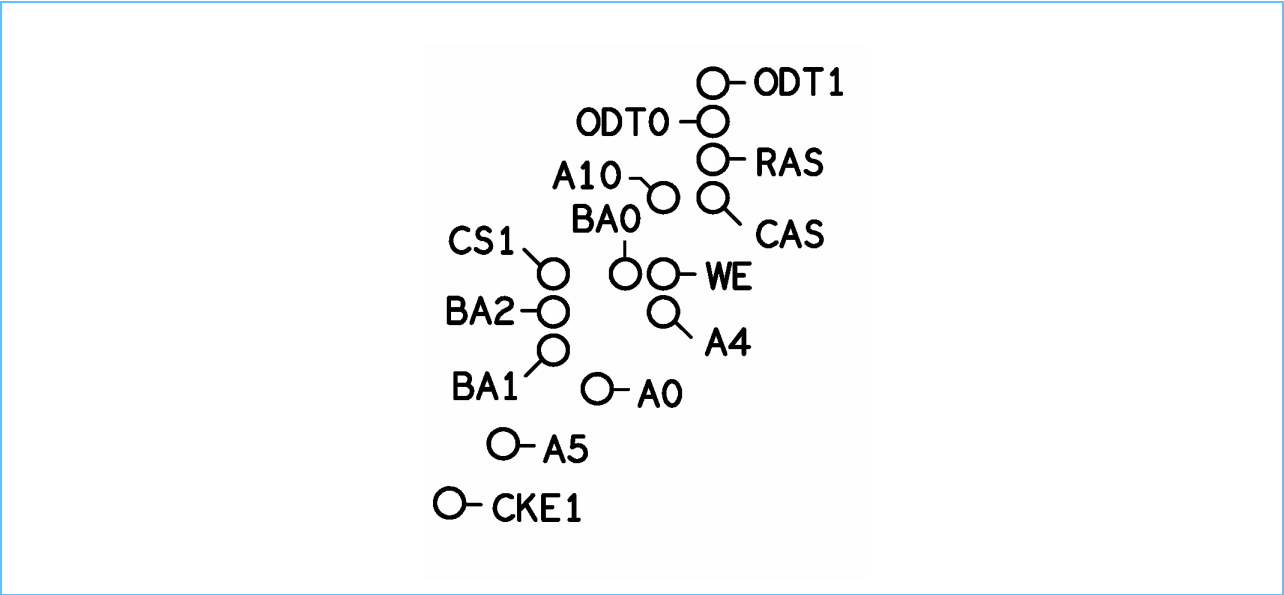


Figure 59 — Test Point Identification (Raw Card Version E): Front Side View, Test Points Near the First DRAM

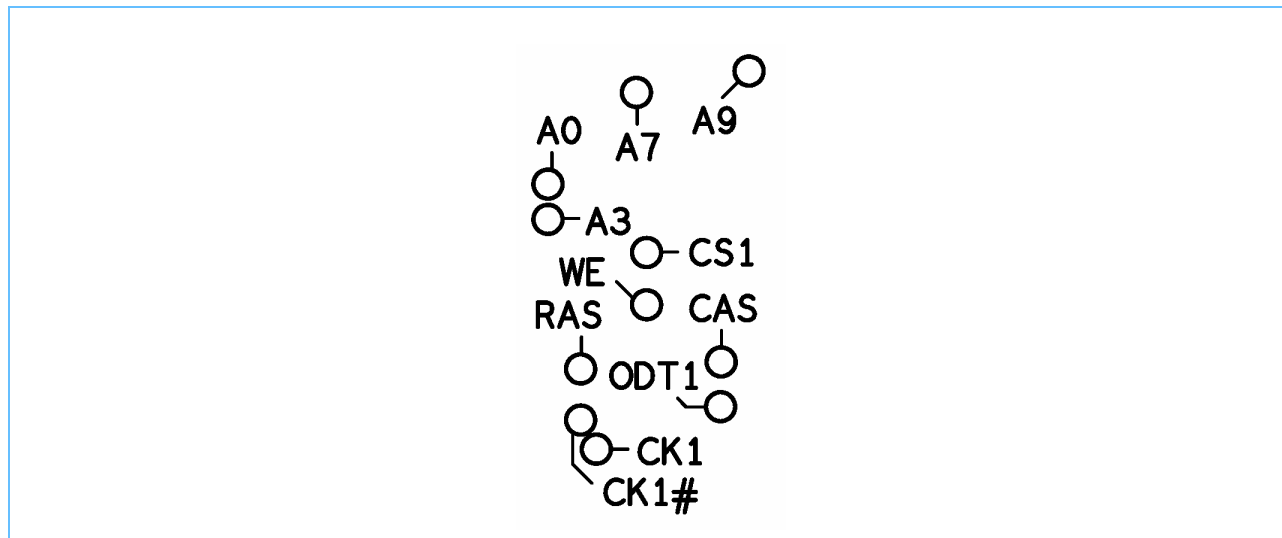


Figure 60 — Test Point Identification (Raw Card Version E): Front Side View
Test Points Between the Fifth and Sixth DRAM Sites

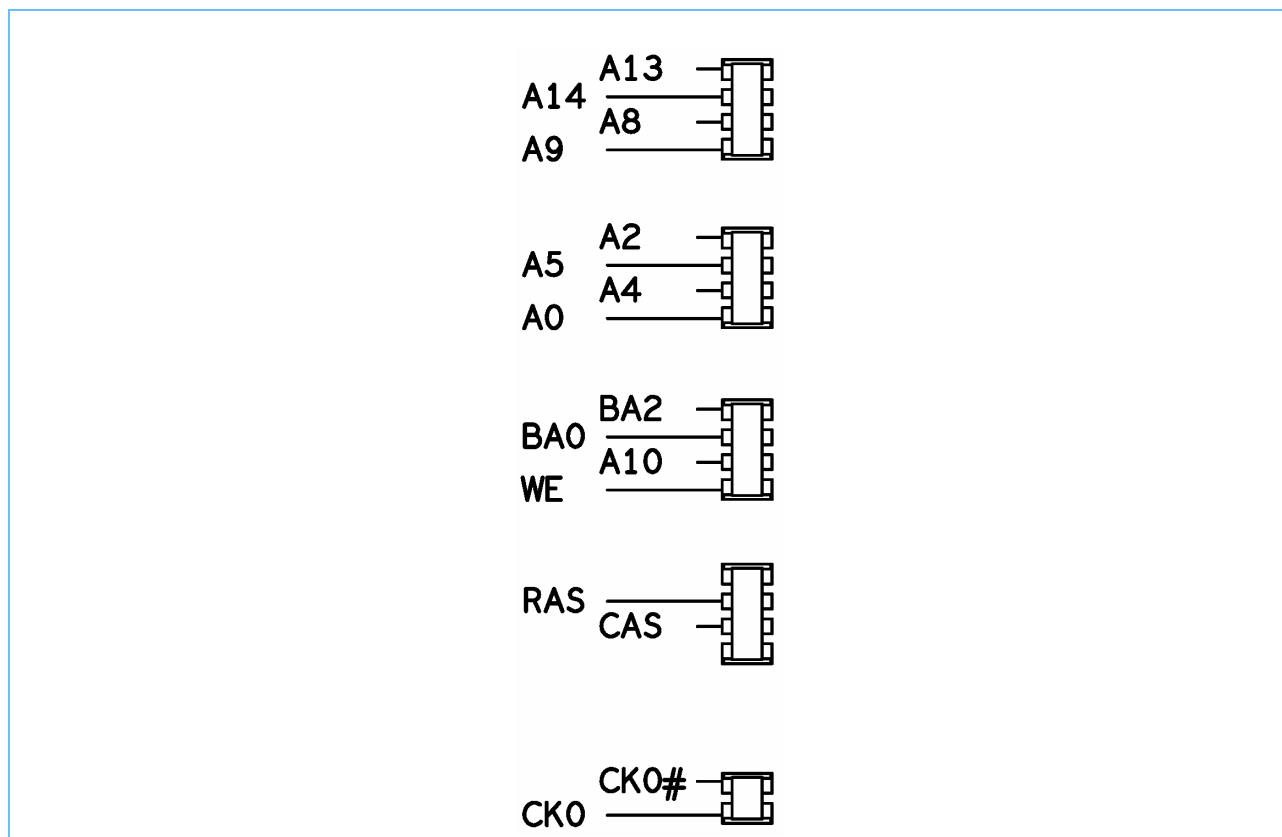


Figure 61 — Test Point Identification (Raw Card Version E): Front Side View
Test Points at the Terminations

Raw Card F is a two-sided module which prevents convenient access to test points. Other via locations can also be used (these will be identified) but they are further away from the DRAM pins. Additional vias have been added to provide additional test points. This compromises the timing, but availability of the test points is considered important enough that this trade-off has been made. Figure 62 shows the location of the test points on the left side of the module (not all test points will be available when a large DRAM is installed). Figure 63 shows the location of the test points for the right side of the module.

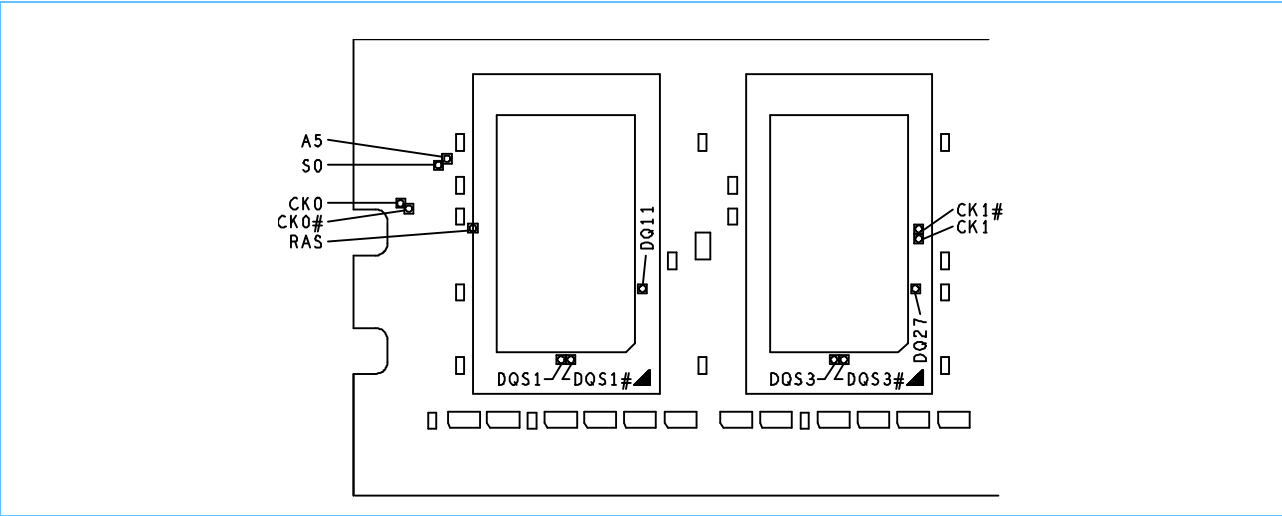


Figure 62 — Test Point Identification (Raw Card Version F): Front, Left Side View

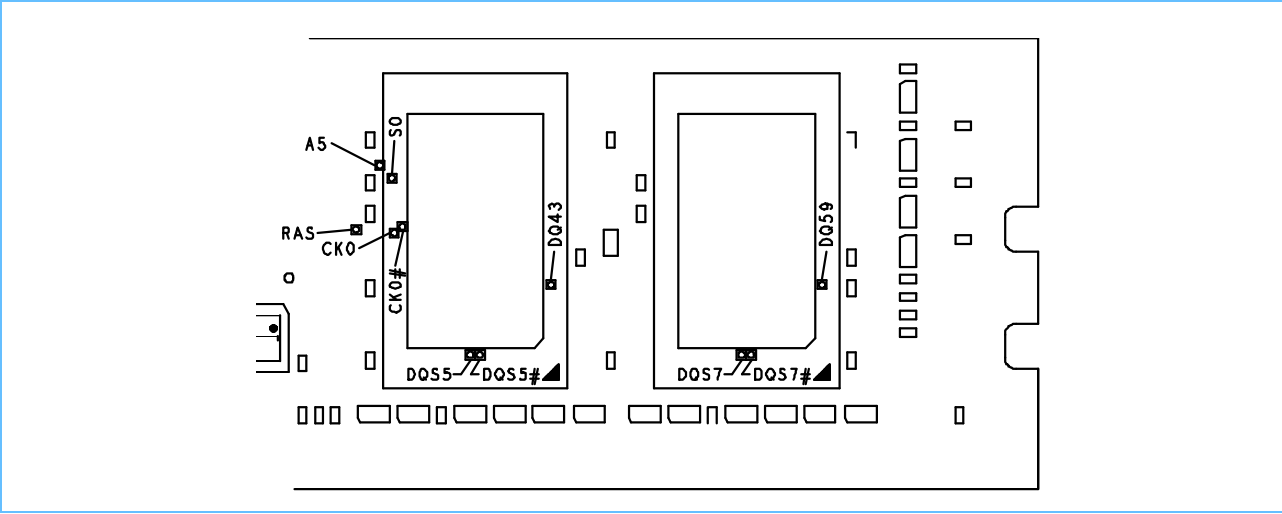


Figure 63 — Test Point Identification (Raw Card Version F): Front, Right Side View

Termination resistors also provide a good point to access the signals. Maps of these signal assignments are shown in Figures 64 and 65.

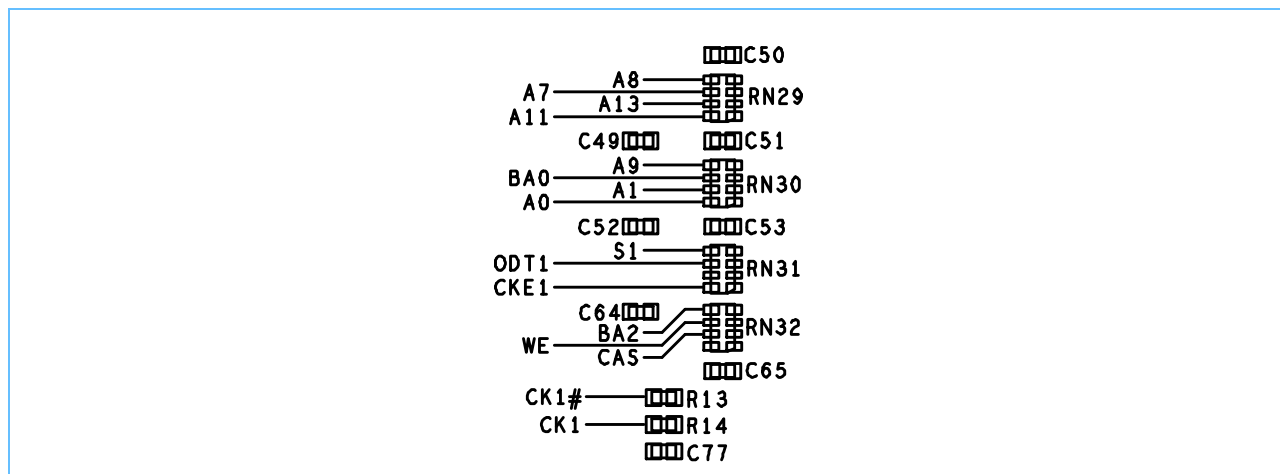


Figure 64 — Test Point Identification (Raw Card Version F): Front Side View Signal Locations at the Termination Resistors

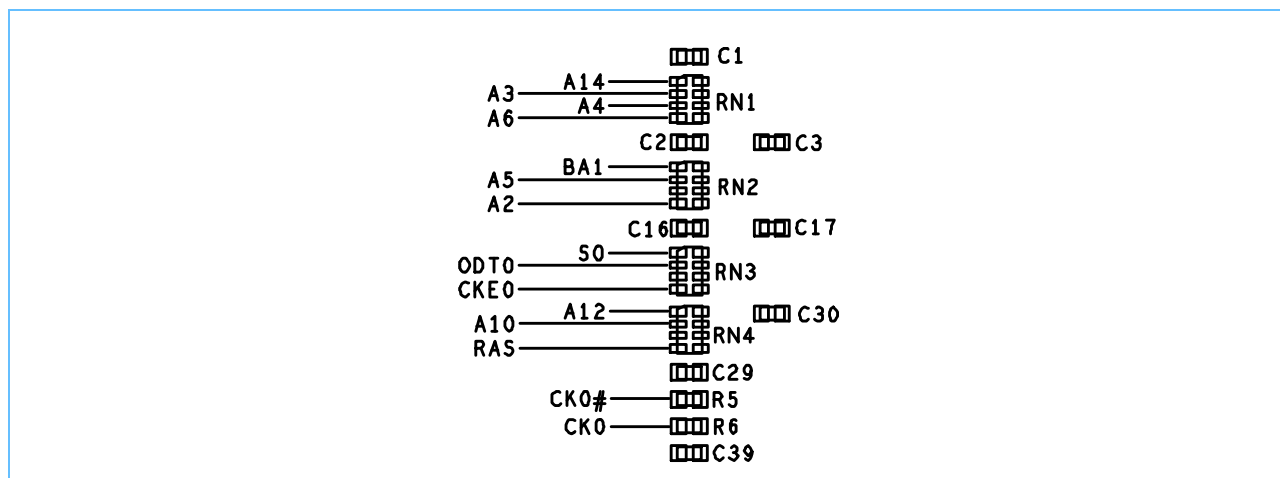


Figure 65 — Test Point Identification (Raw Card Version F): Back Side View Signal Locations at the Termination Resistors

Raw Card F has a ground plane on the outside layers. This will provide reasonable access to ground for the ground side of any probe. Use caution: there is a V_{TT} plane on the other side of the resistor networks. The decoupling capacitors are between the V_{TT} and V_{DD} and can not be used for probe ground.

7 Serial Presence Detect

7.1 Serial Presence Detect Component Specification

The contents of the lower 128 bytes (Bytes 0–127) of the SPD EEPROM must be software write protected by the DIMM vendor, using one of the two methods standardized by JEDEC JC-45: either the permanent software write protect method, or the reversible software write protect method.

7.2 Serial Presence Detect Definition

The Serial Presence Detect function MUST be implemented on the DDR3 SDRAM Unbuffered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR3 Module Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices.

The following table is intended to be an **example** of the SPD data for a PC3-8500, double-sided 2GB (2 x 128 Meg x 64) non-ECC, 240-pin unbuffered DDR3 SDRAM DIMM. This example shows a module comprised of sixteen 128 Meg x 8 DRAM components.

Table 41 — Serial Presence Detect, Example Raw Card Version B (Part 1 of 2)

Byte Number	Byte Attribute Description	SPD Entry Value	Hexadecimal Byte Value
0	CRC range, EEPROM bytes, bytes used	Bytes 0–116/256/176	92
1	SPD revision	Rev 0.0	00
2	DRAM device type	DDR3 SDRAM	0B
3	Module type (form factor)	UDIMM	02
4	SDRAM Device density and banks	1Gb, 8 banks	02
5	SDRAM device row and column count	14 rows, 10 columns	11
6	Byte 6 reserved	None	00
7	Module ranks and device DQ count	2 Ranks, x8 DQs	09
8	ECC tag and module memory Bus width	Non-ECC, 64-bit Bus	03
9	Fine timebase dividend/divisor (in pico seconds)	5/2 = 2.5ps	52
10	Medium timebase dividend	1ns	01
11	Medium timebase divisor	8ns	08
12	Minimum SDRAM cycle time (t_{CKMIN})	1.875ns	0F
13	Byte 13 reserved	None	00
14	CAS latencies supported (CL4 ≥ CL11)	CAS 8, 7, and 6	1C
15	CAS latencies supported (CL12 ≥ CL18)	None	00
16	Minimum CAS latency time ($t_{AA_{MIN}}$)	13.125ns	69
17	Minimum write recovery time ($t_{WR_{MIN}}$)	15ns	78
18	Minimum \overline{RAS} -to- \overline{CAS} delay ($t_{RCD_{MIN}}$)	13.125ns	69
19	Minimum row ACTIVE-to-ROW ACTIVE delay ($t_{RRD_{MIN}}$)	7.5ns	3C
20	Minimum row PRECHARGE delay ($t_{RP_{MIN}}$)	13.125ns	69
21	Upper nibble for t_{RAS} and t_{RC}	1(2C) and 1(A4)	11
22	Minimum ACTIVE-to-PRECHARGE delay ($t_{RAS_{MIN}}$)	0x12C = 37.5ns	2C

Table 41 — Serial Presence Detect, Example Raw Card Version B (Part 2 of 2)

Byte Number	Byte Attribute Description	SPD Entry Value	Hexadecimal Byte Value
23	Minimum ACTIVE-to-ACTIVE/REFRESH delay (⁴ RC _{MIN})	0x1A4 = 52.5ns	A4
24	Minimum refresh recovery delay (⁴ RFC _{MIN}) LSB	(combo bytes 24, 25)	70
25	Minimum refresh recovery delay (⁴ RFC _{MIN}) MSB	0x370=110ns ⁴ RFC _{MIN}	03
26	Minimum internal WRITE-TO-READ command delay (⁴ WTR _{MIN})	7.5ns	3C
27	Minimum internal READ-to-PRECHARGE command delay (⁴ RTP _{MIN})	7.5ns	3C
28	Minimum four active window delay (⁴ FAW _{MIN}) LSB	(combo bytes 28, 29)	01
29	Minimum four active window delay (⁴ FAW _{MIN}) MSB	0x12C = 37.5ns	2C
30	SDRAM device output drivers supported	RZQ/7 supported	02
31	SDRAM device thermal and refresh options	ASR, extended temperature	05
32–59	Bytes 32–59 reserved	None	00000000000000000000
60	Module height (NOMINAL)	30 mm	0F
61	Module thickness (MAX)	DR, 4 mm MAX	11
62	Raw card ID reference	Raw Card B	01
63	DRAM address mapping edge connector	Standard	00
64–116	Bytes 64–116 reserved	None	00000000000000000000
117	Module manufacturer ID (LSB)	Manufacturer specific	80
118	Module manufacturer ID (MSB)	Manufacturer specific	2C
119	Module manufacturer location ID	Variable data	00
120	Module manufacturer year	Variable data	00
121	Module manufacturer week	Variable data	00
122–125	Module serial number	Variable data	00000000
126–127	CRC	Calculated value	027B
128–145	Module part number	ASCII values	16JTF25664AY-1G1A1
146–147	Module revision code	Variable data	41
148	DRAM Device manufacturer ID (LSB)	Manufacturer specific	80
149	DRAM device manufacturer (MSB)	Manufacturer specific	2C
150–175	Manufacturer-reserved bytes 150–175	Reserved	00000000000000000000
176–255	Customer-reserved bytes 176–255	Reserved	FFFFFFFFFFFFFFFFFFFFFF

8 Product Label

The following label should be applied to all 240pin Unbuffered DDR3 DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

DDR3 DIMM Label Format:

ggggg eRxff PC3-wwwwm-abc-dd-ef

Contents need not be located on a single line of text, nor in the same font size. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields.

Where:

ggggg = Module total capacity, in bytes

256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed

1R = 1 rank of DDR3 SDRAM installed

2R = 2 ranks

xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly

x4 = x4 organization (4 DQ lines per SDRAM)

x8 = x8 organization

x16 = x16 organization

wwww = Module bandwidth in MB/s

5300 = 5.33 GB/s

6400 = 6.40 GB/s

m = Module Type

F = Fully Buffered DIMM ("FBDIMM")

M = Micro-DIMM

N = Mini-Registered DIMM ("Mini-RDIMM"), no address/command parity function

P = Registered DIMM ("RDIMM"), with address/command parity function

R = RDIMM, no address/command parity function

S = Small Outline DIMM ("SODIMM")

U = Unbuffered DIMM ("UDIMM")

a = DDR3 SDRAM CAS Latency, in clocks at maximum operating frequency

b = DDR3 SDRAM minimum ^tRCD specification, in clocks at maximum operating frequency

c = DDR3 SDRAM minimum ^tRP specification, in clocks at maximum operating frequency

dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM

e = Reference design file used for this design (if applicable)

A = Reference design for Raw Card Version "A" is used for this assembly

B = Reference design for Raw Card Version "B" is used for this assembly

Z = None of the reference designs were used for this assembly

f = Revision number of the reference design used

0 = Initial release

1 = First revision

2 = Second revision

P = Pre-release or Engineering sample

Z = To be used when field e = Z

Note: The Gerber reference designs provide as foundations for a module PCB. Manufacturers may make modifications to the designs as long as the signal integrity and timing is maintained.

9 DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to <http://www.jedec.org>
2. Click on 'Standards Publications'
3. Click on "Search Standards and Publications"
4. Use the search box "By Document Number"
5. Enter MO-269 to download

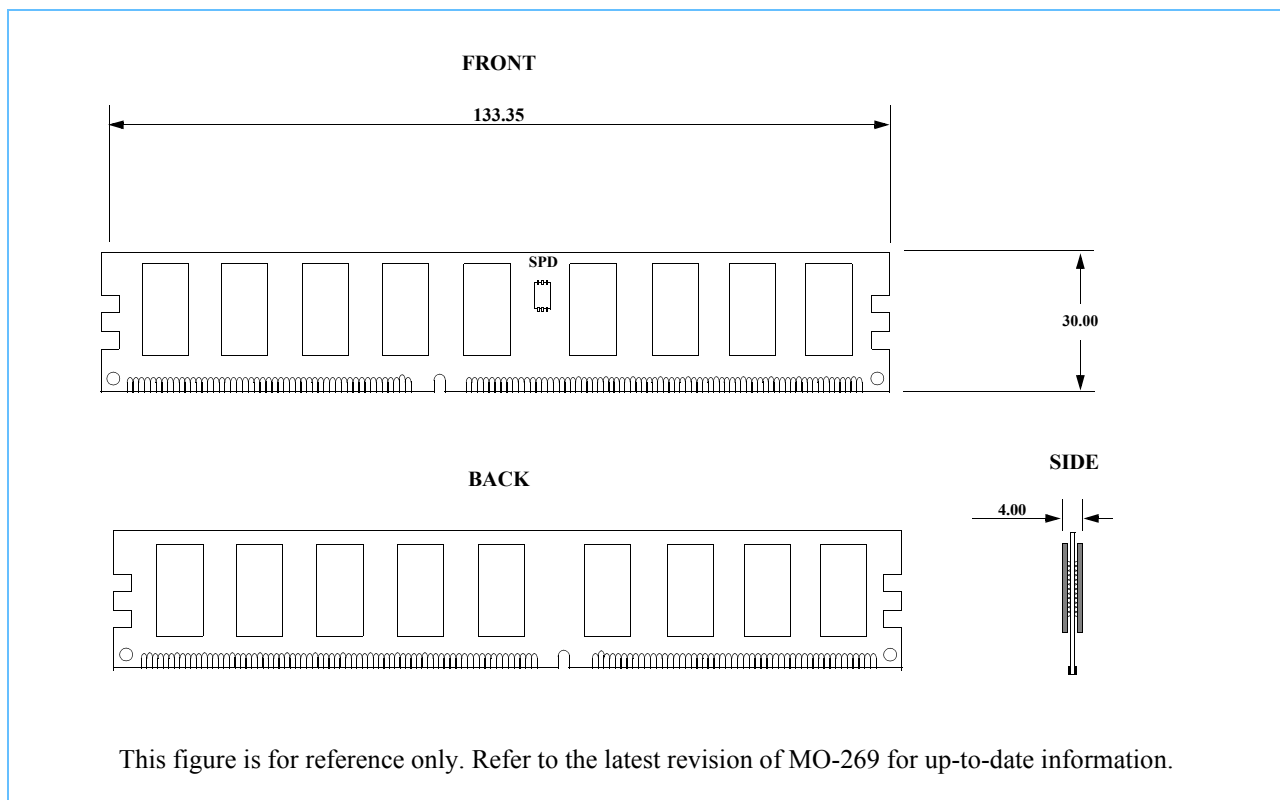


Figure 66 — Mechanical Drawing with Keying Positions

Annex A DDR3 240-Pin Connector S-Parameter

A.1 Purpose and Scope

The increase in DDR speeds and resultant bandwidth requirements has initiated activities within relevant JEDEC Committees to assess and further determine respectable performance (electrical) criteria for the connector interface (includes the module gold fingers). This document outlines target specifications for DDR3 UDIMM connector that were derived from empirical data (measurement) in terms of the connector to module interface. Other system link components, link topologies as well as transmitter and receiver requirements were discussed and considered in order to reach the consensus reflected in this document.

A.2 Related Documents

Document #	Document
MO-269	JEDEC Document: MO (Module Outline)
SO-007	JEDEC Document: SO (Socket Outline)
EIA-364	Electrical Connector/Socket Test Procedures Including Environmental Classifications
EIA-364-1000.01	Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Business Office Applications
T-Rex	S-parameter Measurement Procedure
PS-001	DDR3 Connector Specification

A.3 Mechanical Drawings

A.3.1 Connector Footprint

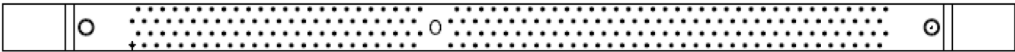


Figure A.1 – PCB Connector Footprint Refer to JEDEC SO-007 for details.

A.3.2 Connector Outline

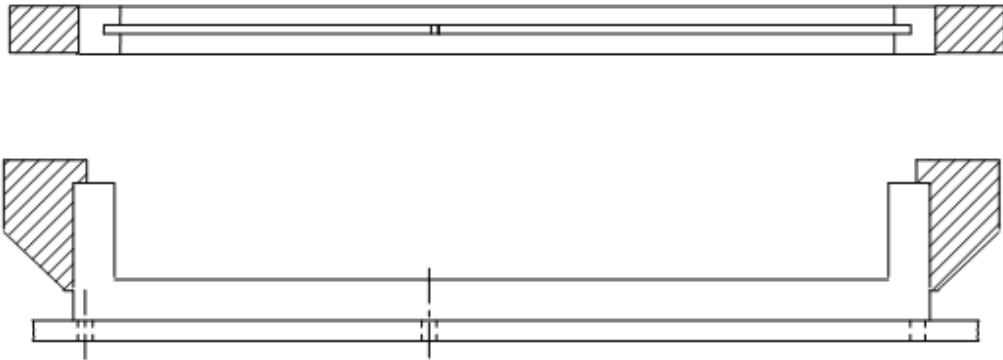


Figure A.2 – Connector Outline Refer to JEDEC SO-007 for details.

A.3.3 Module Outline

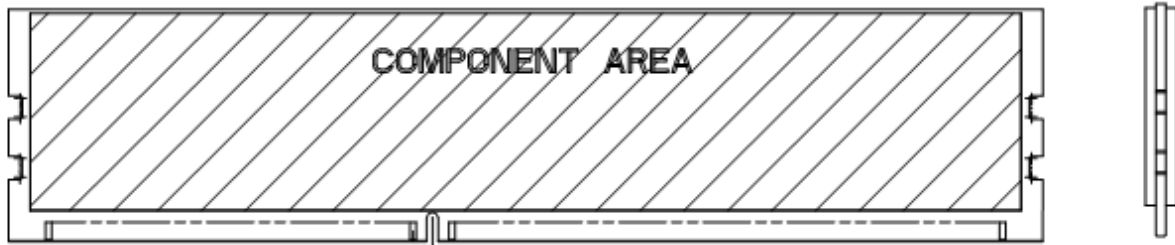


Figure A.3 – Module Profile, refer to JEDEC MO-269 for details

A.4 Connector S-Parameter Requirements

A.4.1 Frequency Domain Requirements (see note below the table)

Parameter*	Specification	Measurement Procedure
<p>S21 (Insertion Loss)</p> <p>Note: Effects of the base board thru-hole via and module gold edge finger are included in the spec.</p>	<p>< 0.8 dB, $f \leq 2.5$ GHz < 1.2 dB, $2.5 \text{ GHz} < f \leq 3.5$ GHz < 2.5 dB, $3.5 \text{ GHz} < f \leq 5.0$ GHz</p>	<p>See T-Rex Measurement Procedure document.</p> <ol style="list-style-type: none"> 1. The step-by step measurement procedure is outlined in the T-Rex Measurement Procedure document. 2. A T-Rex test fixture for connector characterization shall be provided.
<p>S11 (Return Loss)</p> <p>Note: Effects of the base board thru-hole via and module gold edge finger are included in the spec.</p>	<p>< -10.0 dB, $f \leq 3.5$ GHz < -5.0 dB, $3.5 \text{ GHz} < f \leq 5.0$ GHz</p>	<p>See T-Rex Measurement Procedure document.</p> <ol style="list-style-type: none"> 1. The step-by step measurement procedure is outlined in the T-Rex Measurement Procedure document. 2. A T-Rex test fixture for connector characterization shall be provided.
<p>FEXT S14 (Far End Cross-Talk)</p> <p>Note: Effects of the base board thru-hole via and module gold edge finger are included in the specification.</p>	<p>< -17 dB, $f \leq 2.5$ GHz < -13.5 dB, $2.5 \text{ GHz} < f \leq 3.5$ GHz < -10 dB, $3.5 \text{ GHz} < f \leq 5.0$ GHz</p> <p>(Measurement one pin adjacent to the drive pin)</p>	<p>See T-Rex Measurement Procedure document.</p> <ol style="list-style-type: none"> 1. The step-by step measurement procedure is outlined in the T-Rex Measurement Procedure document. 2. A T-Rex test fixture for connector characterization shall be provided.
<p>NEXT S13 (Near End X-Talk)</p> <p>Note: Effects of the base board thru-hole via and module gold edge finger are included in the specification.</p>	<p>< -11.5 dB, $f \leq 2.5$ GHz < -9.5 dB, $2.5 \text{ GHz} < f \leq 3.5$ GHz < -8 dB, $3.5 \text{ GHz} < f \leq 5.0$ GHz</p> <p>(Measurement one pin adjacent to the drive pin)</p>	<p>See T-Rex Measurement Procedure document.</p> <ol style="list-style-type: none"> 1. The step-by step measurement procedure is outlined in the T-Rex Measurement Procedure document 2. A T-Rex test fixture for connector characterization shall be provided.

*** Note: The parameters noted in Chart 6.1 apply when the reference plane under the gold contact pads is pulled back 100% or below the gold pads at least 0.2 mm.**

A.4.2 Frequency Domain Measurements

Figures A.4 and A.5 illustrate Base Board and Module footprint for electrical measurements.

Measurements shall be taken from 250 MHz to 10.0 GHz, using a Vector Network Analyzer (VNA). For maximum accuracy, the impact of the trace between the SMA connectors and the connector will be removed by TRL calibration. DUT trace impedance is defined as $50 (\pm 7.5\%)$ Ohms. Refer to the Section A.5 for details on the DUT board and DUT module.

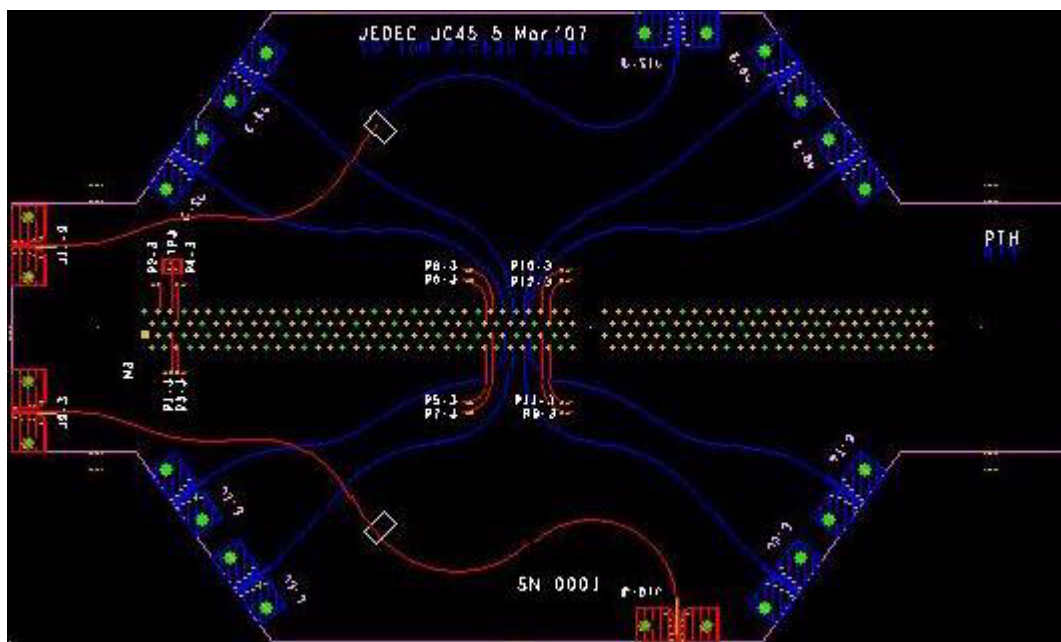


Figure A.4 – T-Rex Base board footprint illustration

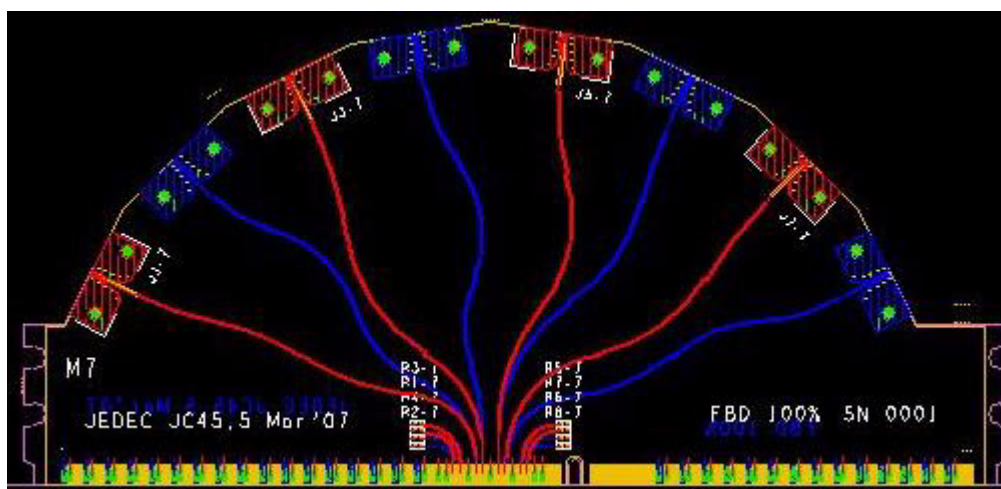


Figure A.5 – T-Rex Module board footprint illustration

All measurements must be made at room temperature and humidity conditions, not to exceed 65% RH (non-condensing).

A.5 Measurement of S-parameters

A.5.1 Required Equipment

Vector Network Analyzer (VNA) System – TRL calibration capability required.

SMA’s- Southwest Microwave 292-07A-5.

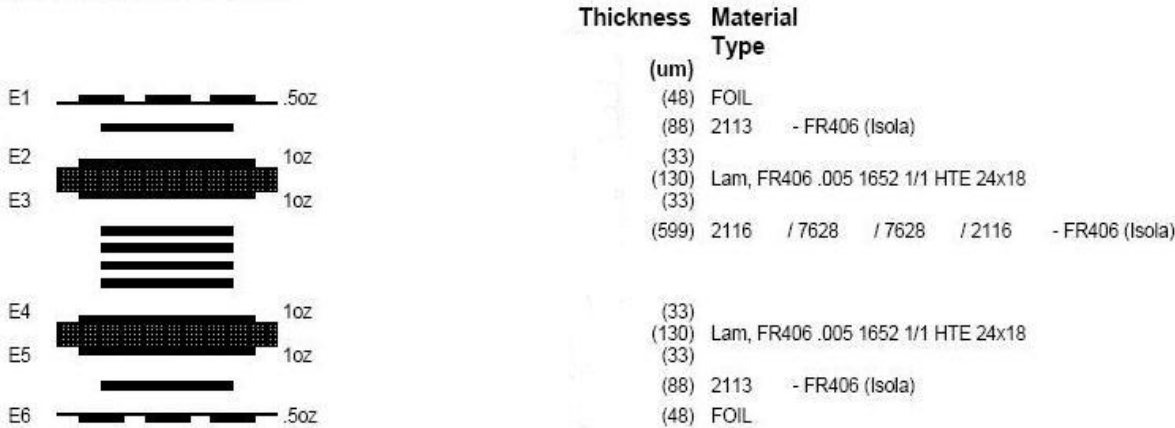
Calibration Standard - TRL standards are part of test board panel. The following calibration standards are provided: Open, Short, Zero length Thru, and Lines.

Two 50 Ω high frequency, low loss phase-matched cables. Recommend cables offered by Micro Coax (part number UFB197C) or equivalent. The cables are used to connect the SMA’s to the measurement ports on the VNA.

A.5.2 Test Fixture and Samples

Figure A6 describe details of the 6-layer DUT base board and DUT module PCB stackup to be used. Reference design including PCB stackup and specifications of the DUT module card can be provided upon request (JC45.5). The DUT base board and module impedance is defined at 50 (± 7.5%) Ohms.

soldermask: Enthone 3241 DSR



Overall Board Thicknesses (Over Conductor)
(mm)
nom: (1.26)

Figure A6 - DUT Board PCB stackup.

A.5.3 Sample Preparation

DUT base board and DUT module shall be for electrical test only. Align the connector pins with the corresponding through holes vias of the DUT base board. Firmly press the connector into the base board with uniform pressure across the connector body until all of the connector standoff points are flush with the DUT base board surface. Use wave solder process to mate the connector and DUT base board. Ensure that the gap between the DUT base board and the connector standoff must be less than 0.05 mm to be considered a good sample.