

## 4.20.17 - 214-Pin PC3-12800 DDR3 Unbuffered MicroDIMM Design Specification

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# **PC3-12800 DDR3 Unbuffered MicroDIMM Reference Design Specification**

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## 1. Product Description

This reference specification defines the electrical and mechanical requirements for the PC3-12800 memory module, a 214-pin, 800MHz clock (16000 MT/s data rate), 64-bit wide, Unbuffered Synchronous Double Data Rate 3(DDR3) DRAM Micro Dual In-Line Memory Module (DDR3 SDRAM MicroDIMMs). It also defines a slower version, the PC3-10600, using 667MHz clock (1333 MT/s data rate) DDR3 SDRAMs, the PC3-8500, using 533MHz clock (1066 MT/s data rate) DDR3 SDRAMs, the PC3-6400, using 400MHz clock (800 MT/s data rate) DDR3 SDRAMs. These DDR3 SDRAM MicroDIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Reference design examples are included which provide an initial basis for Unbuffered MicroDIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 800MHz clock rate support. Other designs are acceptable, and all Unbuffered DDR3 MicroDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

### Product Family Attributes

Attribute:	Values:	Notes:
MicroDIMM Organization	x 64	
MicroDIMM Dimensions (nominal)	30 mm high, 54.0mm wide	
MicroDIMM Types Supported	Unbuffered	
Pin Count	214	
SDRAMs Supported	512 Mb, 1 Gb, 2 Gb, 4 Gb	
Capacity	256 MB, 512 MB, 1 GB, 2GB	
Serial Presence Detect	Should be consistent with JEDEC latest Rev.	
Voltage Options, Nominal	1.5 V $V_{DD}$ 1.5 V $V_{DDQ}$ 3.0V to 3.6 V $V_{DDSPD}$	1
Interface	SSTL_15	
Note 1: $V_{DDSPD}$ is not tied to $V_{DD}$ or $V_{DDQ}$ on the DDR3 MicroDIMM.		

### Raw Card Summary

Raw Card	Number of DDR3 SDRAMs	SDRAM Organization	Number of Ranks
A	4	x16	1

## 2. Environmental Requirements

PC3-12800 DDR3 SDRAM Unbuffered MicroDIMMs are intended for use in mobile computing environments that have limited capacity for heat dissipation.

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T <sub>OPR</sub>	Operating Temperature (ambient)	0 to +65	°C	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 3. Architecture

### Pin Description

CK[1:0]	Clock Inputs, positive line	2	DQS[7:0]	Data strobes	8
$\overline{CK}$ [1:0]	Clock inputs, negative line	2	$\overline{DQS}$ [7:0]	Data strobes complement	8
CKE[1:0]	Clock Enables	2			
$\overline{RAS}$	Row Address Strobe	1	$\overline{EVENT}$	Thermal sensor EVENT signal	1
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	DDR3 SDRAM RESET signal	1
$\overline{WE}$	Write Enable	1	NC, TEST	Logic Analyzer specific test pin (No connect on MicroDIMM)	1
$\overline{S}$ [1:0]	Chip Selects	2			
A[9:0], A11, A[15:13]	Address Inputs	14	V <sub>DD</sub>	Core and I/O Power	18
A10/AP	Address Input/Autoprecharge	1	V <sub>SS</sub>	Ground	56
A12/ $\overline{BC}$	Address Input/Burst Chop	1	V <sub>REFDQ</sub>	Input/Output Reference for Data	1
			V <sub>REFCA</sub>	Input/Output Reference for Commands and address	1
BA[2:0]	SDRAM Bank Address	3			
ODT[1:0]	On-die termination control	2			
SCL	Serial Presence Detect (SPD) Clock Input	1	V <sub>tt</sub>	Termination Voltage	2
SDA	SPD Data Input/Output	1	V <sub>DDSPD</sub>	SPD Power	1
SA[1:0]	SPD address	2			
			NC	No connect	8
DQ[63:0]	Data Input/Output	64			
DM[7:0]	Data Masks	8			<b>Total: 214</b>

## Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/ $\overline{\text{CK0}}$ , CK1/ $\overline{\text{CK1}}$	Input	Cross point	<b>Clock:</b> CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$ . Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$ (both directions of crossing).
CKE[1:0]	Input	Active High	<b>Clock Enable:</b> CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for self refresh exit. After VREF has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$ , ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{\text{S}}$ [1:0]	Input	Active Low	<b>Chip Select:</b> All commands are masked when $\overline{\text{S}}$ is registered HIGH. $\overline{\text{S}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{S}}$ is considered part of the command code.
$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	Input	Active Low	<b>Command Inputs:</b> $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{S}}$ ) define the command being entered.
BA[2:0]	Input	—	<b>Bank Address Inputs:</b> BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
ODT[1:0]	Input	Active High	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ , and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU/ $\overline{\text{DQSU}}$ , DQSL/ $\overline{\text{DQSL}}$ , DMU, and DML signal. The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.
A0 -A15	Input	—	<b>Address Inputs:</b> Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below). The address inputs also provide the op-code during (Extended) Mode Register Set commands.
A10/AP	Input		<b>Autoprecharge:</b> A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/ $\overline{\text{BC}}$	Input		<b>Burst Chop:</b> A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
DQ[63:0]	In/Out	—	Data Input/Output pins.
DM[7:0]	Input	Active High	<b>Input Data Mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM is enabled by EMRS command.
$\overline{\text{DQS}}$ [7:0], DQS[7:0]	In/Out	Cross point	<b>Data Strobe:</b> output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, $\overline{\text{DQSL}}$ corresponds to the data on $\overline{\text{DQL0-DQL7}}$ ; DQSU corresponds to the data on $\overline{\text{DQU0-DQU7}}$ . The data strobe DQS, $\overline{\text{DQSL}}$ , and DQSU are paired with differential signals $\overline{\text{DQS}}$ , $\overline{\text{DQSL}}$ , and DQSU, respectively, to provide differential pair signaling to the system during reads and writes.
V <sub>DD</sub> , V <sub>DD</sub> SPD, V <sub>SS</sub>	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.

## Input/Output Functional Description

Symbol	Type	Polarity	Function
V <sub>REFCA</sub> , V <sub>REFDQ</sub>	Supply	---	Reference Voltage for Data, Commands and Address
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V <sub>DD</sub> to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V <sub>DD</sub> to act as a pull up.
SA[1:0]	Input	—	Address pins used to select the Serial Presence Detect base address.
NC,TEST	In/Out	—	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (MicroDIMMs).
$\overline{\text{RESET}}$	Input	Active Low	$\overline{\text{RESET}}$ is an active low input to the DRAM compatible with a CMOS rail to rail signal with a DC high $\Rightarrow 0.8 * V_{DDQ}$ and DC low $\leq 0.2 * V_{DDQ}$ , i.e., 1.20V for high and 0.30V for low. $\overline{\text{RESET}}$ is referenced to VSS. No signal termination is required for $\overline{\text{RESET}}$ . It is expected that the $\overline{\text{RESET}}$ signal will be heavily loaded across multiple chips. A slow slew rate receiver design is recommended. It is also recommended that DRAM designs implement on-chip noise filtering to prevent false triggering.
$\overline{\text{EVENT}}$	Output	Active Low	$\overline{\text{EVENT}}$ signal from the thermal sensor

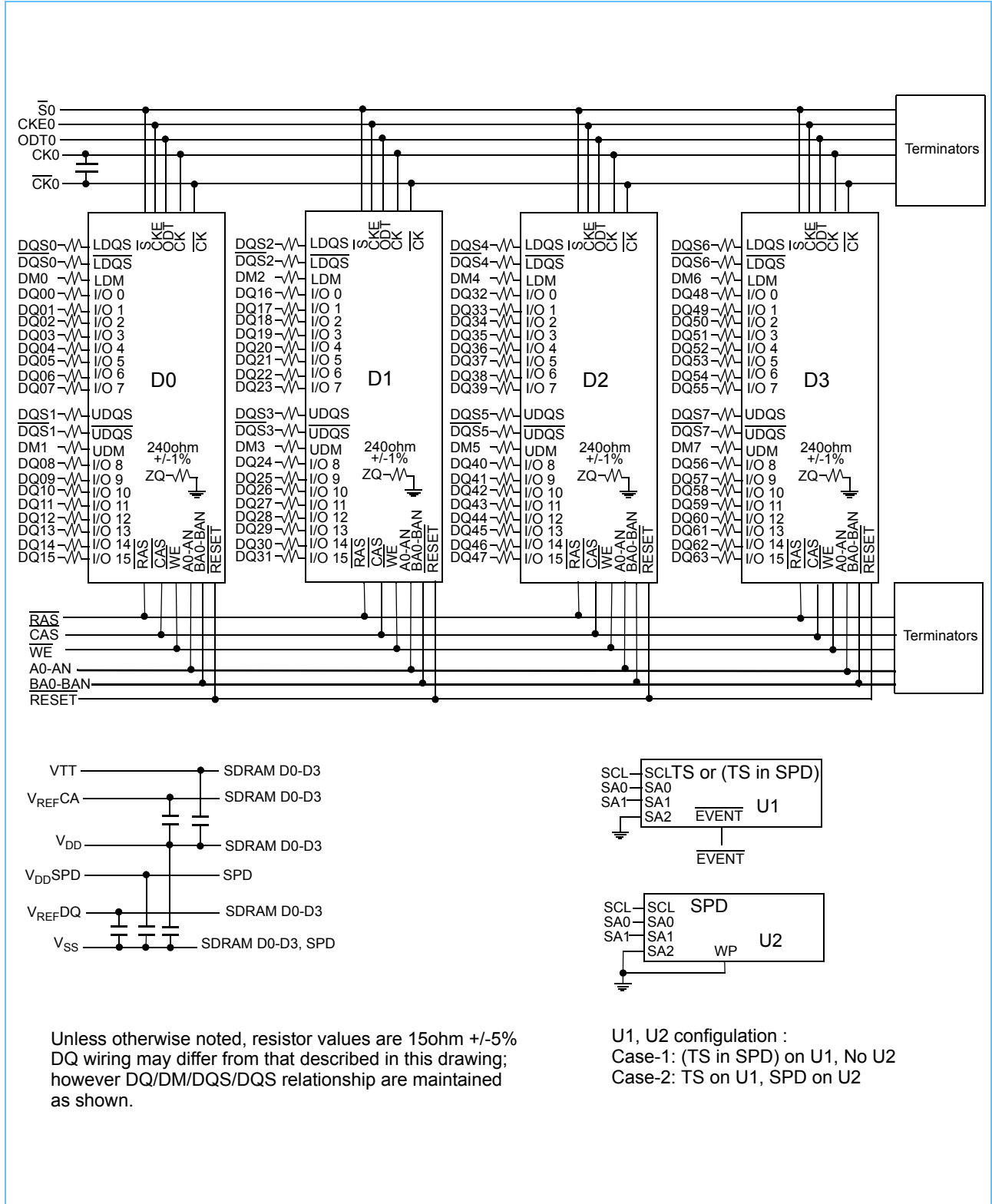
## DDR3 SDRAM MicroDIMM Pinout

Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side	Pin #	Lower Side	Pin #	Upper Side
1	V <sub>REFD</sub> Q	108	V <sub>SS</sub>	28	DM3	135	DQS2	55	V <sub>DD</sub>	162	V <sub>DD</sub>	82	DQ34	189	DQ47
2	V <sub>SS</sub>	109	DQ4	29	V <sub>SS</sub>	136	V <sub>SS</sub>	56	A10/AP	163	A0	83	DQ35	190	V <sub>SS</sub>
3	DQ12	110	DQ5	30	$\overline{\text{DQS3}}$	137	DQ22	57	BA0	164	BA1	84	V <sub>SS</sub>	191	DQ42
4	DQ13	111	V <sub>SS</sub>	31	DQS3	138	DQ23	58	V <sub>DD</sub>	165	V <sub>DD</sub>	85	V <sub>SS</sub>	192	DQ43
5	V <sub>SS</sub>	112	DQ0	32	V <sub>SS</sub>	139	V <sub>SS</sub>	59	$\overline{\text{S0}}$	166	$\overline{\text{RAS}}$	86	V <sub>SS</sub>	193	V <sub>SS</sub>
6	DQ8	113	DQ1	33	DQ30	140	DQ18	60	$\overline{\text{CAS}}$	167	$\overline{\text{WE}}$	87	DQ52	194	DQ60
7	DQ9	114	V <sub>SS</sub>	34	DQ31	141	DQ19	61	V <sub>DD</sub>	168	V <sub>DD</sub>	88	DQ53	195	DQ61
8	V <sub>SS</sub>	115	DM0	35	V <sub>SS</sub>	142	V <sub>SS</sub>	62	A13 <sup>3</sup>	169	ODT0	89	V <sub>SS</sub>	196	V <sub>SS</sub>
9	DM1	116	V <sub>SS</sub>	36	DQ26	143	NC	63	ODT1	170	$\overline{\text{S1}}$	90	DQ48	197	DQ56
10	V <sub>SS</sub>	117	$\overline{\text{DQS0}}$	37	DQ27	144	NC	64	V <sub>DD</sub>	171	V <sub>DD</sub>	91	DQ49	198	DQ57
11	$\overline{\text{DQS1}}$	118	DQS0	38	V <sub>SS</sub>	145	$\overline{\text{RESET}}$	65	NC,TEST T	172	NC	92	V <sub>SS</sub>	199	V <sub>SS</sub>
12	DQS1	119	V <sub>SS</sub>	39	NC	146	NC	66	NC	173	V <sub>REFCA</sub>	93	DM6	200	DM7
13	V <sub>SS</sub>	120	DQ6	40	V <sub>DD</sub>	147	V <sub>DD</sub>	67	V <sub>SS</sub>	174	NC	94	V <sub>SS</sub>	201	V <sub>SS</sub>
14	DQ14	121	DQ7	41	CKE0	148	CKE1	68	DQ36	175	NC	95	$\overline{\text{DQS6}}$	202	$\overline{\text{DQS7}}$
15	DQ15	122	V <sub>SS</sub>	42	A14 <sup>3</sup>	149	A15 <sup>3</sup>	69	DQ37	176	V <sub>SS</sub>	96	DQS6	203	DQS7
16	V <sub>SS</sub>	123	DQ2	43	V <sub>DD</sub>	150	V <sub>DD</sub>	70	V <sub>SS</sub>	177	DQ44	97	V <sub>SS</sub>	204	V <sub>SS</sub>
17	DQ10	124	DQ3	44	A12/ $\overline{\text{BC}}$	151	BA2	71	DQ32	178	DQ45	98	DQ54	205	DQ62
18	DQ11	125	V <sub>SS</sub>	45	A11	152	A9	72	DQ33	179	V <sub>SS</sub>	99	DQ55	206	DQ63
19	V <sub>SS</sub>	126	DQ20	46	V <sub>DD</sub>	153	V <sub>DD</sub>	73	V <sub>SS</sub>	180	DQ40	100	V <sub>SS</sub>	207	V <sub>SS</sub>
20	V <sub>SS</sub>	127	DQ21	47	A8	154	A7	74	DM4	181	DQ41	101	DQ50	208	DQ58
21	V <sub>SS</sub>	128	V <sub>SS</sub>	48	A5	155	A6	75	V <sub>SS</sub>	182	V <sub>SS</sub>	102	DQ51	209	DQ59
22	DQ28	129	DQ16	49	V <sub>DD</sub>	156	V <sub>DD</sub>	76	$\overline{\text{DQS4}}$	183	DM5	103	V <sub>SS</sub>	210	V <sub>SS</sub>
23	DQ29	130	DQ17	50	A3	157	A4	77	DQS4	184	V <sub>SS</sub>	104	SA0	211	$\overline{\text{EVENT}}$
24	V <sub>SS</sub>	131	V <sub>SS</sub>	51	A2	158	A1	78	V <sub>SS</sub>	185	$\overline{\text{DQS5}}$	105	V <sub>DD</sub> SPD	212	SDA
25	DQ24	132	DM2	52	V <sub>DD</sub>	159	V <sub>DD</sub>	79	DQ38	186	DQS5	106	SA1	213	SCL
26	DQ25	133	V <sub>SS</sub>	53	CK1	160	CK0	80	DQ39	187	V <sub>SS</sub>	107	VTT	214	VTT
27	V <sub>SS</sub>	134	$\overline{\text{DQS2}}$	54	$\overline{\text{CK1}}$	161	$\overline{\text{CK0}}$	81	V <sub>SS</sub>	188	DQ46				

## Note.

1. NC = No Connect; NU = Not Useable, RFU = Reserved Future Use.
2. TEST(pin 65) is reserved for bus analysis probes and is NC on normal memory modules.
3. This address might be connected to NC balls of the NC balls of the DRAMs(depending on density); either way they will be connected to the termination resistor.

Block Diagram: Raw Card Version A (Populated as 1rank of x16 SDRAMs)



## 4. Component Details

### x16 Ballout(MO-207 DU-Z)for 512Mb, 1Gb, 2Gb and 4Gb DDR3 SDRAMs (Top View)

1	2	3		7	8	9
VDDQ	DQU5	DQU7	<b>A</b>	DQU4	VDDQ	VSS
VSSQ	VDD	VSS	<b>B</b>	$\overline{\text{DQS}}\text{U}$	DQU6	VSSQ
VDDQ	DQU3	DQU1	<b>C</b>	DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU	<b>D</b>	DQU0	VSSQ	VDD
USS	VSSQ	DQL0	<b>E</b>	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	<b>F</b>	DQL1	DQL3	VSSQ
VDDQ	DQL6	$\overline{\text{DQSL}}$	<b>G</b>	VDD	VSS	USSQ
VREFDQ	VDDQ	DQL4	<b>H</b>	DQL7	DQL5	VDDQ
NC	VSS	$\overline{\text{RAS}}$	<b>J</b>	CK	VSS	NC
ODT	VDD	$\overline{\text{CAS}}$	<b>K</b>	$\overline{\text{CK}}$	VDD	CKE
NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$	<b>L</b>	A10/AP	ZQ	NC
VSS	BA0	BA2	<b>M</b>	A15	VREFCA	VSS
VDD	A3	A0	<b>N</b>	A12/ $\overline{\text{BC}}$	BA1	VDD
VSS	A5	A2	<b>P</b>	A1	A4	VSS
VDD	A7	A9	<b>R</b>	A11	A6	VDD
VSS	$\overline{\text{RESET}}$	A13	<b>T</b>	A14	A8	VSS

## DDR3 SDRAM FBGA Component Specifications

The DDR3 SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC MO-207 DU-Z(no support ball)and DY-Z(with support ball).

## Reference SPD Component Specifications

The Serial Presence Detect EEPROMs have their own power pin,  $V_{DDSPD}$ , so that they can be programmed or read without powering up the rest of the module.

### SPD Component DC Electrical Characteristics

Symbol	Parameter	Min	Nom	Max	Units
$V_{DDSPD}$	Core Supply Voltage	3.0	3.3	3.6	V

## Thermal Sensor Component Specifications

The Thermal Sensor has the common SMBus signals and power/GND pins with SPD. It must support the overvoltage(Max 10V) tolerance on the A0 pin.

### Thermal Sensor Component DC Electrical Characteristics

Symbol	Parameter	Min	Nom	Max	Units
$V_{DDSPD}$	Core Supply Voltage	3.0	3.3	3.6	V

## 5. Unbuffered MicroDIMM Details

### DDR3 SDRAM Module Configurations (Reference Designs)

Raw Card	MicroDIMM Capacity	MicroDIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	# of Ranks	SDRAM Package Type	# of banks in SDRAM	# Address bits row/col
A	256 MB	32 M x 64	512 Mbit	32 M x 16	4	1	FBGA	8	12/10
A	512 MB	64 M x 64	1 Gbit	64 M x 16	4	1	FBGA	8	13/10
A	1 GB	128 M x 64	2 Gbit	128 M x 16	4	1	FBGA	8	14/10
A	2 GB	256 M x 64	4 Gbit	256 M x 16	4	1	FBGA	8	15/10

### Input Loading Matrix

Signal Names	Input Device	R/C A
Clock (CK <sub>n</sub> , $\overline{\text{CK}}_n$ )	SDRAM	4
CKEn/ $\overline{\text{S}}_n$ /ODT <sub>n</sub>	SDRAM	4
Addr/ $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ /BA/ $\overline{\text{WE}}$	SDRAM	4
DQ <sub>n</sub> /DQS <sub>n</sub> / $\overline{\text{DQS}}_n$ /DM <sub>n</sub>	SDRAM	1
SCL/SDA/SAn	EEPROM	1

### DDR3 MicroDIMM Gerber File Releases

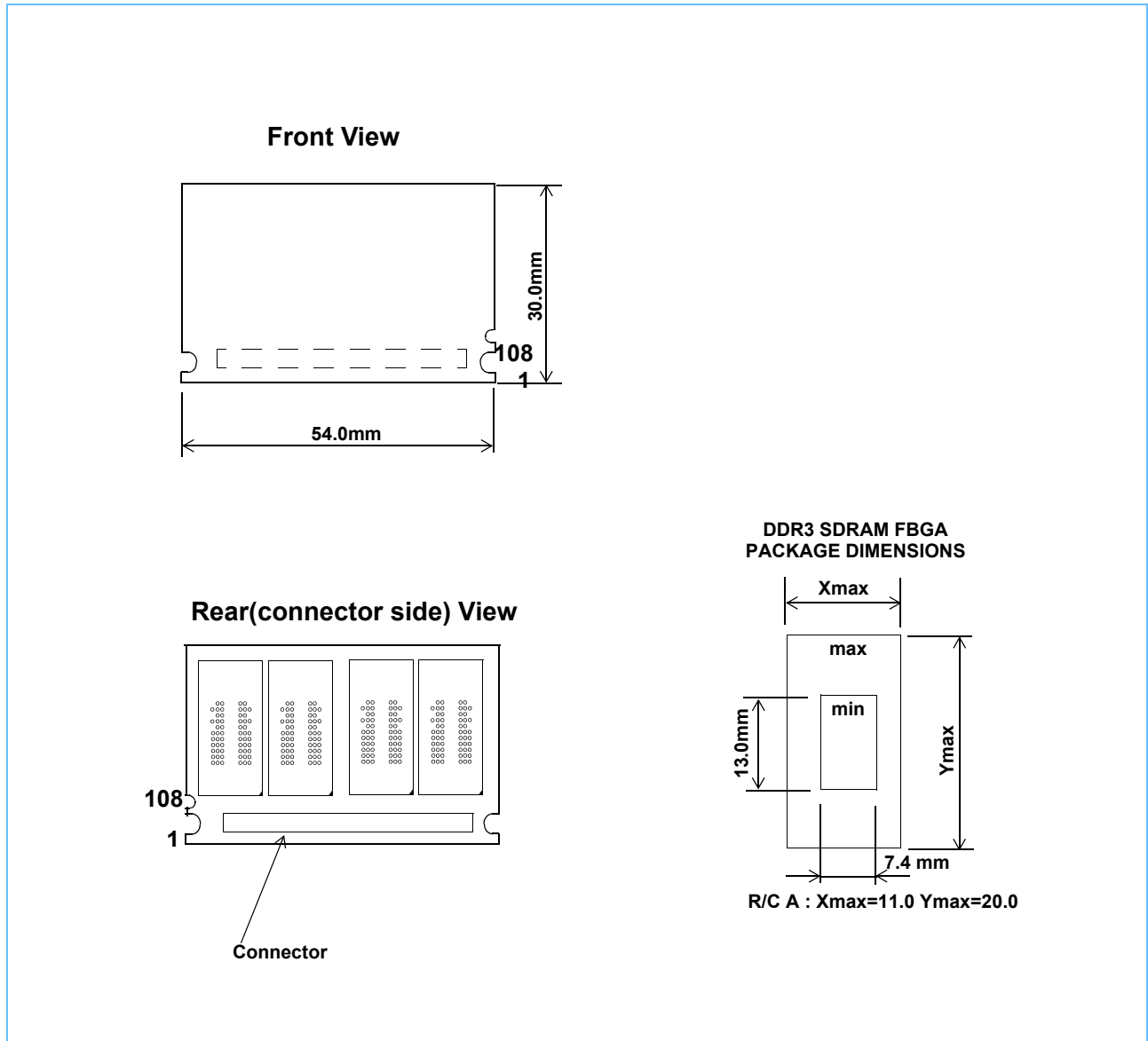
Reference design file updates will be released as needed. This specification will reflect the most recent design files, but may be updated to reflect clarifications to the specification only; in these cases, the design files will not be updated. The following table outlines the most recent design file releases

**Note:** Future design file releases will include both a date and a revision label. All changes to the design file are also documented within the 'read-me' file.

Raw Card	Specification Revision	Applicable Design File	Notes
A	0.34	0.31	

### Example Raw Card Component Placement

This example is for reference only; refer to JEDEC standard MO-260 variation C for details.



## 6. MicroDIMM Wiring Details

### Signal Groups

This specification categorizes SDRAM timing-critical signals into four groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Page
Data, Data Mask, Data Strobe	DQ [63:0], DM[7:0], DQS[7:0], $\overline{\text{DQS}}$ [7:0]	19, 20
Clocks	CK [1:0], $\overline{\text{CK}}$ [1:0]	21
Select, Clock Enable, ODT	$\overline{\text{S}}$ [1:0], CKE [1:0], ODT[1:0]	22
Address/command	Ax, BAx, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	23

### General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing recommendations are as follows. Other stackups and layouts are possible that meet the electrical characteristics.

- Route all signal traces using appropriate trace width(e.g: 0.075mm) and enough spacing(e.g: 0.15mm) between adjacent traces considering cross talk effect.
- Route clocks as much as possible using the inner layers.
- Test points are required.

### Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered MicroDIMM designs. The diagrams should be used to determine individual signal wiring on a MicroDIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify MicroDIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one DDR3 SDRAM input unless mentioned. It is highly recommended that the net structure routing data in this document be simulated by the user.

## Clock Control and Address/Command Groups

The DDR3 modules implement a fly-by topology for routing CLK, CTRL, and ADD/CMD signal groups, rather than the traditional Tree structure utilized on legacy DDR modules. On DDR3 modules, the CTRL and ADD/CMD groups are length/delay matched to CLK, between the connector and each SDRAM, resulting in significantly reduced timing skew across these groups, vs legacy modules. This fundamental topology change is instrumental in enabling the higher operating speeds of DDR3. A summary table of the length/delay matching rules associated with these signal groups is provided below.

## Module Length Matching Rules

Signal Group	Matching Rules
CLM to CLK# Matching	Match TLx segment by TLx to segment to within 0.1mm
CLK Pair to CLK Pair Matching (Pair to Pair - Avg. Length)	Match total compensated length from connector to each DRAM to within 0.25mm
CTRL Group Matching	Match total compensated length from connector to each DRAM to within 1.0mm
CTRL to CLK Matching	Match total compensated length of all CTRL signals from connector to each DRAM to within CLK +/- 0.5mm
ADR/CMD Matching	Match total compensated length from connector to each DRAM to within 1.0mm
ADR/CMD to CLK Matching	Match total compensated length of all ADR/CMD signals from connector to each DRAM to within CLK +/- 0.5mm
TL2 Stub Length Matching	Match TL2 stub length at each DRAM (top and bottom), on a given signal, to within 0.5mm
TL2 MAX Stub Length Limits	CLK : TL2 <= 3.0mm CTR: TL2 <= 4.0mm ADR/CMD: TL2 <= 5.6mm
CLK First to Last Length	The maximum length from the first DRAM and the last DRAM = 166mm
Neckdown Length	5.0mm <= length <= 10.0mm Match to within +/- 1.0mm
<ol style="list-style-type: none"> <li>1. All length matching is done using velocity compensated stripline equivalent lengths.</li> <li>2. The velocity compensation ratio of 1.1 will be used (MS length / 1.1 = SL equivalent length)</li> <li>3. The neckdown length is the trailing portion of the TL1 segment, which is routed at 0.1mm width</li> <li>4. Maximum first to last length can be calculated by subtracting length to the first DRAM from the length to the last DRAM</li> <li>5. Via compensation is not required</li> <li>6. All clocks are length matched, segment by segment and have matched via count</li> </ol>	

## Lead-in vs Loaded Sections

The CLK, CTRL, and ADD/CMD topologies are conceptually divided into two topology sections. The segments between the connector and the first SDRAM node via (TL0 + TL1) are collectively termed the lead-in section, while the segments that run between SDRAM node vias (TL3, TL4, TL5...), as well as the SDRAM load stubs (TL2), are collectively termed the loaded section. The loaded section also includes the segments between the last SDRAM and the termination.

In order to reduce the impedance discontinuity seen at the first load, the lead-in section is routed at a lower nominal impedance than the loaded section, typically with the lead-in section routed at 45 ohms nominal and the loaded section routed at 60 ohms nominal, although some modules may vary. The transition from the wider lead-in trace width to the standard width of the loaded section must occur within a length window preceding the first SDRAM node via, which is termed the neckdown length.

## Length/Delay Matching to SDRAM Devices

As mentioned previously, length/delay matching is required between the connector and each SDRAM individually. The length/delay matching process is iterative in nature, and there is no single best method defined. It is generally recommended that the path from the connector to the first SDRAM (TL0 + TL1 + TL2) be matched across the CLK group, and then across CTRL and ADD/CMD groups, as per the length matching guidelines, adjusting CLK length as needed to reach the length window of the CTRL and ADD/CMD groups. It is important to note that the matching is done from connector to the SDRAM ball, and includes the TL2 segment. It is during this process that the breakout pattern dependent length variance in the TL2 stub on each signal will be tuned out.

Once length/delay matching to the first device is completed, the length matching to the remaining devices is straightforward, and can be accomplished by simply length matching the intra-node segments (TL3, TL4, TL5..), assuming the TL2 stub length for a given signal does not vary from SDRAM to SDRAM.

Note that it is recommended that the TL2 stub length on any given signal be closely matched on top and bottom side pattern, and at each SDRAM. This will facilitate the most accurate overall length/delay matching.

The total compensated length from the connector to the first and to the last SDRAM is documented in the segment length tables for each module type, in the net structure definitions sections. It is required that the length matching rules be met at all SDRAM devices.

## Velocity Compensation

Since the lead-in section can have a wide variation in the proportion of its length routed as microstrip vs stripline, the length/delay matching process includes a mechanism for compensating for the velocity delta between these two types of PCB interconnect. A compensation factor of 1.1 has been specified for this purpose. All microstrip segment lengths are to be divided by 1.1 before summation into the length matching equation. The resulting compensated length is termed the stripline equivalent length. While some amount of residual velocity mismatch skew remains in the design, the process is a substantial improvement over simple length matching.

## Data and Strobe Group

The DDR3 modules treat each byte lane as a separate signal sub-group, with each byte lane group length/delay matched, with velocity compensation as previously described. The length of the individual byte lanes may vary substantially across the module, with the controller providing timing realignment circuitry. A summary table of the length/delay matching rules associated with the data signal group is provided below.

## DQ/DQS Matching

Signal Group	Matching Rules
DQS to DQS# Matching	Match TLx segment by TLx to segment to within 0.1mm
DQ/DM to DQS within Byte Lane	Match total compensated length from connector to DRAM of all DQ and DM signals within a byte lane to DQS within +/- 0.2mm
<ol style="list-style-type: none"> <li>1. All length matching is done using velocity compensated stripline equivalent lengths.</li> <li>2. The velocity compensation ratio of 1.1 will be used (MS length / 1.1 = SL equivalent length)</li> <li>3. Via compensation is only required if the via count varies within the byte lane. Via equivalent length = 2.0mm</li> </ol>	

## Via Compensation

All current MicroDIMM module designs have matched via counts within all byte lanes, and therefore, via compensation is not required. Should future modules be developed where the via count is mismatched within a byte lane, then via compensation must be implemented, and the via equivalent length is defined to be 2.0 mm.

## Decoupling Capacitor Guideline

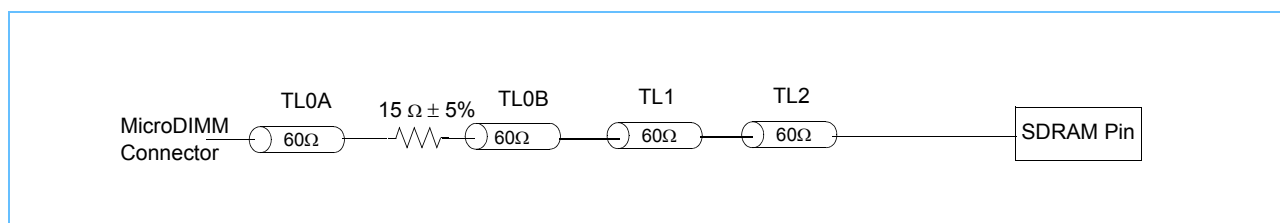
	Value, Counts	Note
VDD	Minimum 3 of 0.1uF decoupling capacitors per DRAM	Should be placed as close as possible to the DRAM VDD ball
	Minimum 2 of 2.2uF bulk decoupling capacitors per module	
Vtt	Minimum 1 of 0.1uF decoupling capacitors per 3 termination resistors (per 2 termination resistors is preferable.)	Should be placed as close as possible to the Vtt termination resistor
	Minimum 1 of 0.1uF decoupling capacitor at near the card edge Vtt pin	
V <sub>REFCA</sub>	Minimum 1 of 0.1uF decoupling capacitor per DRAM	Should be placed as close as possible to the DRAM V <sub>REFCA</sub> ball
	Minimum 1 of 0.1uF decoupling capacitor at near the card edge V <sub>REFCA</sub> pin	
V <sub>REFDQ</sub>	Minimum 1 of 0.1uF decoupling capacitor per DRAM	Should be placed as close as possible to the DARM V <sub>REFDQ</sub> ball
	Minimum 1 of 0.1uF decoupling capacitor at near the card edge V <sub>REFDQ</sub> pin	
<ol style="list-style-type: none"> <li>1. This guideline should be kept as long as the space permits</li> <li>2. 0.1uF can be replaced with 0.22uF</li> </ol>		

## Data Net Structures

### DQ[63:0], DM[7:0], DQS[7:0], $\overline{\text{DQS}}[7:0]$

Special attention has been paid to balancing the data nets within a DDR3 SDRAM, within a particular MicroDIMM, and across the MicroDIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. It is recommend to maintain consistent delays for all nets as described in the following tables.

### Net Structure Routing for DQ[63:0], DM[7:0], DQS[7:0], $\overline{\text{DQS}}[7:0]$ (Raw card A)



### Trace Lengths for DQ[63:0], DM[7:0], DQS[7:0], $\overline{\text{DQS}}[7:0]$ (Raw card A)

Raw card A	TL0A Micro-Strip		TL0B Micro-Strip		TL1 Strip		TL2 Micro-Strip		Compensated Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ0-DQ7, DM0, DQS0, $\overline{\text{DQS}}0$	2.7	3.6	0.6	2.0	7.5	8.8	0.5	0.7	12.5	12.6	1,2, 3, 4, 5
DQ8-DQ15, DM1, DQS1, $\overline{\text{DQS}}1$	2.1	2.5	1.4	2.4	6.3	8.5	0.5	2.5	12.3	12.4	1,2, 3, 4, 5
DQ16-DQ23, DM2, DQS2, $\overline{\text{DQS}}2$	2.8	3.4	0.6	2.8	7.3	8.6	0.5	0.7	12.4	12.5	1,2, 3, 4, 5
DQ24-DQ31, DM3, DQS3, $\overline{\text{DQS}}3$	2.1	2.5	0.8	2.4	8.2	9.3	0.5	0.7	12.7	12.8	1,2, 3, 4, 5

1. All distances are given in millimeters.
2. Trace width/spacing : DQ, DM: 0.075/minimum 0.25, DQS,  $\overline{\text{DQS}}$ : 0.075/0.1, DQS/ $\overline{\text{DQS}}$  and other spacing is minimum 0.25
3. Micro-strip line must be compensated as Equivalent Stripline Length = Microstrip Length / 1.1
4. Compensated Total is TL0A + TL0B + TL1 + TL2 in equivalent stripline length.

### Trace Lengths for DQ[63:0], DM[7:0], DQS[7:0], $\overline{\text{DQS}}$ [7:0] (Raw card A)

Raw card A	TL0A Micro-Strip		TL0B Micro-Strip		TL1 Strip		TL2 Micro-Strip		Compensated Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQ32- DQ39, DM4, DQS4, $\overline{\text{DQS}}$ 4	2.1	2.5	1.3	2.2	6.3	8.3	0.5	2.6	12.0	12.1	1, 2, 3, 4, 5
DQ40- DQ47, DM5, DQS5, $\overline{\text{DQS}}$ 5	2.8	3.9	0.7	3.3	5.5	8.2	0.5	0.7	12.0	12.1	1, 2, 3, 4, 5
DQ48- DQ55, DM6, DQS6, $\overline{\text{DQS}}$ 6	2.2	2.9	0.8	2.7	7.5	9.5	0.5	0.7	13.0	13.1	1, 2, 3, 4, 5
DQ56- DQ63, DM7, DQS7, $\overline{\text{DQS}}$ 7	2.8	3.5	0.6	1.9	7.8	9.2	0.5	0.7	12.9	13.0	1, 2, 3, 4, 5

1. All distances are given in millimeters.
2. Trace width/spacing : DQ, DM: 0.075/minimum 0.25, DQS,  $\overline{\text{DQS}}$ : 0.075/0.1, DQS/ $\overline{\text{DQS}}$  and other spacing is minimum 0.25
3. Micro-strip line must be compensated as Equivalent Stripline Length = Microstrip Length / 1.1
4. Compensated Total is TL0A + TL0B + TL1 + TL2 in equivalent stripline length.

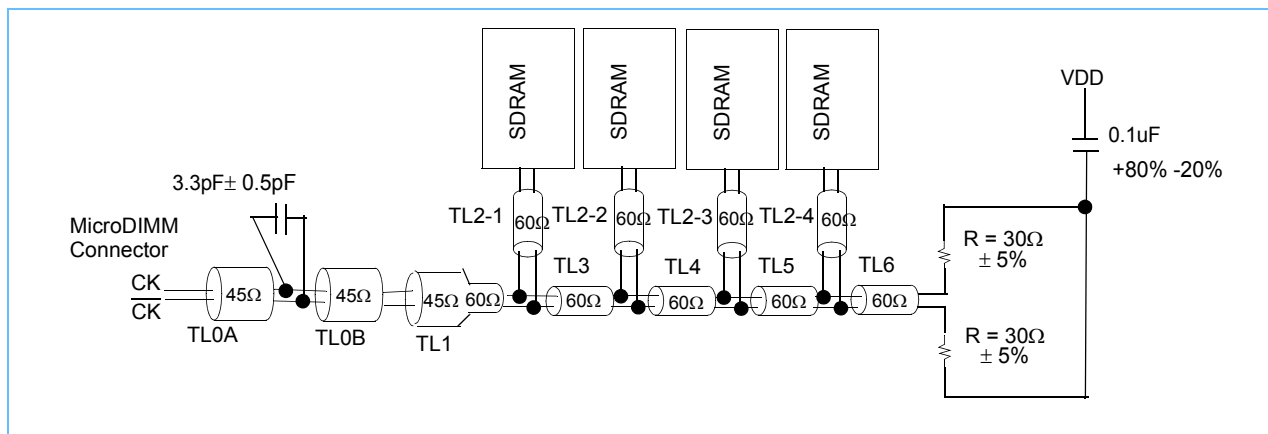
## Differential Clock Net Structures

### CK[1:0], $\overline{\text{CK}}[1:0]$

DDR3 SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair in the SDRAM
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 2.54mm total) between clocks of the same function

### Clock Net Wiring (Raw card A)



### Trace Lengths for Clock Routing (Raw card A)

Raw card A	TL0A Micro-Strip		TL0B Micro-strip		TL1 Strip		TL2 Micro-Strip		TL3 Strip		TL4 Strip		TL5 Strip		TL6 Strip/Micro-Strip Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	1.6	1.7	27.3	27.4	40.3	40.4	1.6	1.7	13.5	13.6	18.6	18.7	13.5	13.6	10.4	10.5	1, 2

1. All distances are given in millimeters.
2. Trace width/spacing : CK,  $\overline{\text{CK}}$  : 0.15/0.1(45Ω), 0.075/0.1(60Ω), CK and other spacing: minimum 0.25
3. Ck1,  $\overline{\text{CK}}1$  are terminated with 75ohm resistor near card edge on R/C A.

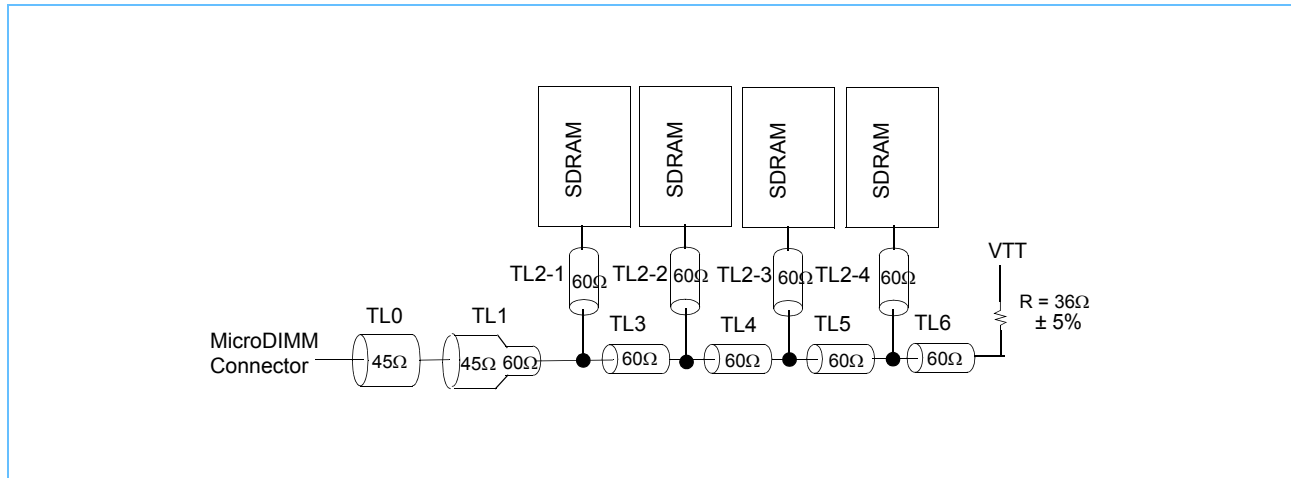
### Trace Lengths Detail for Clock(Raw card A)

Neckdown length on TL1		Compensated length TL0A+TL0B+TL1+TL2-1		Compensated length TL0A+TL0B+TL1+TL3+TL2-2		Compensated length TL0A+TL0B+TL1+TL3+TL4+TL2-3		Compensated length TL0A+TL0B+TL1+TL3+TL4+TL5+TL2-4		Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6.9	7.1	68.1	68.2	81.6	81.7	100.2	100.3	113.7	113.8	1, 2, 3

1. Neckdown length is the length of (60Ω)part of TL1
2. Compensated length is the equivalent stripline length.
3. Micro-strip line must be compensated as Equivalent Stripline Length = Microstrip Length / 1.1

**Control Net Structures  $\overline{S}$  [1:0],  $\overline{CKE}$ [1:0],  $\overline{ODT}$ [1:0] (Raw cards A)**

**Net Structure Routing for Control Net Structures  $\overline{S}$  [1:0],  $\overline{CKE}$ [1:0],  $\overline{ODT}$ [1:0] (Raw cards A)**



**Trace Lengths for Control Net Structures  $\overline{S}$  [1:0],  $\overline{CKE}$ [1:0],  $\overline{ODT}$ [1:0] (Raw card A)**

Raw card A	TL0 Micro-Strip		TL1 Strip		TL2 Micro-Strip		TL3 Strip		TL4 Strip		TL5 Strip		TL6 Strip/Micro-Strip Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	23.3	65.0	8.5	46.5	0.5	0.7	13.4	13.6	18.5	18.7	13.4	13.6	2.8	11.2	1, 2

1. All distances are given in millimeters
2. Trace width/spacing : 0.15/minimum 0.15(45Ω), 0.075/minimum 0.15(60Ω)
3.  $\overline{S}$ 1,  $\overline{CKE}$ 1,  $\overline{ODT}$ 1 are not connected on R/C A

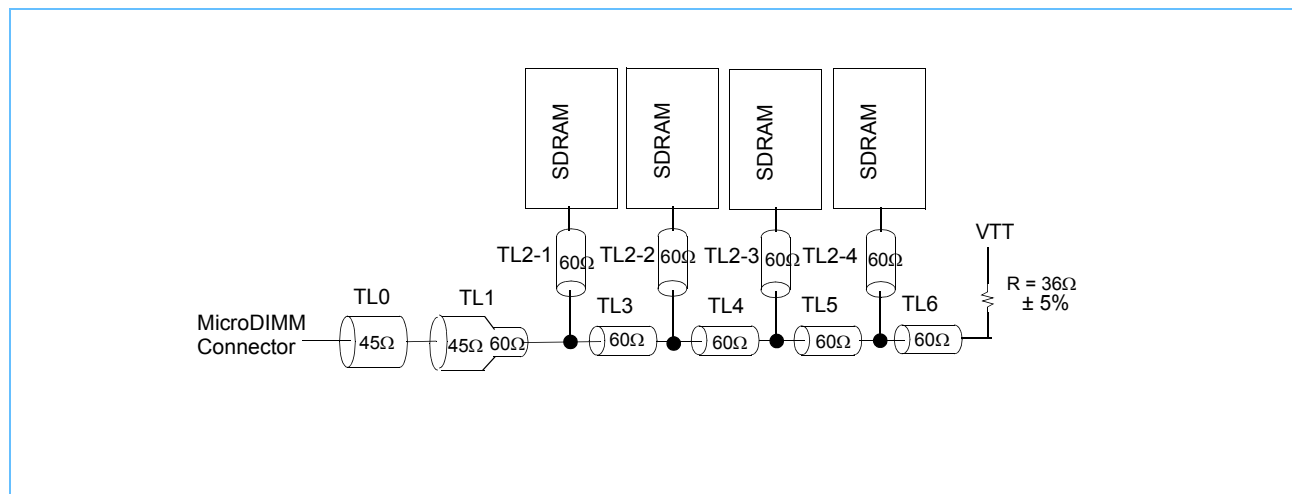
**Trace Lengths Detail for Control Net Structure (Raw card A)**

	Neckdown length on TL1		Compensated length TL0+TL1+TL2-1		Compensated length TL0+TL1+TL3+TL2-2		Compensated length TL0+TL1+TL3+TL4+TL2-3		Compensated length TL0+TL1+TL3+TL4+TL5+TL2-4		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	6.9	7.1	68.0	68.2	81.5	81.7	100.1	100.3	113.6	113.8	1, 2,3

1. Neckdown length is the length of (60Ω)part of TL1
2. Compensated length is the equivalent stripline length.
3. Micro-strip line must be compensated as Equivalent Stripline Length = Microstrip Length / 1.1

## Address/Control Net Structures Ax, BAx, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ (Raw card A)

### Net Structure Routing for Address/Control Net Structures Ax, BAx, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ (Raw card A)



### Trace Lengths for Address/Command Net Structures Ax, BAx, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ (Raw card A)

Raw card A	TL0 Micro-Strip		TL1 Strip		TL2 Micro-Strip		TL3 Strip		TL4 Strip		TL5 Strip		TL6 Strip/Micro-Strip Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
	23.4	65.9	7.5	46.1	0.5	0.9	13.4	13.6	18.5	18.7	13.4	13.6	5.8	10.7	1

- All distances are given in millimeters
- Trace width/spacing : 0.15/minimum 0.15(45Ω), 0.075/minimum 0.15(60Ω)

### Trace Lengths Detail for Address/Command (Raw card A)

Neckdown length on TL1		Compensated length TL0+TL1+TL2-1		Compensated length TL0+TL1+TL3+TL2-2		Compensated length TL0+TL1+TL3+TL4+TL2-3		Compensated length TL0+TL1+TL3+TL4+TL5+TL2-4		Notes
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
6.9	7.1	68.0	68.2	81.5	81.7	100.1	100.3	113.6	113.8	1, 2, 3

- Neckdown length is the length of (60Ω) part of TL1
- Compensation length is the equivalent stripline length.
- Micro-strip line must be compensated as Equivalent Stripline Length = Microstrip Length / 1.1

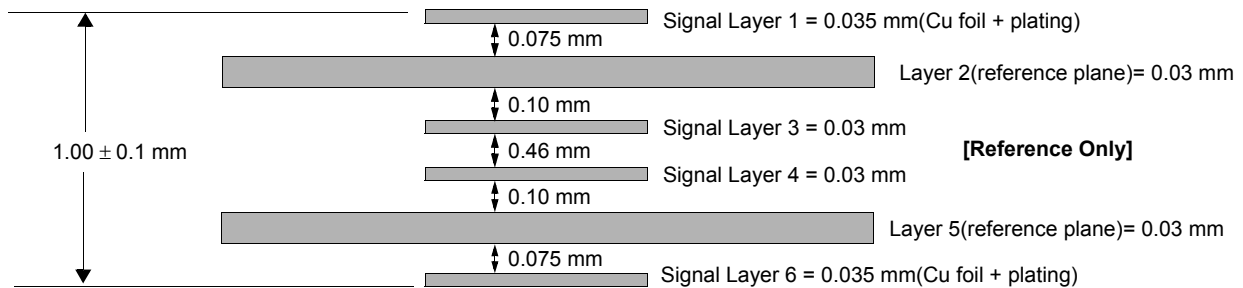
## PCB Electrical Specifications

The DDR3 MicroDIMM printed circuit board design uses multi-layers of glass epoxy material. It shall have the reference planes to form the signal traces(except low speed signals such as SMBus) the transmission lines. The reference planes can be divided so adjacent signal layers maintain a constant Vss or Vdd reference. All data is referenced to Vss and all address/command and clocks are referenced to Vdd.

Parameter	Min	Typ	Max	Units
Trace velocity: S0 (outer layers)	5.5	-	6.7	ps/mm
Trace velocity: S0 (inner layers)	6.5	-	7.6	ps/mm
Trace impedance: Z0 (W=0.075mm traces in gerber, all layers)	54	60	66	Ohms

Note: PCB manufacturers must adjust the trace widths and/or stackup(example below) to achieve the required parameters above.

### Cross Section example.



### Other trace impedance reference values

Parameter	Min	Typ	Max	Units
Trace impedance: Z0 (W=0.15mm traces in design, all layers)	40.5	45	49.5	Ohms
Trace impedance: Zdiff (W/S=0.15mm/0.1mm traces in design, all layers)	57.8	68	78.2	Ohms
Trace impedance: Zdiff (W/S=0.075mm/0.1mm traces in design, all layers)	74.8	88	101.2	Ohms

- All trace widths are subject to adjustment by PCB vendor, as required to align impedance targets.
- Target min/max values in this table are for reference only.



## 7. Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC3-12800 DDR3 SDRAM Unbuffered MicroDIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR3 SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices. **This section will be updated when Rev1.0 SPD spec defined.**

The following table is intended to be an **example** of a typical PC3-6400/8500 MicroDIMM. SPD values indicating different MicroDIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or MicroDIMMs. This example assumes:

- Module Organization: 512MB
- Device Composition: 64Mx16
- Device Package: FBGA
- Module Physical Ranks: 1
- CAS latency: 6

### Serial Presence Detect Data Example (Part 1 of 2)

Byte # (dec)	Byte # (hex)	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Notes
			DDR3- 800	DDR3- 1066	DDR3- 800	DDR3- 1066	
0	00	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	SPD : 128bytes, CRC : 116bytes		81		1, 2
1	01	SPD Revision	1.0		10		
2	02	Key Byte / DRAM Device Type	DDR3 SDRAM		0B		
3	03	Key Byte / Module Type	MicroDIMM		04		
4	04	SDRAM Density and Banks	8banks, 1Gb		02		3
5	05	SDRAM Addressing	Row:14, Clm: 10		09		3
6	06	Reserved					
7	07	Module Organization	1R, x16		02		3
8	08	Module Memory Bus Width	64bits		03		
9	09	Fine Timebase Dividend and Divisor					
10	0A	Medium Timebase Dividend					
11	0B	Medium Timebase Divisor					
12	0C	SDRAM Minimum Cycle Time (tCKmin)					3
13	0D	Reserved					
14	0E	CAS Latencies Supported, Least Significant Byte					3
15	0F	CAS Latencies Supported, Most Significant Byte					3
16	10	Minimum CAS Latency Time (tAamin)					3
17	11	Minimum Write Recovery Time (tWRmin)					3
18	12	Minimum RAS# to CAS# Delay Time (tRCDmin)					3

1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes.
2. Size of SPD device will typically be programmed as 256 bytes.
3. From DDR3 SDRAM datasheet.
4. These are optional, in accordance with the JEDEC spec.

**Serial Presence Detect Data Example** (Part 2 of 2)

Byte # (dec)	Byte # (hex)	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Notes
			DDR3- 800	DDR3- 1066	DDR3- 800	DDR3- 1066	
19	13	Minimum Row Active to Row Active Delay Time (tRRDmin)					3
20	14	Minimum Row Precharge Time (tRPmin)					3
21	15	Upper Nibbles for tRAS and tRC					3
22	16	Minimum Active to Precharge Time (tRASmin), Least Significant Byte					3
23	17	Minimum Active to Active/Refresh Time (tRCmin), Least Significant Byte					3
24	18	Minimum Refresh Recovery Time (tRFCmin), Least Significant Byte					3
25	19	Minimum Refresh Recovery Time (tRFCmin), Most Significant Byte					3
26	1A	Minimum Internal Write to Read Command Delay Time (tWTRmin)					3
27	1B	Minimum Internal Read to Precharge Command Delay Time (tWTRmin)					3
28	1C	Upper Nibble for tFAW					3
29	1D	Minimum Four Activate Window Delay Time (tFAW-min)					3
30	1E	SDRAM Output Drivers supported					3
31	1F	SDRAM Refresh Options					3
32-59		TBD, General Section					
60		Module Nominal Height	30.0		0E		
61		Module Maximum Thickness	3.8		11		
62		Reference Raw Card Used	Raw Card A		00		
63		Address Mapping from Edge Connector to DRAM	Standard		00		
64-116		Reserved(Unbuffered)					
117-118	22	Module ID: Module Manufacturer's JEDEC ID Code					
119	23	Module ID: Module Manufacturing Location					
120-121	24	Module ID: Module Manufacturing Date					
122-125	25	Module ID: Module Serial Number					
126-127	26	Cyclical Redundancy Code	CRC		CRC		
128-145	27	Module Part Number					4
146-147	28	Module Revision Code					4
148-149	29	DRAM Manufacturer's JEDEC ID Code					4
150-175	2A	Manufacturer's Specific Data					4
176-255	2B	Open for customer use					

1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes.  
2. Size of SPD device will typically be programmed as 256 bytes.  
3. From DDR3 SDRAM datasheet.  
4. These are optional, in accordance with the JEDEC spec.

## 8. Product Label

### DDR3 "End-User" DIMM Label Format:

The following label shall be applied to all DDR3 memory modules targeted at end-user type products to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggggg, are to be omitted when not needed.

ggggg eRxff PC3-wwwwwm-aa-bb-ccd

### Where:

- ggggg = Module total capacity, in bytes  
256MB, 512MB, 1GB, 2GB, 4GB, etc.
- eR = Number of ranks of memory installed  
1R = 1 rank of DDR3 SDRAM installed  
2R = 2 ranks  
4R = 4 ranks
- xff = Device organization (bit width) of DDR3 SDRAMs used on this assembly  
x4 = x4 organization (4 DQ lines per SDRAM)  
x8 = x8 organization  
x16 = x16 organization
- wwwww = Module bandwidth in MB/s  
6400 = 6.40 GB/s (PC3-800 SDRAMs, 8 byte primary data bus)  
8500 = 8.53 GB/s (PC3-1066 SDRAMs, 8 byte primary data bus)  
10600 = 10.66 GB/s (PC3-1333 SDRAMs, 8 byte primary data bus)  
12800 = 12.80 GB/s (PC3-1600 SDRAMs, 8 byte primary data bus)
- m = Module Type  
E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)  
F = Fully Buffered DIMM ("FB-DIMM")  
M = Micro-DIMM  
R = Registered DIMM ("RDIMM")  
S = Small Outline DIMM ("SO-DIMM")  
U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)
- aa = DDR3 SDRAM CAS Latency in clocks at maximum operating frequency
- bb = JEDEC SPD Revision Encoding and Additions level used on this DIMM
- cc = Reference design file used for this design (if applicable)  
A = Reference design for raw card 'A' is used for this assembly  
B = Reference design for raw card 'B' is used for this assembly  
AV = Reference design for raw card 'AV' is used for this assembly  
ZZ = None of the reference designs were used for this assembly
- d = Revision number of the reference design used  
0 = Initial release  
1 = First revision  
2 = Second revision  
P = Pre-release or Engineering sample  
Z = To be used when field cc = ZZ

**Example:**

512MB 1Rx16 PC3-10600M-7-10-D2

is a 512 MB DDR3 Micro-DIMM using 1 rank of x16 SDRAMs operational to DDR3-1333 performance with CAS Latency = 7 using JEDEC DDR3 SPD revision 1.0, raw card reference design file D revision 2 used for the assembly

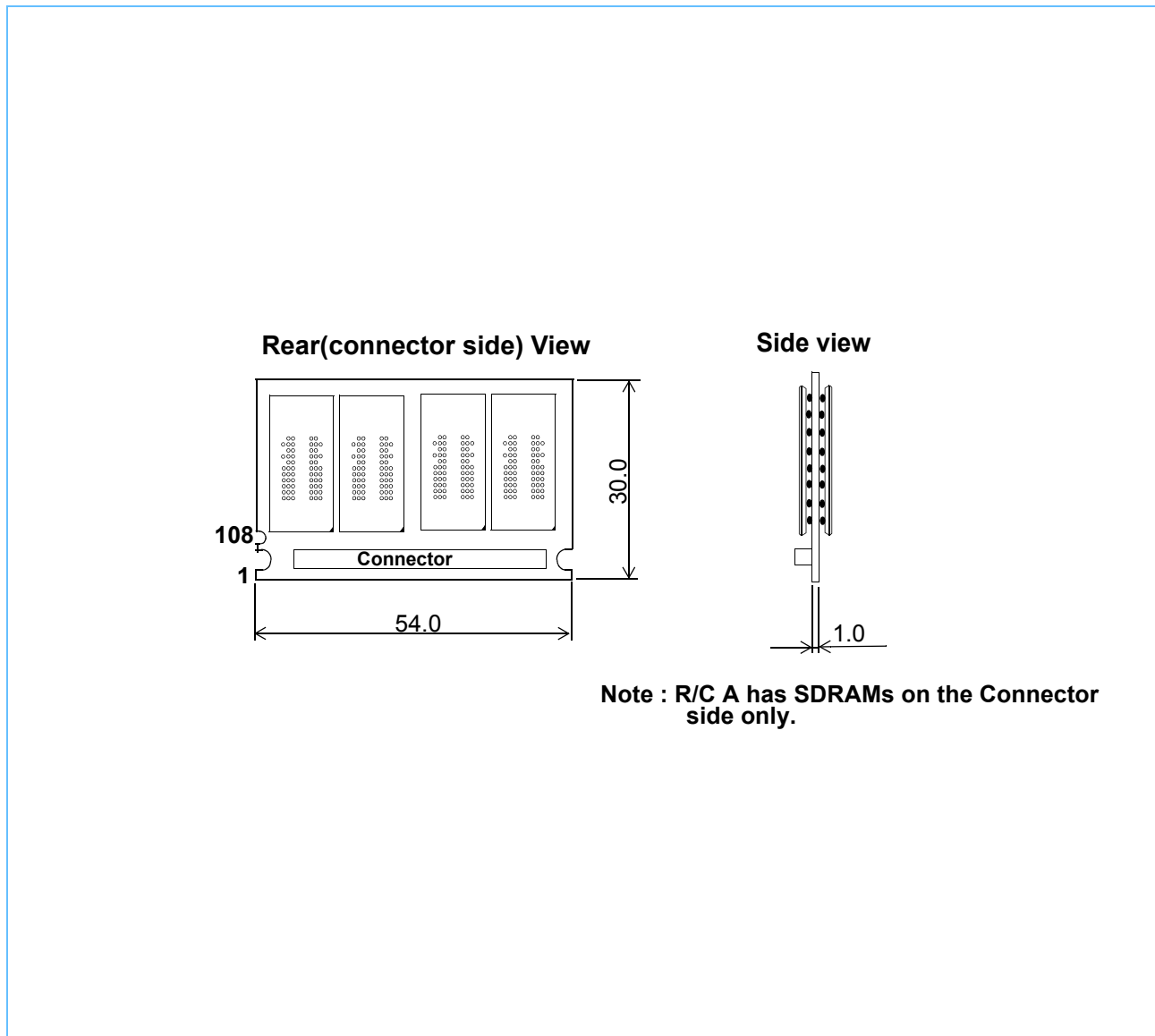
## 9. MicroDIMM Mechanical Specifications

JEDEC is standardizing detailed mechanical information for the 214 Pin DIMM family. This information can be accessed on the worldwide web as follows after standardization is completed.

1. Go to <http://www.jedec.org>.
2. Click on 'Free Standards' --> 'JEP95 MAIN PAGE' --> 'Microelec. Outlines'
3. Scroll down and select 'MO-260' to download the PDF for this product family.
4. Or you can search this document from 'Free Standards' top page.

This example is for reference only; please refer to JEDEC standard MO-260 variation-C for details.

### Reference Simplified Mechanical Drawing



## Revision History:

Date	Rev.	Page	Changes
Oct/2005	0.01		Initial draft.
May/2006	0.1	All	Update
28/June/2006	0.11	All	Update
11/July/2006	0.12	10	Added thermal sensor overvoltage requirement
		15-19	Updated trace length for the gerber Rev0.1
18/July/2006	0.13	22, 23	Updated SPD section
28/July/2006	0.3	8, 15,16,18, 19	Corrected DQ stub resistor value from 22ohm to 15ohm Corrected Rtt value for adr/cmd/ctrl/ck+/- from 39ohm to 36ohm
		18, 19	Corrected topology picture
04/August/2006	0.31	15	Added Length matching Rules
		16-20	Moved Data nets to the top of net structure section
		16-20	Added trace width/spacing at the note of trace length tables.
		16, 17	Added via compensation value
		18-20	Corrected leadin impedance from 40 to 45 ohm
		21	Updated PCB Electrical Specifications
10/August/2006	0.32	8	Re-drew the block diagram with Frame Maker's graphic capability
		13, 27	Updated outline with upper notch at left/right to one side only
		15	Added DQS/DQ/DM length matching rule
		21	Updated target trace impedances
		25	Changed cc example including raw card A, B
25/October/2006	0.33	16-18	Quoted trace routing and decoupling guidelines from SO-DIMM spec
		19	Changed CK Cterm 2.2 to 3.3pF, Rtt 36 to 30ohm to be consist with SO-DIMM spec
		24	Changed trace impedance requirement to be consist with SO-DIMM spec
		30	Added variation number "C" to MO-260
		5, 6, 8, 10	Deleted "BA3"
12/December/2006	0.34	14	Corrected MO-260 variation to C
		21	Corrected termination resistor value for unused clock to 75ohm
		24	Made notes for Cross Section Example clearer
		28, 29	Corrected DIMM label section