

**4.20.9 - 100-Pin DDR SDRAM Unbuffered 32b-DIMM Design  
Specification**

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**DDR SDRAM Unbuffered 32b-DIMM  
Reference Design Specification**

Revision 1.1

Updated February 24, 2004

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## 1. Product Description

This reference specification defines the electrical and mechanical requirements for the 32b-DIMM DDR module. This is a 100-pin module supporting 100MHz, 133MHz, and 167Mhz clock (200, 266, 333 MT/s data rate) Double Data Rate (DDR) Synchronous DRAM. The data bus is 32-bits wide with no ECC support and the address is unbuffered. The 32b-DIMM DDR module is intended for use in embedded applications.

Reference design examples are included which provide an initial basis for 32b-DIMM designs. Any modifications to these reference designs must meet all system timing, signal integrity and thermal requirements for 167 MHz clock rate support. Other designs are acceptable, and all 32b-DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

### Product Family Attributes

Attribute:	Values:	Notes:
32b-DIMM Organization	x 32,	
32b-DIMM Dimensions (nominal)	30.48 mm high, 90.19 mm wide for raw card B, C and E 25.4 mm high, 90.19 mm wide for raw card A and D	
32b-DIMM Types Supported	Unbuffered	
Pin Count	100	
DDR SDRAMs Supported	64 Mb, 128 Mb, 256 Mb, 512 Mb	
Capacity	32 MB, 64 MB, 128 MB, 256 MB, 512 MB	
Serial Presence Detect	Consistent with JEDEC 21-C Appendix D Release 11	
Voltage Options	2.5 V $V_{DD}$ 2.5 V $V_{DDQ}$	1
Interface	SSTL_2	
Note 1: $V_{DD}SPD$ is tied to $V_{DD}$ or $V_{DDQ}$ on the DDR 32b-DIMM .		

## 2. Environmental Requirements

DDR SDRAM unbuffered 32b-DIMMs are intended for standard office environments that have limited capability for heating and air conditioning.

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
T <sub>OPR</sub>	Operating Temperature (ambient)	0 to +65	°C	1
H <sub>OPR</sub>	Operating Humidity (relative)	10 to 90	%	1
T <sub>STG</sub>	Storage Temperature	-50 to +100	°C	1
H <sub>STG</sub>	Storage Humidity (without condensation)	5 to 95	%	1
	Barometric Pressure (operating & storage)	105 to 69	kPa	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

### 3. Architecture

#### Pin Description

CK(0:1)	Clock Inputs, positive line	2	DQ(0:31)	Data Input/Output	32
$\overline{\text{CK}}$ (0:1)	Clock inputs, negative line	2			
CKE(0:1)	Clock Enables	2	DM(0:3)	Data Masks	4
$\overline{\text{RAS}}$	Row Address Strobe	1	DQS(0:3)	Data strobes	4
$\overline{\text{CAS}}$	Column Address Strobe	1			
$\overline{\text{WE}}$	Write Enable	1			
$\overline{\text{S}}$ (0:1)	Chip Selects	2	V <sub>DD</sub>	Core and I/O Power	14
A(0:9,11:13)	Address Inputs	13	V <sub>SS</sub>	Ground	14
A10/AP	Address Input/Autoprecharge	1	V <sub>REF</sub>	Input/Output Reference	1
BA(0:1)	SDRAM Bank Address	2			
SCL	Serial Presence Detect (SPD) Clock Input	1			
SDA	SPD Data Input/Output	1			
SA0	SPD address	1	DU	Reserved for future use	1
					<b>Total: 100</b>

## Input/Output Functional Description

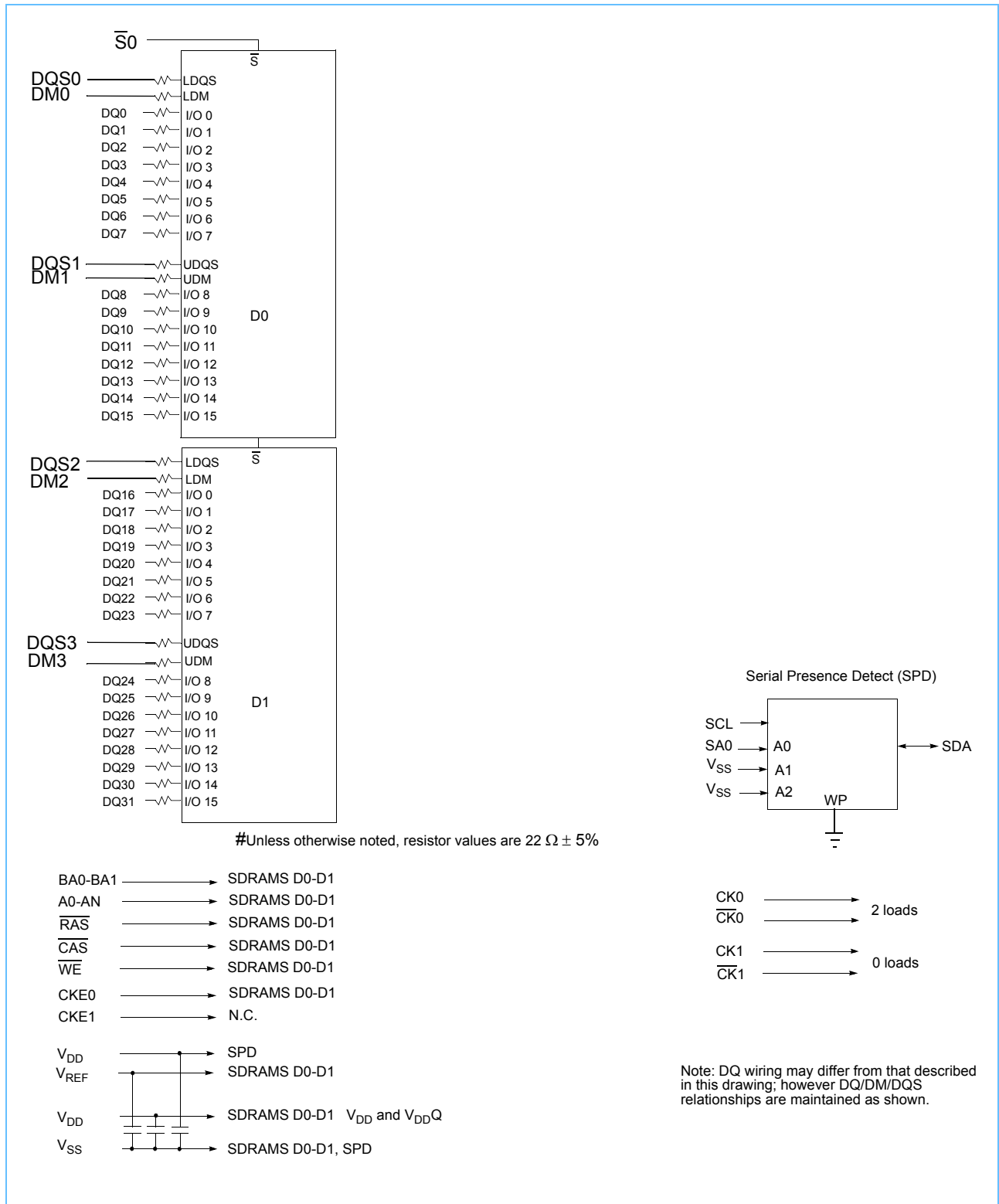
Symbol	Type	Polarity	Function
CK0 - CK1, $\overline{\text{CK0}} - \overline{\text{CK1}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	Input	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{\text{S0}}$ ; Bank 1 is selected by $\overline{\text{S1}}$ .
$\overline{\text{RAS}}, \overline{\text{CAS}},$ $\overline{\text{WE}}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ , $\overline{\text{CAS}}$ , $\overline{\text{RAS}}$ , and $\overline{\text{WE}}$ define the operation to be executed by the DDR SDRAM.
BA0 - BA1	Input	—	Selects which DDR SDRAM bank of four is activated.
A0 - A9, A11-A13 A10/AP	Input	—	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$ . In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ31	In/Out	—	Data Bit Input/Output pins.
DM0 - DM3	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 - DQS3	In/Out	—	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window.
V <sub>DD</sub> , V <sub>SS</sub>	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	In/Out	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V <sub>DD</sub> to act as a pull up.
SCL	Input	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V <sub>DD</sub> to act as a pull up.
SA0	Input	—	Address pin used to select the Serial Presence Detect.

### DDR SDRAM 32b-DIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	DQ0	51	DQ4	26	A5	76	A2
2	V <sub>SS</sub>	52	V <sub>SS</sub>	27	A3	77	A0
3	DQ1	53	DQ5	28	A1	78	BA1
4	DQS0	54	DM0	29	A10	79	$\overline{\text{RAS}}$
5	V <sub>DD</sub>	55	V <sub>DD</sub>	30	V <sub>DD</sub>	80	V <sub>DD</sub>
6	DQ2	56	DQ6	31	BA0	81	$\overline{\text{CAS}}$
7	DQ3	57	DQ7	32	$\overline{\text{WE}}$	82	$\overline{\text{S1}}$
8	V <sub>DD</sub>	58	V <sub>DD</sub>	33	$\overline{\text{S0}}$	83	A13
9	DQ8	59	DQ12	34	DQ16	84	DQ20
10	DQ9	60	DQ13	35	V <sub>SS</sub>	85	V <sub>SS</sub>
11	V <sub>SS</sub>	61	V <sub>SS</sub>	36	DQ17	86	DQ21
12	DQS1	62	DM1	37	DQS2	87	DM2
13	DQ10	63	DQ14	38	V <sub>DD</sub>	88	V <sub>DD</sub>
14	V <sub>DD</sub>	64	V <sub>DD</sub>	39	DQ18	89	DQ22
15	DQ11	65	DQ15	40	DQ19	90	DQ23
16	V <sub>SS</sub>	66	V <sub>SS</sub>	41	V <sub>DD</sub>	91	V <sub>DD</sub>
17	CK0	67	CK1	42	DQ24	92	DQ28
18	$\overline{\text{CK0}}$	68	$\overline{\text{CK1}}$	43	DQ25	93	DQ29
19	V <sub>DD</sub>	69	V <sub>DD</sub>	44	V <sub>SS</sub>	94	V <sub>SS</sub>
20	CKE1	70	CKE0	45	DQS3	95	DM3
21	A12	71	A11	46	DQ26	96	DQ30
22	NC	72	A8	47	V <sub>SS</sub>	97	V <sub>SS</sub>
23	A9	73	A6	48	DQ27	98	DQ31
24	A7	74	A4	49	SA0	99	SDA
25	V <sub>SS</sub>	75	V <sub>SS</sub>	50	V <sub>REF</sub>	100	SCL

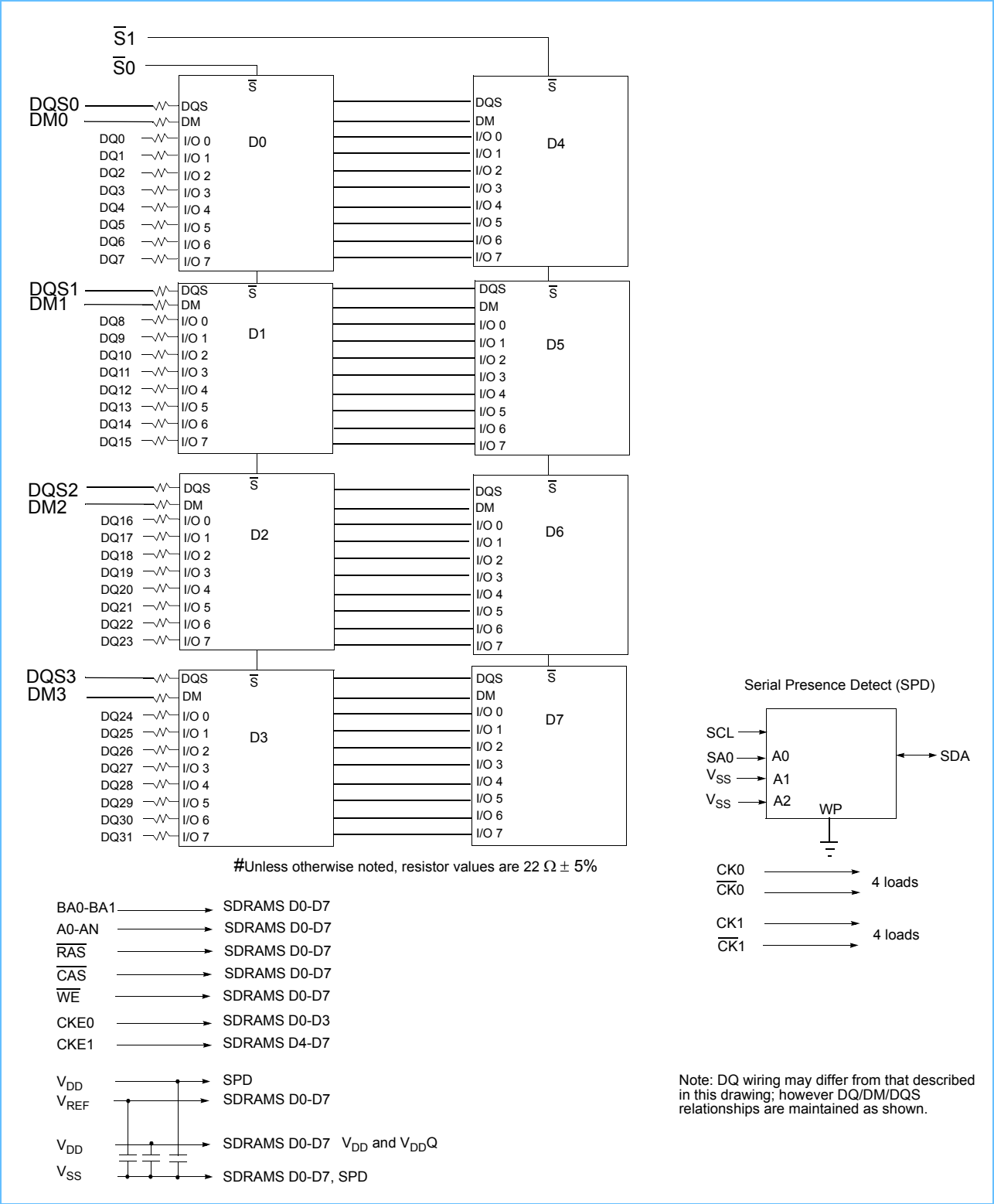
### Block Diagram: Raw Card Version A

(Populated as 1 physical bank of x16 DDR SDRAMs on a 6 layered PCB)



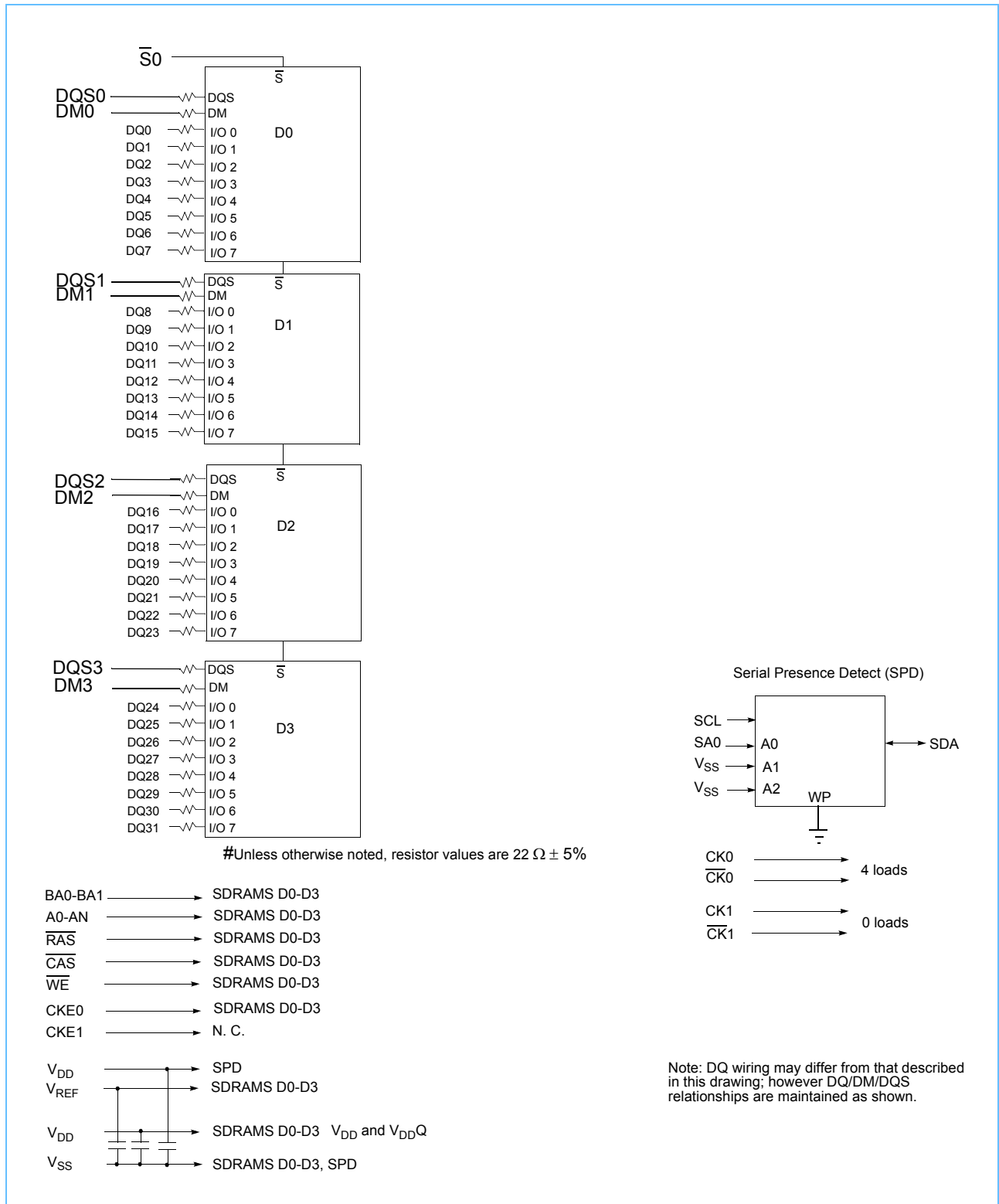
**Block Diagram: Raw Card Version B**

(Populated as 2 physical banks of x8 DDR SDRAMs on a 6 layered PCB)



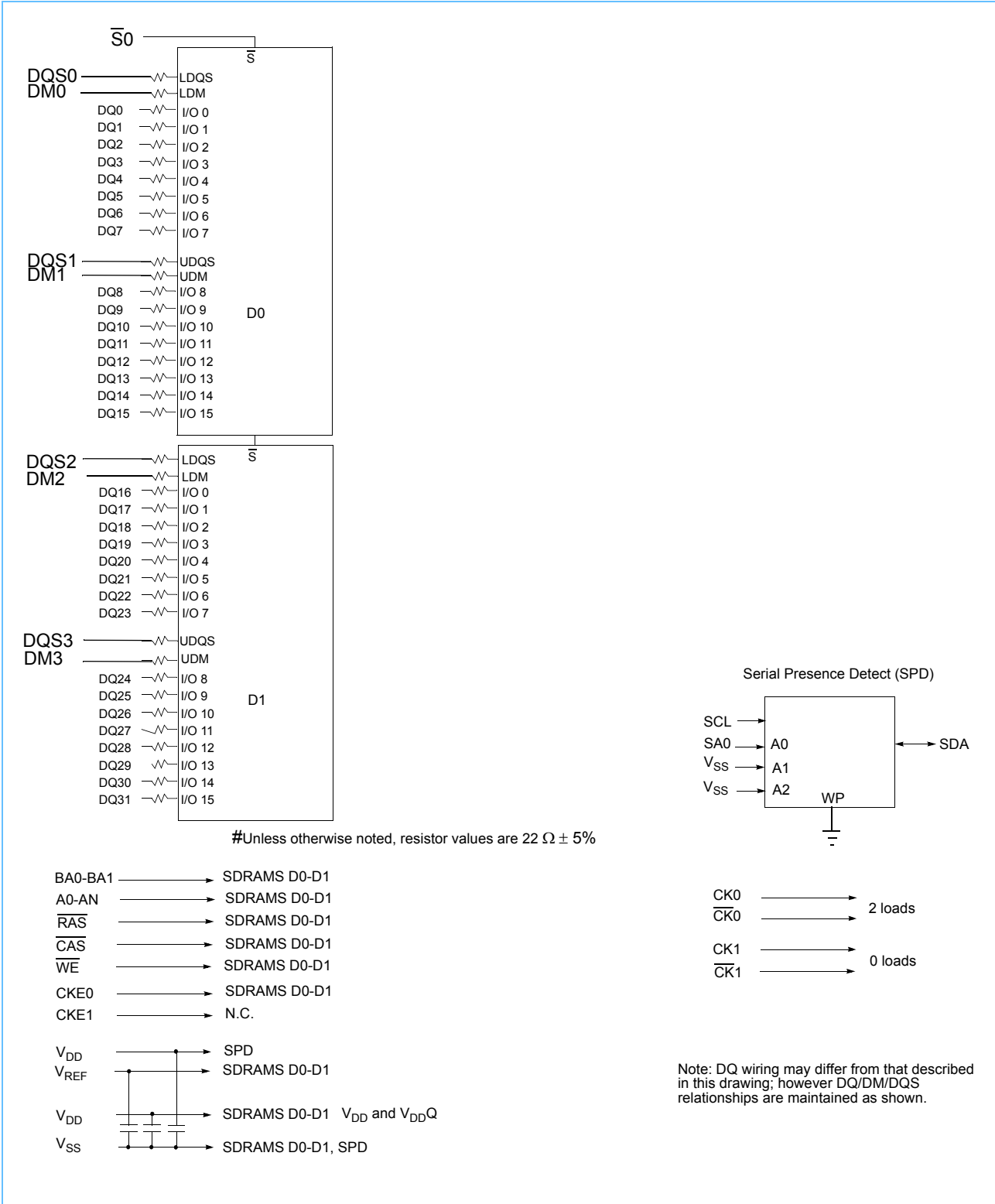
### Block Diagram: Raw Card Version C

(Populated as 1 physical bank of x8 DDR SDRAMs on a 6 layered PCB)



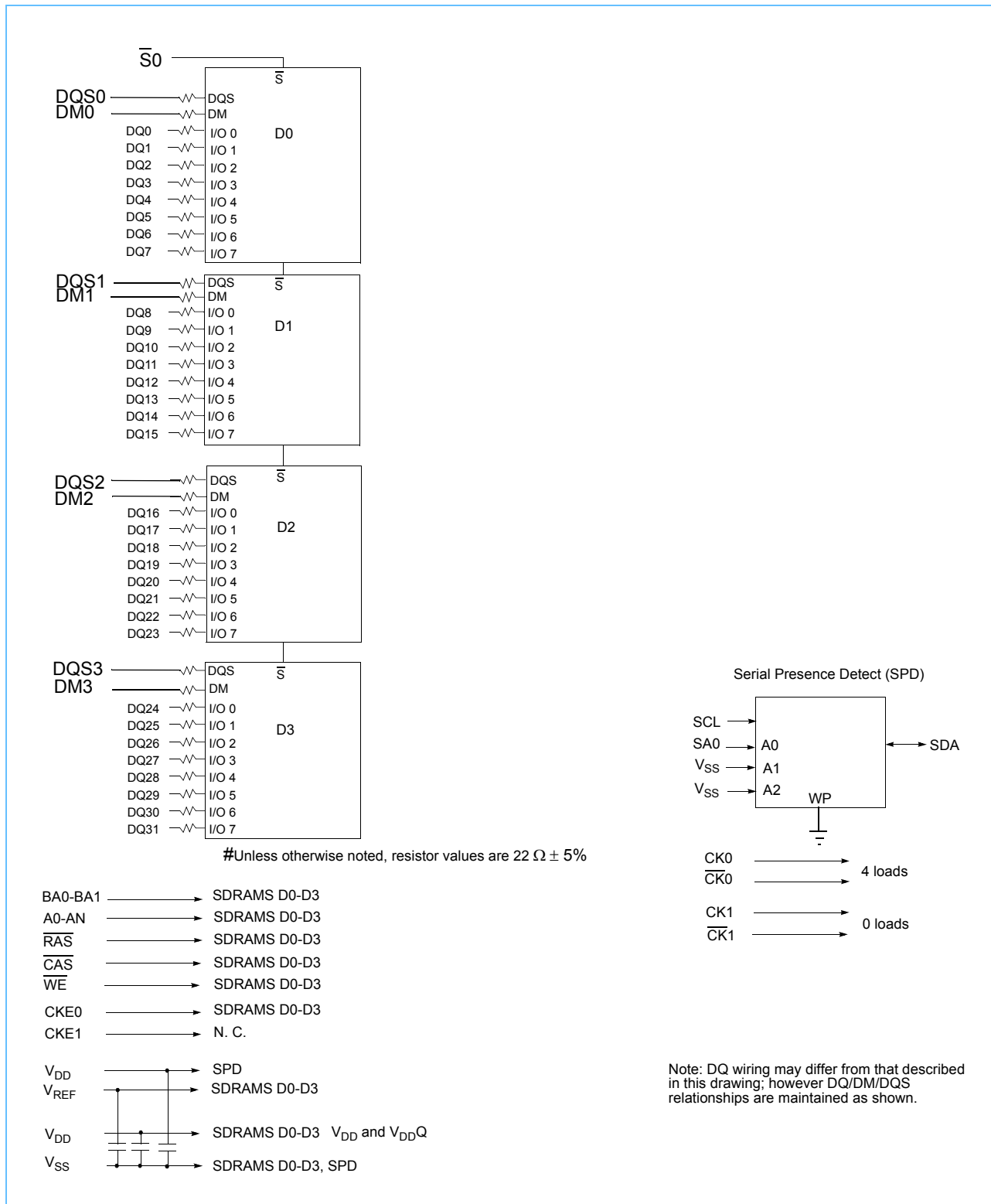
**Block Diagram: Raw Card Version D**

(Populated as 1 physical bank of x16 DDR SDRAMs on a 4 layered PCB)

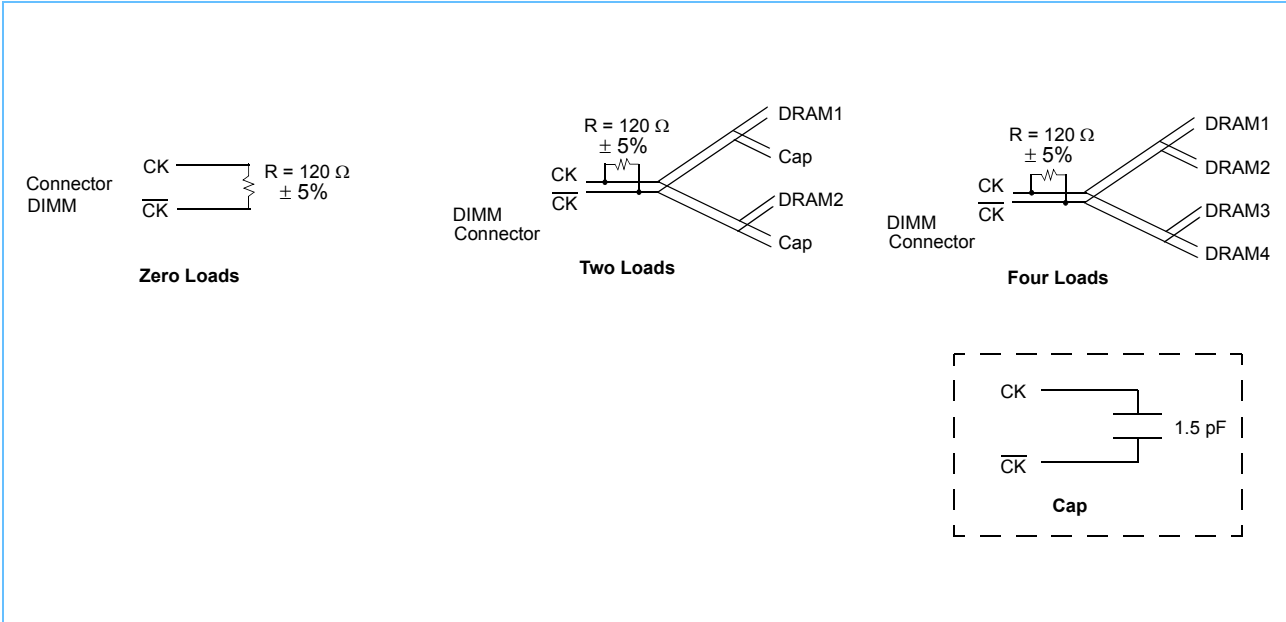


### Block Diagram: Raw Card Version E

(Populated as 1 physical bank of x8 DDR SDRAMs on a 4 layered PCB)

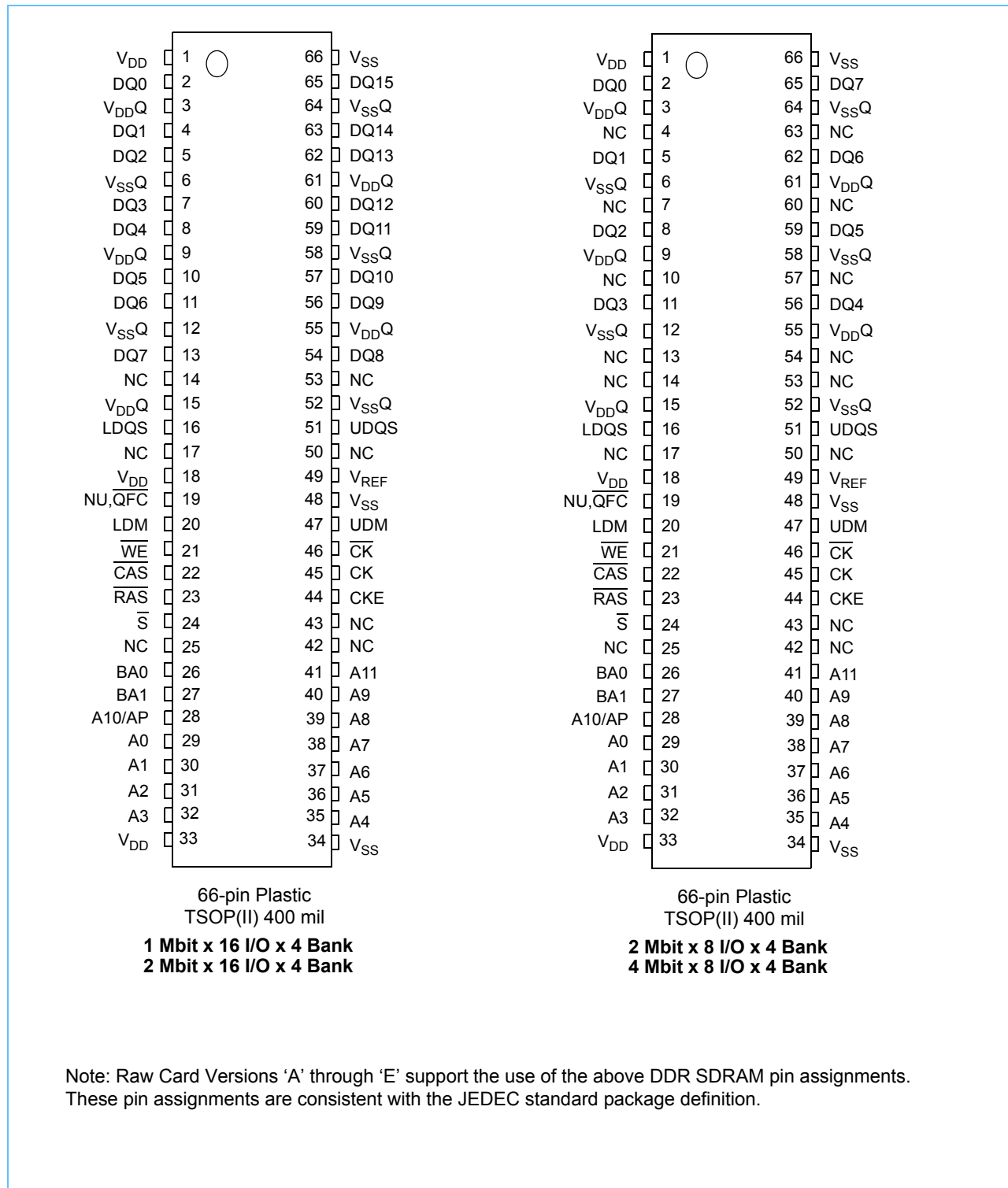


### Logical Clock Net Structures



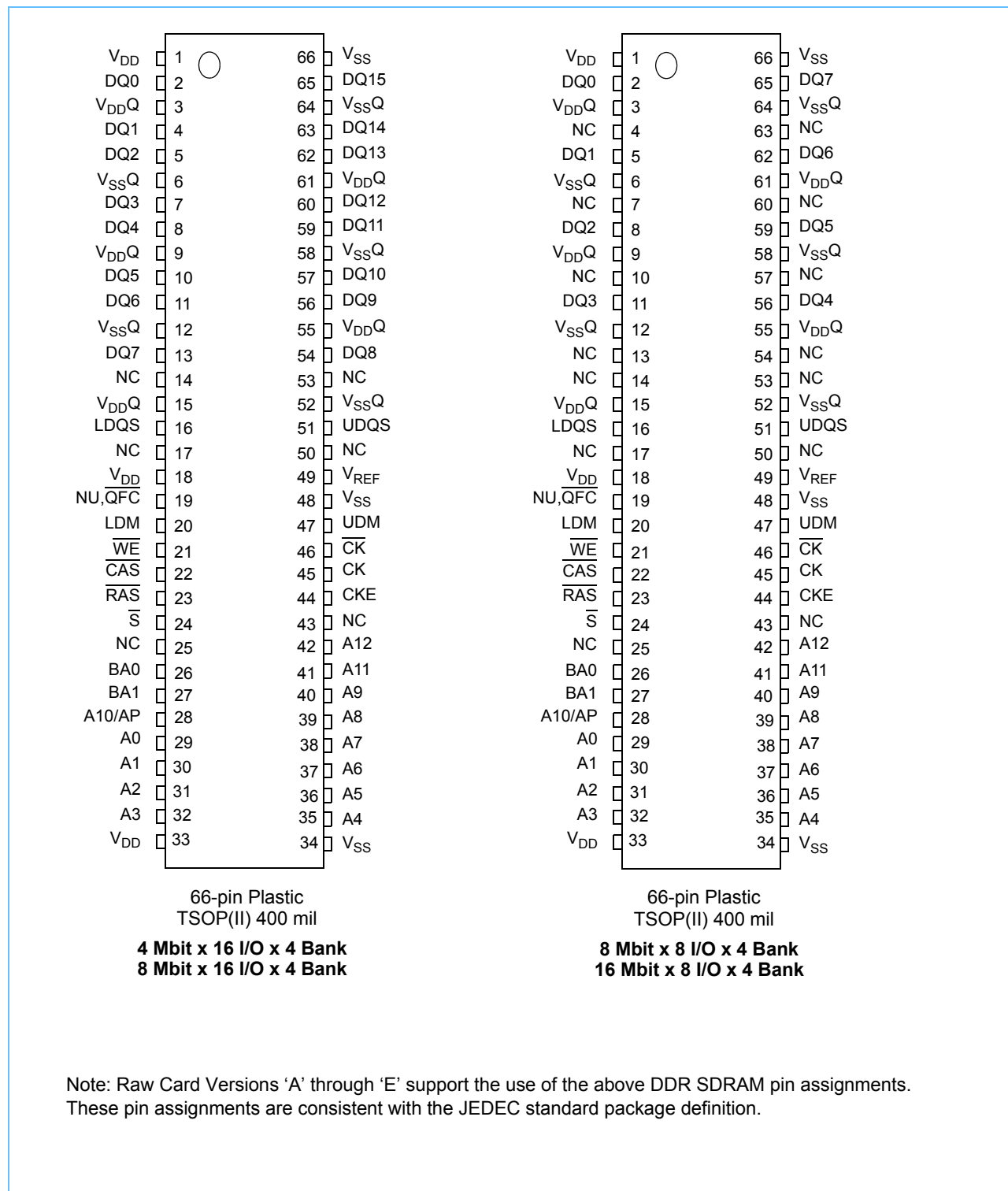
## 4. Component Details

### Pin Assignments for 64 Mb and 128 Mb DDR SDRAM Planar Components (Top View)



### Pin Assignments for 256 Mb and 512 Mb 66 pin DDR SDRAM Planar Components

(Top View)



## Reference DDR SDRAM Component Specifications

The DDR SDRAM components used with this 32 bit DIMM design specification are intended to be consistent with the latest revision of the JEDEC DDR333, DDR266 and DDR200 SDRAM specifications. Refer to standard JESD-79 for component details.

## Reference SPD Component Specifications

The Serial Presence Detect EEPROMs are powered off the 2.5 volt  $V_{DD}$  power supply. It does not have a separate supply..

## DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
$V_{DD}$	Core Supply Voltage	2.3	2.7	V

## 5. Unbuffered 32b-DIMM Details

### DDR SDRAM Module Configurations (Reference Designs)

Raw Card Version	32b-DIMM Capacity	32b-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
A	16 MB	4 M x 32	64 Mb	4 M x 16	2	66 lead TSOP	1	4	12/8
A	32 MB	8 M x 32	128 Mb	8 M x 16	2	66 lead TSOP	1	4	12/9
A	64 MB	16 M x 32	256 Mb	16 M x 16	2	66 lead TSOP	1	4	13/9
A	128 MB	32 M x 32	512 Mb	32 M x 16	2	66 lead TSOP	1	4	13/10

Raw Card Version	32b-DIMM Capacity	32b-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
B	64 MB	16 M x 32	64 Mb	8 M x 8	8	66 lead TSOP	2	4	12/9
B	128 MB	32 M x 32	128 Mb	16 M x 8	8	66 lead TSOP	2	4	12/10
B	256 MB	64 M x 32	256 Mb	32 M x 8	8	66 lead TSOP	2	4	13/10
B	512 MB	128 M x 32	512 Mb	64 M x 8	8	66 lead TSOP	2	4	13/11

Raw Card Version	32b-DIMM Capacity	32b-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
C	32 MB	8 M x 32	64 Mb	8 M x 8	4	66 lead TSOP	1	4	12/9
C	64 MB	16 M x 32	128 Mb	16 M x 8	4	66 lead TSOP	1	4	12/10
C	128 MB	32 M x 32	256 Mb	32 M x 8	4	66 lead TSOP	1	4	13/10
C	256 MB	64 M x 32	512 Mb	64 M x 8	4	66 lead TSOP	1	4	13/11

Raw Card Version	32b-DIMM Capacity	32b-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
D	16 MB	4 M x 32	64 Mb	4 M x 16	2	66 lead TSOP	1	4	12/8
D	32 MB	8 M x 32	128 Mb	8 M x 16	2	66 lead TSOP	1	4	12/9
D	64 MB	16 M x 32	256 Mb	16 M x 16	2	66 lead TSOP	1	4	13/9
D	128 MB	32 M x 32	512 Mb	32 M x 16	2	66 lead TSOP	1	4	13/10

Raw Card Version	32b-DIMM Capacity	32b-DIMM Organization	SDRAM Density	SDRAM Organization	# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# Address bits row/col
E	32 MB	8 M x 32	64 Mb	8 M x 8	4	66 lead TSOP	1	4	12/9
E	64 MB	16 M x 32	128 Mb	16 M x 8	4	66 lead TSOP	1	4	12/10
E	128 MB	32 M x 32	256 Mb	32 M x 8	4	66 lead TSOP	1	4	13/10
E	256 MB	64 M x 32	512 Mb	64 M x 8	4	66 lead TSOP	1	4	13/11

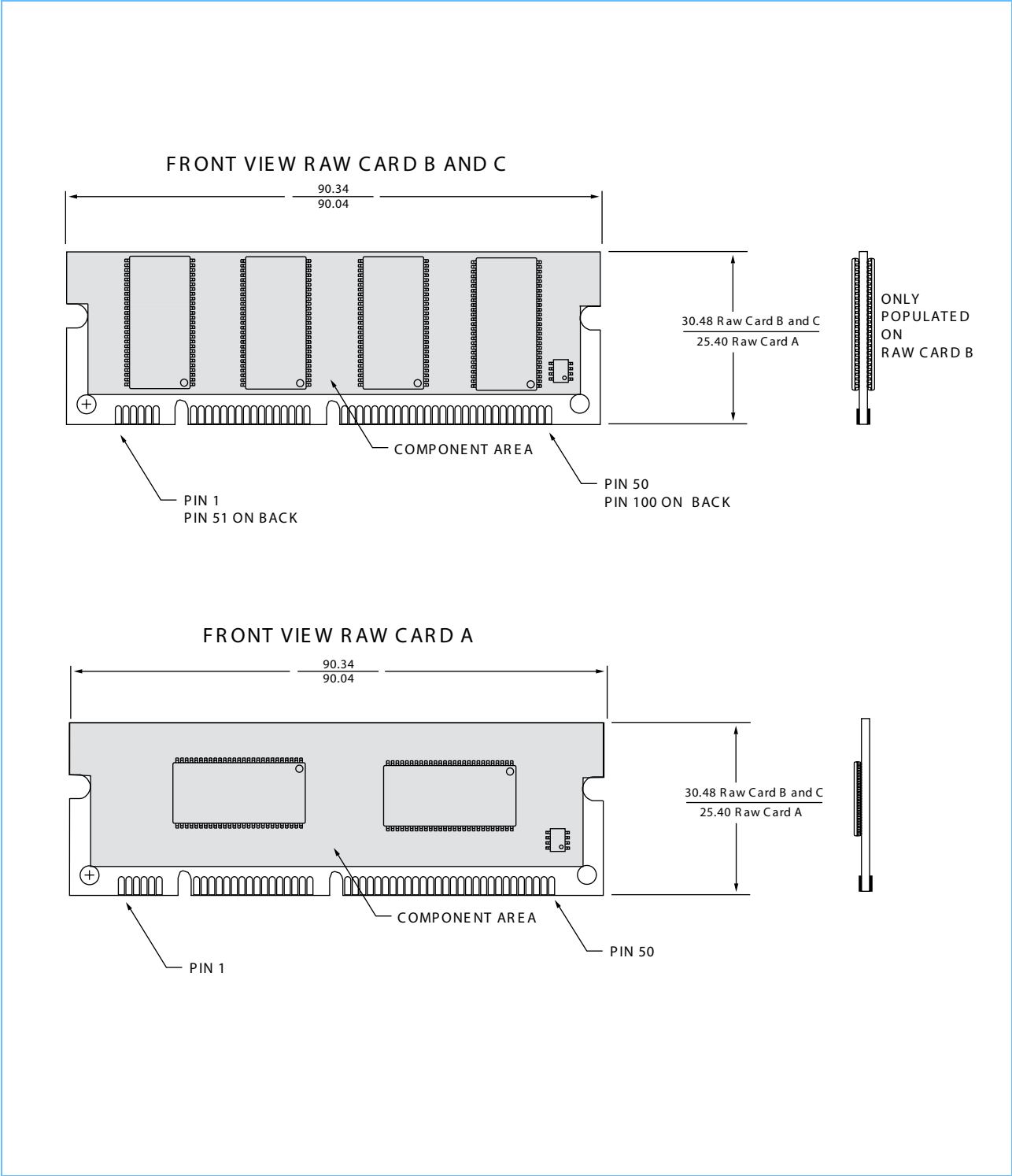
## Gerber File Releases

Reference design file updates will be released as needed. This specification will reflect the most recent design files, but may be updated to reflect clarifications to the specification only; in these cases, the design files will not be updated. The following table outlines the most recent design file releases:

Raw Card	Specification Revision	Applicable Gerber File	Notes
A	0.5	A1	
B	0.5	B1	
C	0.5	C1	
D	1.0	D1	
E	1.0	E1	

### Example Raw Card Component Placement

The component layout for Raw Cards B, C and E are similar. Raw cards A and D are a lower profile variation. This example is for reference only; please refer to JEDEC standard MO-161 variation DA and GA for details.



## 6. 32b-DIMM Wiring Details

### Signal Groups

This reference specification categorizes DDR SDRAM timing-critical signals into seven groups whose members have identical loadings and routings. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Page
Clocks for Unbuffered 32b-DIMM	CK [1:0], $\overline{CK}$ [1:0]	21
Data, Data Mask, Data Strobe	DQ [31:0], DM[3:0], DQS[3:0]	22
Select	$\overline{S}$ [1:0]	23
Clock Enable	CKE [1:0]	24
Address/Control	Ax, BAx, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	25

### General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing recommendations are as follows. Other stackups and layouts are possible that meet the electrical characteristics.

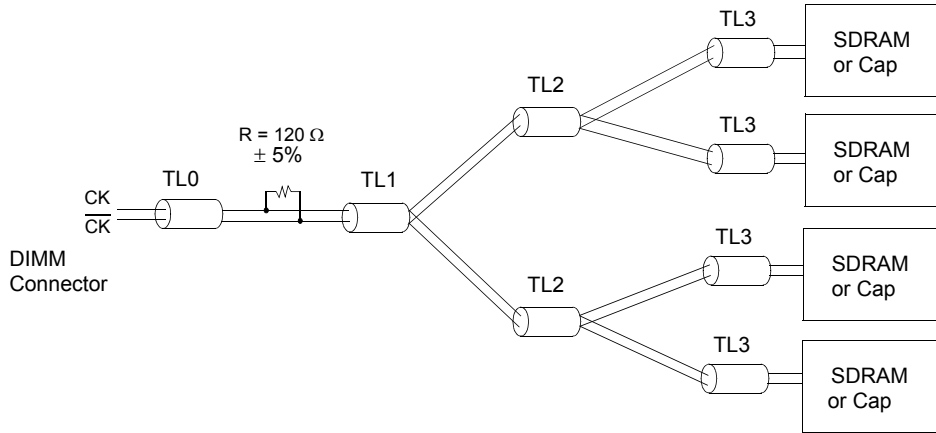
- Route all signal traces except clocks using 0.10 mm rules, 0.15 mm minimum spacing between adjacent traces.
- Route clocks as much as possible using the inner layers in the 6 layer stack-up.
- Internal signal layers and the power plane should have a ground ring around the perimeter of the board, stitched to ground at 12.7 mm intervals. The ground ring should be at least 0.5 mm wide where layout permits, but can be reduced to 0.25 mm when necessary.
- No test points are required.

### Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for unbuffered 32b-DIMM designs. The diagrams should be used to determine individual signal wiring on a 32b-DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify 32b-DIMM functionality, a full simulation of all signal integrity and timing is required. The given net structures and trace lengths are not inclusive for all solutions.

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one DDR SDRAM input. The net structure routing data in this document accurately represent reference Raw Card versions A, B, C, D and E.

## Clock Net Wiring



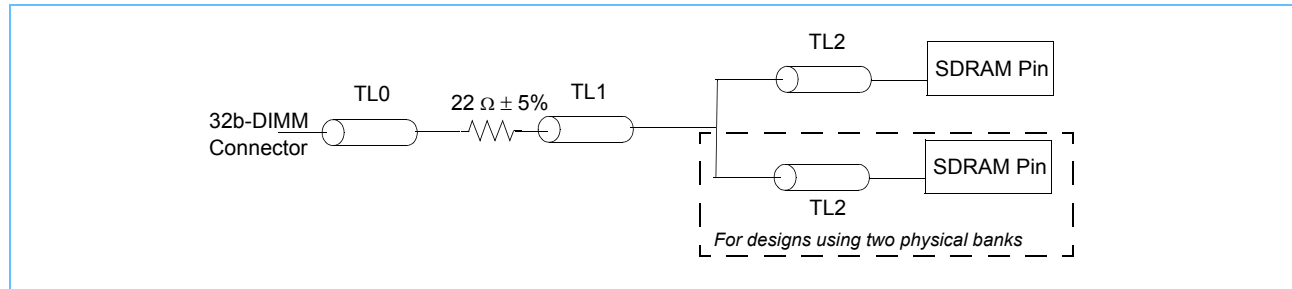
### Clock Routing Trace Lengths

Raw card	TL0		TL1		TL2		TL3	
	Min	Max	Min	Max	Min	Max	Min	Max
A	22.00	22.02	1.47	1.49	20.07	20.45	8.18	8.31
B	41.05	41.07	0.00	0.02	8.64	8.66	7.92	7.94
C	17.65	17.67	0.00	0.02	24.54	24.56	17.07	17.09
D	17.31	17.32	0.92	0.94	22.25	24.51	9.35	9.37
E	17.66	17.67	1.15	1.15	25.91	25.92	14.36	16.91

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

## Data Net Structures DQ[31:0], DM[3:0], DQS[3:0]

### Net Structure Routing for Data, Data Mask, Data Strobe



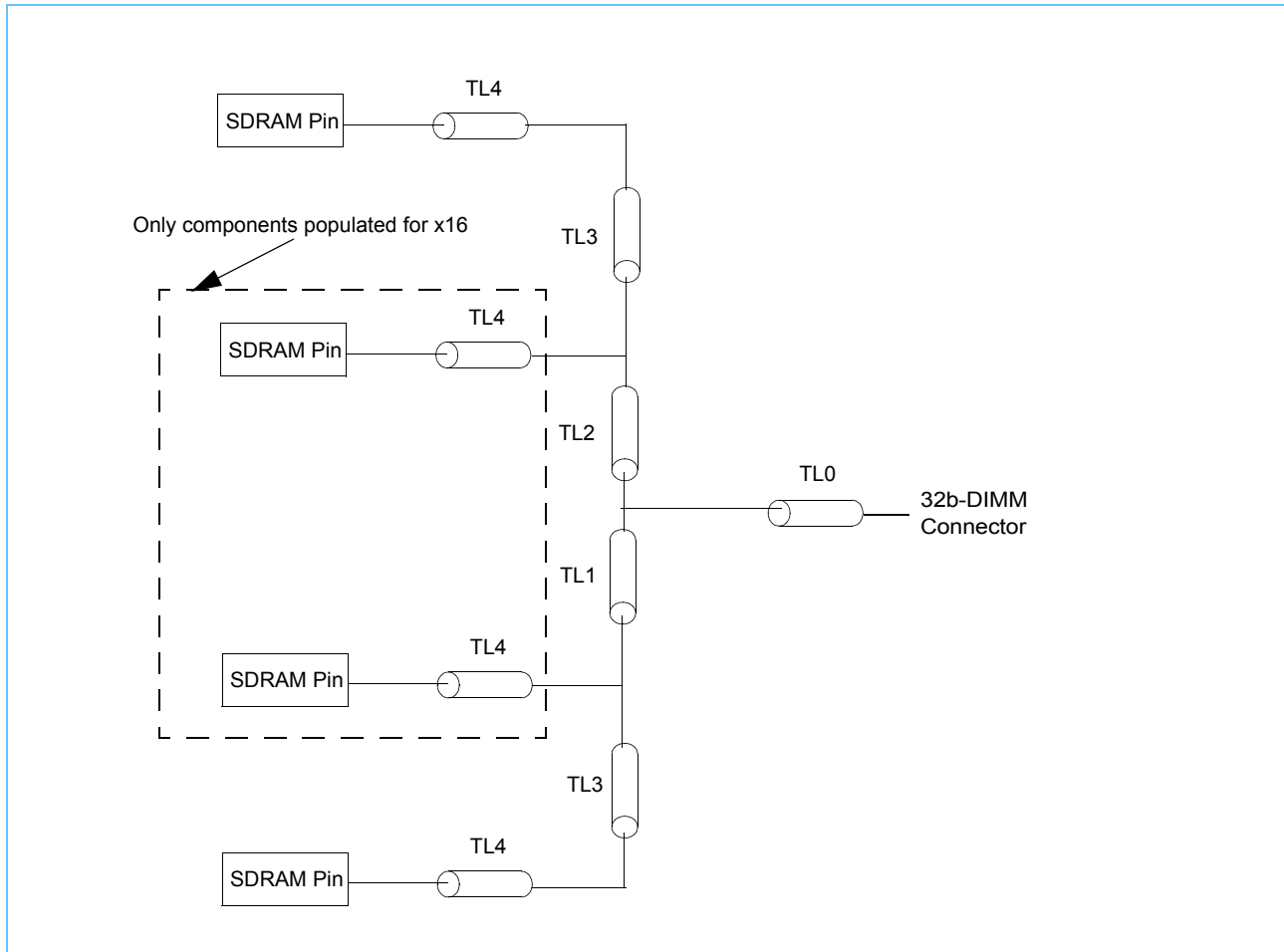
### Trace Lengths for Data Net Structure

Raw card	TL0		TL1		TL2		Total	
	Min	Max	Min	Max	Min	Max	Min	Max
A	3.55	3.57	20.88	32.05	N/A	N/A	24.43	35.62
B	3.66	8.18	10.01	18.34	1.17	7.75	$20.83^2$	$23.88^2$
C	3.66	6.02	19.10	23.52	N/A	N/A	$24.13^2$	$27.18^2$
D	3.01	5.26	29.79	41.41	N/A	N/A	$32.80^3$	$46.67^3$
E	3.71	5.46	17.79	22.12	N/A	N/A	$21.50^3$	$27.58^3$

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.
2. Raw Cards B and C total length minimum is for traces with a via and maximum is for traces with no via.
3. Raw Cards D and E total length minimum is for traces with a maximum via count and maximum is for traces with no via.

## Select Net Structures $\bar{S}[1:0]$

### Net Structure Routing for Select



### Trace Lengths for Select Net Structures

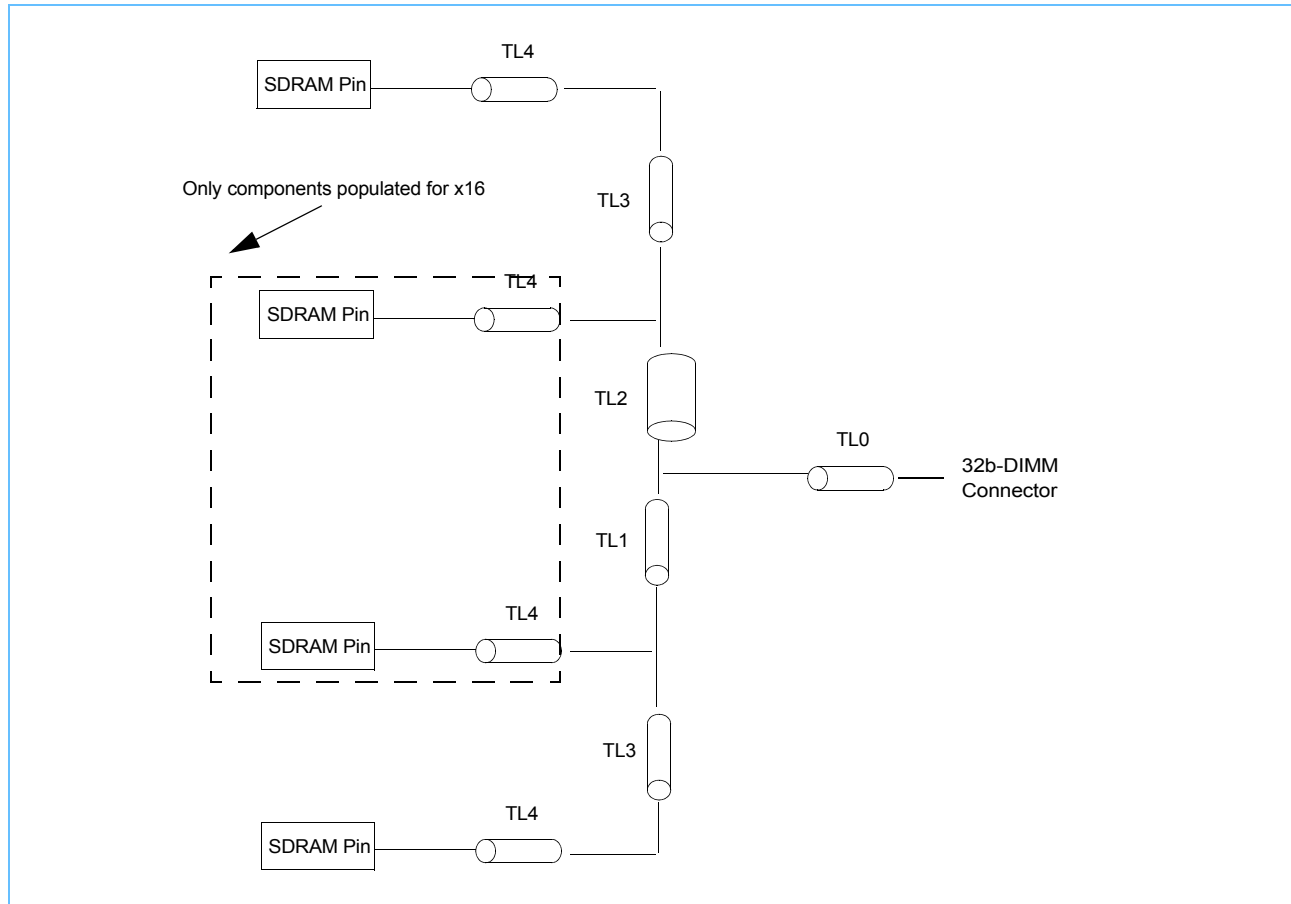
Raw Card	TL0		TL1 + TL4		TL2 + TL4	
	Min	Max	Min	Max	Min	Max
A	125.14	125.16	22.29	22.31	22.29	22.31
D	111.35	111.35	28.03	28.08	28.03	28.08

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

Raw Card	TL0		TL1		TL2		TL3		TL4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
B	86.87	86.89	17.78	17.80	17.78	17.80	16.69	16.71	7.75	7.77
C	76.20	76.22	17.93	17.95	17.93	17.95	16.64	16.66	6.53	6.55
E	80.02	80.02	17.93	17.93	17.93	17.93	16.62	16.66	6.51	6.75

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

## Clock Enable Net Structures, CKE [1:0] Net Structure Routing for Clock Enable



### Trace Lengths for Clock Enable Net Structure

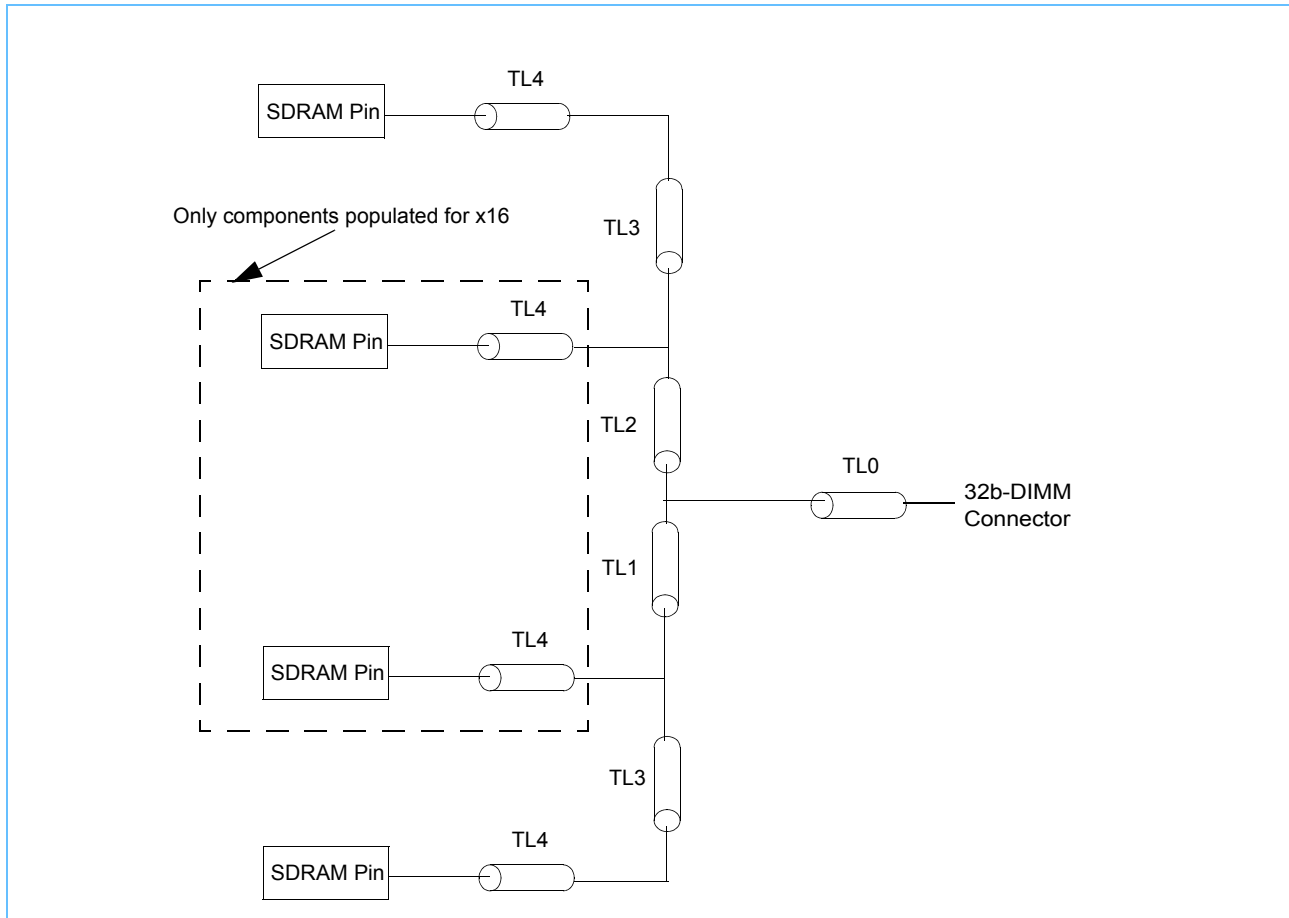
Raw Card	TL0		TL1 + TL4		TL2 + TL4	
	Min	Max	Min	Max	Min	Max
A	125.69	125.71	21.61	21.63	22.82	22.84
D	112.37	112.37	28.07	28.07	28.07	28.07

- All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

Raw Card	TL0		TL1		TL2		TL3		TL4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
B	86.87	86.89	17.78	17.80	17.78	17.80	16.69	16.71	7.75	7.77
C	76.20	76.22	17.93	17.95	17.93	17.95	16.64	16.66	6.53	6.55
E	76.25	76.25	17.93	17.93	17.93	17.93	16.59	16.62	6.52	6.53

- All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

## Address/Control Net Structures Ax, BAx, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ Net Structure Routing for Address and Control



### Trace Lengths for Address and Control Net Structures

Raw Card	TL0		TL1 + TL4		TL2 + TL4	
	Min	Max	Min	Max	Min	Max
A	125.17	126.18	22.17	22.32	21.97	22.38
D	107.29	114.96	27.55	30.61	27.55	30.61

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

Raw Card	TL0		TL1		TL2		TL3		TL4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
B	32.00	32.02	17.78	17.80	17.78	17.80	16.69	16.71	7.75	7.77
C	76.20	76.22	17.93	17.95	17.93	17.95	16.64	16.66	6.53	6.55
E	71.14	76.25	17.92	17.95	17.92	17.95	6.52	15.26	23.12	23.14

1. All distances are given in mm and should be kept within a tolerance of  $\pm 0.03$  mm.

## Cross Section Recommendations

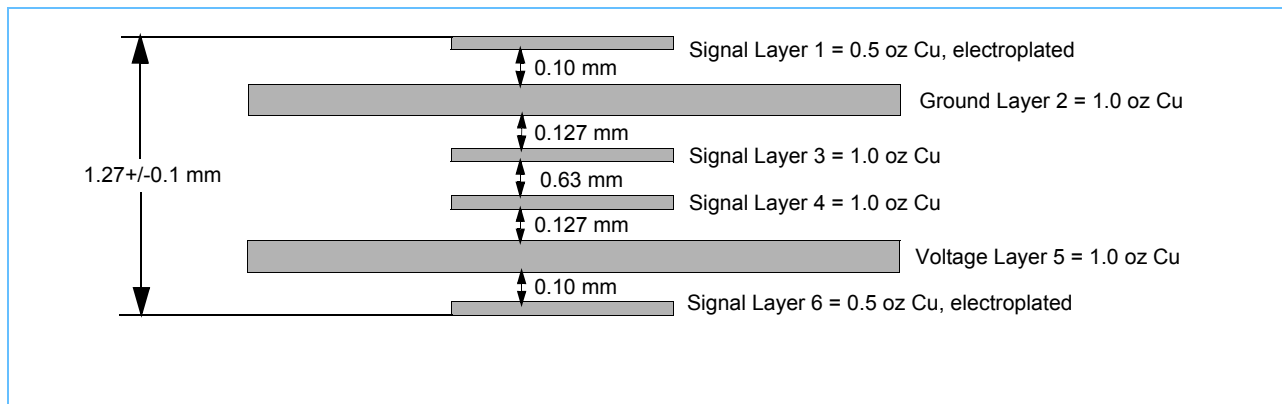
The DDR 32b-DIMM printed circuit board design uses six-layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 0.1 mm wide traces with 0.15 mm spacing. The required board impedance is  $60 \Omega \pm 10\%$ .

**Note:** The PCB edge connector contacts shall be gold-plated; chamfered edges are optional.

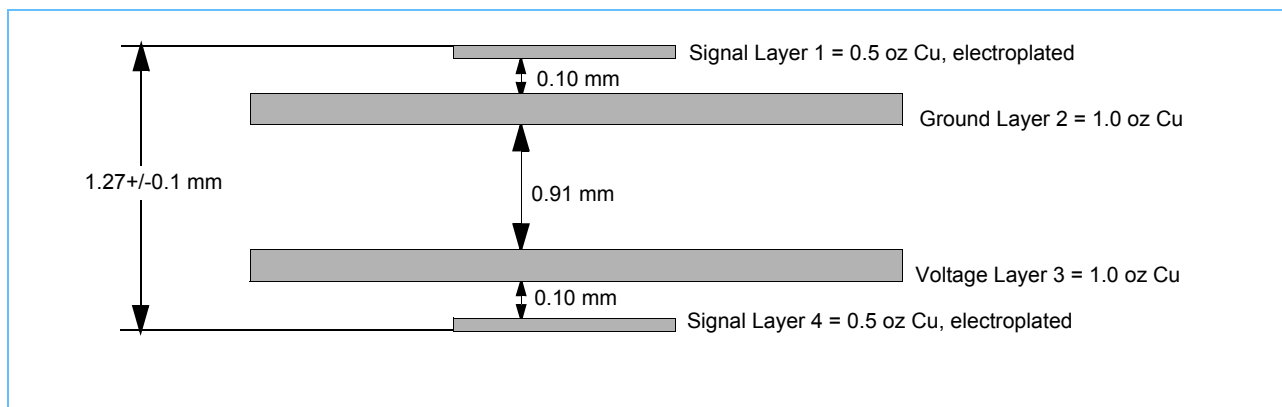
## PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.0	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z0 (all layers)	54	66	Ohms

### Example 6 Layer Stackup



### Example 4 Layer Stackup



## Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors, for DDR SDRAM devices, must be practically located near the device power pins.

## Reference Voltage Vias

A minimum of two vias located near the connector pins should be used to connect  $V_{REF}$  to its inner routing layer.

## 7. Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the DDR SDRAM 32b-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of a typical 32b-DIMM. SPD values indicating different 32b-DIMM performance characteristics will be utilized based on specific characteristics of the SDRAMs or 32b-DIMMs. This example assumes:

- Module Organization: 32 M x 32 (128 Mbyte)
- Device Composition: 4 M x 8 bits x 4 banks (128 Mb)
- Device Package: 66 pin TSOP-II
- Module Physical Banks: 2
- Refresh: 4 K in 64 ms

### Serial Presence Detect Data Example (Part 1 of 3)

Byte #	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Notes
		DDR 333	DDR 266A	DDR 266B	DDR 333	DDR 266A	DDR 266B	
0	Number of Serial PD Bytes Written during Production	128 bytes			80			
1	Total Number of Bytes in Serial PD device	256 bytes			08			
2	Fundamental Memory Type	DDR SDRAM			07			
3	Number of Row Addresses on Assembly	12			0C			
4	Number of Column Addresses on Assembly	10			0A			
5	Number of 32b-DIMM Banks	2			02			
6	Data Width of Assembly	32bits			20			
7	Data Width of Assembly (continued)	32 bits			00			
8	Assembly Voltage Interface Levels ( $V_{DDQ}$ )	SSTL_2			04			
9	SDRAM Device Cycle Time at CL = 2.5 ( $t_{CK}$ )	6.0 ns	7.5 ns	7.5 ns	60	75	75	1
10	SDRAM Device Access Time from Clock ( $t_{AC}$ )	0.70 ns	0.75 ns	0.75 ns	70	75	75	1
11	Assembly Error Detection/Correction Scheme	Non-parity, non-ECC			00			
12	Assembly Refresh Rate/Type	15.6 $\mu$ s Self Refresh			80			
13	SDRAM Device Width	x8			08			
14	Error Checking SDRAM Device Width	Not used			00			
15	Minimum CK Delay, Random Col Access ( $t_{CCD}$ )	1 clock			01			
16	Burst Lengths Supported	2, 4, 8			0E			
17	Number of Device Banks	4			04			

1. Minimum application clock cycle time is 7.5 ns (133 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)

**Serial Presence Detect Data Example** (Part 2 of 3)

Byte #	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Notes
		DDR 333	DDR 266A	DDR 266B	DDR 333	DDR 266A	DDR 266B	
18	CAS Latency	2.5 and 2.0			0C			
19	$\overline{\text{CS}}$ Latency	0 clocks			01			
20	$\overline{\text{WE}}$ Latency	1 clock			02			
21	SDRAM Module Attributes	Differential clocks			20			7
22	General SDRAM Device Attributes	Concurrent fast auto pre-charge			C0			7
23	Minimum Clock Cycle at CL = 2.0 ( $t_{\text{CK}}$ )	7.5 ns	7.5 ns	10 ns	75	75	A0	1
24	Maximum Data Access Time ( $t_{\text{AC}}$ ) from Clock at CL = 2.0	0.70 ns	0.75 ns	0.75 ns	70	75	75	1
25	Minimum Clock Cycle Time at CL = 1.5 ( $t_{\text{CK}}$ )	N/A			00			6
26	Maximum Data Access Time ( $t_{\text{AC}}$ ) from Clock at CL = 1.5	N/A			00			6
27	Minimum Row Precharge Time ( $t_{\text{RP}}$ )	20 ns			50			
28	Minimum Row Active to Row Active delay ( $t_{\text{RRD}}$ )	15 ns			3C			
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay ( $t_{\text{RCD}}$ )	20 ns			50			
30	Minimum Active to Precharge Time ( $t_{\text{RAS}}$ )	42 ns	45 ns	45 ns	2A	2D	2D	
31	Module Physical Bank Density	64 MB			10			
32	Address and Command Setup Time Before Clock ( $t_{\text{IS}}$ )	0.75 ns	0.9 ns	0.9 ns	75	90	90	
33	Address and Command Hold Time After Clock ( $t_{\text{IH}}$ )	0.75 ns	0.9 ns	0.9 ns	75	90	90	
34	Data Input and Mask Setup Time Before Clock ( $t_{\text{DS}}$ )	0.45 ns	0.5 ns	0.5 ns	45	50	50	
35	Data Input and Mask Hold Time After Clock ( $t_{\text{DH}}$ )	0.45 ns	0.5 ns	0.5 ns	45	50	50	
36 - 40	Superset information	No superset			00			6
41	Row cycle time ( $t_{\text{RC}}$ )	60 ns	65 ns	70 ns	3C	41	46	
42	Auto Refresh cycle time ( $t_{\text{RFC}}$ )	72 ns	75 ns	80 ns	48	4B	50	
43	Maximum SDRAM device cycle time ( $t_{\text{CKmax}}$ )	12 ns	12 ns	12 ns	30	30	30	
44	DQS-DQ Skew ( $t_{\text{DQSQ}}$ )	0.45 ns	0.50 ns	0.60 ns	2D	32	3C	8
45	SDRAM Device Data Hold Skew Factor ( $t_{\text{QHS}}$ )	0.55 ns	0.75 ns	1.0 ns	55	75	A0	8
46-61	Reserved	0	0	0	00	00	00	
62	SPD Revision	JEDEC 0			00			
63	Checksum for bytes 0 - 62	Calculated value			cc	cc	cc	2
64 - 71	Manufacturers' JEDEC ID Code							6

1. Minimum application clock cycle time is 7.5 ns (133 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)

**Serial Presence Detect Data Example** (Part 3 of 3)

Byte #	Description	SPD Entry Value			Serial PD Data Entry (Hexadecimal)			Notes
		DDR 333	DDR 266A	DDR 266B	DDR 333	DDR 266A	DDR 266B	
72	Assembly Manufacturing Location							6
73 - 90	Module Part Number							6
91 - 92	Module Revision Code							6
93 - 94	Module Manufacturing Date							3, 4
95 - 98	Module Serial Number							5
99 - 127	Manufacturer's Specific Data							6
128 - 255	Open for Customer Use	Undefined			00			

1. Minimum application clock cycle time is 7.5 ns (133 MHz).
2. cc = Checksum Data byte, 00-FF (Hex).
3. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
4. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
5. ss = Serial number data byte, 00-FF (Hex).
6. Unused bytes are set to the value "00".
7. Unused bits in attribute bytes are set to "0".
8. Values dependent on package type (TSOP-II or FBGA)



## 9. Product Label

The following label should be applied to all DDR 32b-DIMMs, to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label.

### Format:

EPwwwm-aabc-d-ef

### Where:

www: Module Bandwidth

1350 = 1.35 GB/sec

1050 = 1.05 GB/sec

0800 = 0.8 GB/sec

m: Module Type

H = Unbuffered DDR 32b-DIMM (no registers or PLLs on module)

aa: DDR SDRAM CAS Latency

20 = CAS Latency 2.0

25 = CAS Latency 2.5

b: DDR SDRAM minimum  $t_{RCD}$  specification (in clocks)

c: DDR SDRAM minimum  $t_{RP}$  specification (in clocks)

d: JEDEC SPD Revision used on this DDR 32b-DIMM

0 = JEDEC SPD revision 0

e: Gerber file used for this design (if applicable)

A = Reference design for raw card 'A' is used for this assembly

B = Reference design for raw card 'B' is used for this assembly

C = Reference design for raw card 'C' is used for this assembly

D = Reference design for raw card 'D' is used for this assembly

E = Reference design for raw card 'E' is used for this assembly

Z = None of the 'Reference' designs were used for this assembly

f: Revision number of the reference design used

1 = 1st revision

2 = 2nd revision

Blank = Not applicable (used with 'Z' above)

### Example:

EP1350H-2533-2-B1 is a EP1350 Unbuffered DDR 32b-DIMM

with CAS Latency = 2.5,  $t_{RCD} = 3$ ,  $t_{RP} = 3$ ,

using JEDEC SPD revision 2

and produced based on the raw card 'B' Gerber, 1st release

## Revision History:

Date	Rev.	Page	Changes
5/28	0.1		Initial Release
7/24	0.2	18-22	Filled in the trace length tables for Raw cards B and C.
7/24	0.2	All	Updated all units of measure from inches to mm.
7/24	0.2	23	Corrected dimensions on the example stackup.
7/24	0.2	15	Updated the gerber file table.
10/22	0.5	15	Added Raw card A to gerber table.
10/22	0.5	18-22	Filled in the trace length for raw card A and updated the lengths for raw cards B and C.
1/8/03	1.0	8-10	Connected unused upper address bits of SPD to Vss.
2/24/04	1.1	All	Added Raw Cards D and E.