

Appendix X: Serial Presence Detect (SPD) for Fully Buffered DIMM (Revision 1.1)

1.0 Introduction

This appendix describes the serial presence detect (SPD) values for Fully Buffered DIMMs. These presence detects are those referenced in the SPD standard document for ‘Specific Features’. The following SPD fields will occur in the order presented in section 1.1. *Note that the descriptions of Bytes 0 and 1 are different from those found in previous SPD standards.* Further description of Byte 2 is found in Appendix A of the SPD standard. All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

1.1 Address map

The following is the SPD address map for FB-DIMM, i.e., when the value in Key Byte 2 is 0x09. It describes where the individual look-up table entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	1,2
1	SPD Revision	
2	Key Byte / DRAM Device Type	
3	Voltage Levels of this Assembly	
4	SDRAM Addressing	
5	Module Physical Attributes	
6	Module Type / Thickness	
7	Module Organization	
8	Fine Timebase Dividend and Divisor	
9	Medium Timebase Dividend	
10	Medium Timebase Divisor	
11	SDRAM Minimum Cycle Time (tCKmin)	3
12	SDRAM Maximum Cycle Time (tCKmax)	3
13	SDRAM CAS Latencies Supported	
14	SDRAM Minimum CAS Latency Time (tCAS)	
15	SDRAM Write Recovery Times Supported	
16	SDRAM Write Recovery Time (tWR)	3
17	SDRAM Write Latencies Supported	
18	SDRAM Additive Latencies Supported	
19	SDRAM Minimum RAS to CAS Delay (tRCD)	3
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	3
21	SDRAM Minimum Row Precharge Time (tRP)	3
22	SDRAM Upper Nibbles for tRAS and tRC	3
23	SDRAM Minimum Active to Precharge Time (tRAS)	3
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	3
25-26	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	3
27	SDRAM Internal Write to Read Command Delay (tWTR)	3
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	3
29	SDRAM Burst Lengths Supported	
30	SDRAM Terminations Supported	

Byte Number	Function Described	Notes
31	SDRAM Drivers Supported	
32	SDRAM Average Refresh Interval (tREFI) / Double Refresh mode bit / High Temperature self-refresh rate support indication	3
33	Bits 7:4: Tcasemax Delta (SDRAM case temperature difference between maximum case temperature and baseline maximum case temperature), the baseline maximum case temperature is 85 °C. Bits 3:0: DT4R4W Delta (Case temperature rise difference between IDD4R/page open burst read and IDD4W/page open burst write operations).	6, 7, 10, 11
34	Thermal resistance of SDRAM device package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	5, 9, 11
35	DT0: Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 °C offset temperature.	6, 7, 10, 11
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/precharge standby operation for UDIMM and due to IDD2Q/precharge quiet standby operation for RDIMM.	6, 7, 10, 11
37	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation.	6, 7, 10, 11
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	6, 7, 10, 11
39	DT4R/Mode Bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	6, 7, 10, 11
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	6, 7, 10, 11
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	6, 7, 10, 11
42-59	Reserved	
60-78	Reserved	
79	FB-DIMM ODT Values	
80	Reserved	
81-82	FB-DIMM Channel Protocols Supported	
83	Back-to-Back Access Turnaround Time	
84	AMB Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)	
85	AMB Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)	
86	AMB Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)	
87	Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A AMB)	
88	AMB DT Idle_0	8, 10, 11
89	AMB DT Idle_1	8, 10, 11
90	AMB DT Idle_2	8, 10, 11
91	AMB DT Active_1	8, 10, 11
92	AMB DT Active_2	8, 10, 11
93	AMB DT L0s	8, 10, 11
94-97	Reserved	
98	AMB Case Temperature Maximum (Tcase_max)	
99-100	Reserved	
101-106	AMB Personality Bytes: Pre-initialization	
107-114	AMB Personality Bytes: Post-initialization	
115-116	AMB Manufacturer's JEDEC ID Code	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	

Byte Number	Function Described	Notes
119	Module ID: Module Manufacturing Location	
120-121	Module ID: Module Manufacturing Date	
122-125	Module ID: Module Serial Number	
126-127	Cyclical Redundancy Code	
128-145	Module Part Number	4
146-147	Module Revision Code	4
148-149	SDRAM Manufacturer's JEDEC ID Code	4
150-175	Manufacturer's Specific Data	4
176-255	Open for customer use	

1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes.
2. Size of SPD device will typically be programmed as 256 bytes.
3. From SDRAM datasheet.
4. These are optional, in accordance with the JEDEC spec.
5. Refer to JESD51-3 "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages" under JESD51-2 standard.
6. DT parameter is derived as following: $DTx = IDDx * VDD * \Psi T-A$, where $IDDx$ definition is based on JEDEC DDR2 Component Specification and at $VDD = 1.9\text{ V}$, it is the datasheet (worst case) value, and $\Psi T-A$ is the programmed value of $\Psi T-A$ (value in SPD Byte 33). Programmed temperature rise data (DTx) is based on the programmed value of $\Psi T-A$ (value in SPD byte 33).
7. All DT parameters are defined for DDR2 SDRAM densities up to 2 Gbit. 4 Gbit parameters will be defined later.
8. DT parameters for the AMB are derived as following: $DTx = (IDDx * VDD * \Psi T-A) + (ICCx * VCC * \Psi T-A) + (IDDSPDx * VDDSPD * \Psi X T-A)$ where $IDDx$ is at $VDD = 1.9\text{ V}$, $ICCx$ is at $VCC = 1.535\text{ V}$, and $IDDSPDx$ is at $VDDSPD = 3.6\text{ V}$; these are the active AMB powers corresponding to the AMB's respective DIMM configuration loading. The $IDDx$, $ICCx$, and $ISPDx$ are worst case values. $\Psi T-A$ used to program DTx is the programmed value of AMB $\Psi T-A$ (value in SPD byte 87).
9. Rule for rounding off thermal resistance values: $\Psi X X-X$ shall be rounded such that it is nearest/closest to the true value of $\Psi X X-X$.
10. Rule for rounding off DTx : DTx shall be rounded such that it is nearest/closest to the calculated value of DTx .
11. Thermal bytes are for the DIMM as shipped, with any associated heat spreader, heat sink, mechanical clips, and label.

2.0 Details of each byte

2.1 General Section: Bytes 0 to 59

This section contains fields which with little modification can be used for SPD definitions for non-FB-DIMM modules.

Byte 0: Number of Bytes Utilized / Number of Bytes in SPD Device / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6-4 describe the total size of the serial memory used to hold the Serial Presence Detect data. Bit 7 indicates whether the unique module identifier (found in bytes 117 to 125) is covered by the CRC encoded on bytes 126 and 127.

Bit 7	Bit 6 ~ 4	Bit 3 ~ Bit 0
CRC Coverage	SPD Bytes Total	SPD Bytes Used
0 = CRC covers bytes 0 ~ 125 1 = CRC covers bytes 0 ~ 116	Bit [6, 5, 4] : 000 = Undefined 001 = 256 All Others TBD	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 176 0011 = 256 All Others TBD

Byte 1: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte must be coded as 0x11 for SPDs with revision level 1.1. Software should examine the upper nibble(Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

SPD Revision	Encoding Level				Additions Level				Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Revision 0.0	0	0	0	0	0	0	0	0	00
Undefined	0	0	0	0	0	0	0	1	01
...
Revision 1.0	0	0	0	1	0	0	0	0	10
Revision 1.1	0	0	0	1	0	0	0	1	11
...
Undefined	1	1	1	1	1	1	1	1	FF

Byte 2: Key Byte

This byte is the key byte used by BIOS to determine how to interpret all other bytes in the SPD EEPROM. BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any SDRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

Line #	SDRAM / Module Type Corresponding to Key Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	DDR1 SGRAM	0	0	0	0	0	1	1	0	06
7	DDR1 SDRAM	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
9	DDR2 SDRAM FB-DIMM	0	0	0	0	1	0	0	1	09
10	DDR2 SDRAM FB-DIMM PROBE	0	0	0	0	1	0	1	0	0A
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Voltage Levels of this Assembly

This byte describes the expected voltage level for two power supplies that are connected to the module. For example, Fully Buffered DIMM Power Supply 1 is defined as the supply for the channel interface, and Power Supply 2 is defined as the supply for the DRAM interface.

Bit 7 ~ 4	Bit 3 ~ Bit 0
Power Supply 2	Power Supply 1
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1.8 V 0010 = 1.5 V 0011 = 1.2 V All Others TBD	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 1.8 V 0010 = 1.5 V 0011 = 1.2 V All Others TBD

Byte 4: SDRAM Addressing

This byte describes the row addressing, the column addressing, and the number of banks in the SDRAM device. Bits 1-0 encode the number of banks, bits 4-2 encode the number of column address bits, and bits 7-5 encode the number of row address bits.

Bit 7 ~ 5	Bit 4 ~ 2	Bit 1 ~ Bit 0
Row Address Bits	Column Address Bits	Number of Banks
Bit [7, 6, 5] : 000 = 12 001 = 13 010 = 14 011 = 15 All Others TBD	Bit [4, 3, 2] : 0000 = 9 0001 = 10 0010 = 11 All Others TBD	Bit [1, 0] : 00 = 4 01 = 8 10 = 16 11 = 32

Byte 5: Module Physical Attributes

This byte describes the height and thickness of the SDRAM module. Bits 2-0 encode the module thickness, which is defined as the maximum value including all finished assembly parts: devices, heat spreaders, or other mechanical components. Encodings for bits 2-0 will depend on the value of Byte 6, the Module Type.

Bit 7 ~ Bit 6	Bit 5 ~ Bit 3	Bit 2 ~ Bit 0
Reserved	Module Height (mm)	Module Thickness (mm)
	Bit [5, 4, 3] : 000 = Undefined 001 = 15 < x ≤ 20 010 = 20 < x ≤ 25 011 = 25 < x ≤ 30 100 = 30 < x ≤ 35 101 = 35 < x ≤ 40 110 = 40 < x ≤ 50 All others undefined	Bit [2, 1, 0] : See indexed tables below
Note: Refer to JEDEC standard MO-256 for standard module outline characteristics including height and thickness.		

Decoding of the Module Thickness field, based on Module Type (units in mm) is shown below. Table entries other than FB-DIMM are shown for reference only.

Module Thickness			FB-DIMM
Bit 2	Bit 1	Bit 0	Byte 6 [3:0] = 0111
0	0	0	Undefined / Not specified
0	0	1	x ≤ 6.0
0	1	0	6.0 < x ≤ 7.0
0	1	1	7.0 < x ≤ 8.0
1	0	0	8.0 < x ≤ 9.0
1	0	1	9.0 < x
1	1	0	Reserved
1	1	1	Reserved

Byte 6: Module Type

This byte identifies the SDRAM memory module type and also indicates the width of the module. BIOS uses the module type information in this byte to determine the encoding of the module thickness field in byte 5.

Table entries other than FB-DIMM are shown for reference only.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Module Type
	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = RDIMM (width = 133.35 mm nom) 0010 = UDIMM (width = 133.35 mm nom) 0011 = SO-DIMM (width = 67.6 mm nom) 0100 = Micro-DIMM (width = 54.0 mm nom) 0101 = Mini-RDIMM (width = 82.0 mm nom) 0110 = Mini-UDIMM (width = 82.0 mm nom) 0111 = FB-DIMM (width = 133.35 mm nom) All others TBD
Definitions: RDIMM: Registered Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SO-DIMM: Small Outline Dual In-Line Memory Module Micro-DIMM: Micro Dual In-Line Memory Module Mini-RDIMM: Mini Registered Dual In-Line Memory Module Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module FB-DIMM: Fully Buffered Dual In-Line Memory Module	

Byte 7: Module Organization

This byte describes the organization of the SDRAM module. Bits 2-0 encode the device width of the SDRAM devices. Bits 5-3 encode the number of physical ranks on the SDRAM. For example, for a single-rank module with x8 SDRAMs, this byte is encoded 00 001 001, or 0x09.

Bit 7 ~ Bit 6	Bit 5 ~ Bit 3	Bit 2 ~ Bit 0
Reserved	Number of Ranks	SDRAM Device Width
	Bit [5, 4, 3] : 000 = Undefined 001 = 1 Rank 010 = 2 Ranks All others undefined	Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others undefined

Byte 8: Fine Timebase (FTB) Dividend / Divisor

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain timing calculations. This value is used as a multiplier for formulating subsequent timing parameters. The fine timebase (FTB) is defined as the fine timebase dividend, bits 7~4, divided by the fine timebase divisor, bits 3~0. A value of 0x00 should only be programmed if the FTB is not utilized by any SPD fields.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Fine Timebase (FTB) Dividend	Fine Timebase (FTB) Divisor
Values defined from 0 to 15	Values defined from 0 to 15

Examples:

Dividend	Divisor	Timebase (ps)	Use
5	1	5	When time granularity of 5 ps is required
5	2	2.5	When time granularity of 2.5 ps is required

Byte 9: Medium Timebase (MTB) Dividend

Byte 10: Medium Timebase (MTB) Divisor

These bytes define a value in nanoseconds that represents the fundamental timebase for medium grain timing calculations. This value is typically the greatest common divisor for the range of clock frequencies (clock periods) supported by a particular SDRAM. This value is used as a multiplier for formulating subsequent timing parameters. The medium timebase (MTB) is defined as the medium timebase dividend (byte 9) divided by the medium timebase divisor (byte 10).

Byte 9 Bit 7 ~ Bit 0	Byte 10 Bit 7 ~ Bit 0
Medium Timebase (MTB) Dividend	Medium Timebase (MTB) Divisor
Values defined from 1 to 255	Values defined from 1 to 255

Examples:

Dividend	Divisor	Timebase (ns)	Use
1	4	0.25	For clock frequencies of 200, 267, 333, and 400 MHz
1	8	0.125	For clock frequencies of 400, 533, 667, and 800 MHz

To simplify BIOS implementation, DIMMs associated with a given key byte value may differ in MTB value only by a factor of two. For DDR2 FB-DIMM (key byte values 0x09 and 0x10), the defined MTB values are:

Dividend	Divisor	Timebase (ns)	Use
1	4	0.25	FB-DIMM MTB Value
1	8	0.125	FB-DIMM MTB Value

Byte 11: Minimum SDRAM Cycle Time (t_{CKmin})

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM.

Bit 7 ~ Bit 0
Minimum SDRAM Cycle Time (t_{CKmin}) MTB Units
Values defined from 1 to 255

Examples:

tCKmin (MTB units)	Timebase (ns)	tCKmin Result (ns)	Use
20	0.25	5	DDR2 with 200 MHz clock
15	0.25	3.75	DDR2 with 266 MHz clock
12	0.25	3	DDR2 with 333 MHz clock
10	0.25	2.5	DDR2 with 400 MHz clock
20	0.125	2.5	DDR3 with 400 MHz clock
15	0.125	1.875	DDR3 with 533 MHz clock
12	0.125	1.5	DDR3 with 667 MHz clock
10	0.125	1.25	DDR3 with 800 MHz clock

Byte 12: Maximum SDRAM Cycle Time (t_{CKmax})

This byte defines the maximum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM.

Bit 7 ~ Bit 0
Maximum SDRAM Cycle Time (t_{CKmax}) MTB Units
Values defined from 1 to 255

Examples:

tCKmax (MTB units)	Timebase (ns)	tCKmax Result (ns)	Use
32	0.25	8	DDR2, 125 MHz maximum clock period
64	0.125	8	DDR3, 125 MHz maximum clock period

Byte 13: CAS Latencies Supported

This field describes the CAS Latency (CL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of CL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support CAS latencies 3, 4, and 5 would program a CL Range of 3 and a minimum CL of 3: 0011 0011 = 0x33.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
CL Range (clocks)	Minimum CL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 All other values TBD	Bit [3, 2, 1, 0] : 0011 = 3 0100 = 4 0101 = 5 0110 = 6 All other values TBD

Byte 14: Minimum CAS Latency Time (t_{AAmin})

This byte defines the minimum CAS Latency in medium timebase (MTB) units. Software can use this information, along with range of CAS Latencies supported (found in byte 13) to determine the optimal cycle time for a particular module. Parameter t_{AAmin} for a specific DDR2 SDRAM is the smallest number resulting from the multiplication of t_{CKmin} @ CL=n times the CAS latency n for each supported CAS latency for that SDRAM speed bin.

Bit 7 ~ Bit 0
Minimum SDRAM CAS Latency Time (t_{AAmin}) MTB Units
Values defined from 1 to 255

Examples:

t_{AAmin} (MTB units)	Timebase (ns)	t_{AAmin} Result (ns)	Use
60	0.25	15	DDR2-400B
80	0.25	20	DDR2-400C
45	0.25	11.25	DDR2-533B
60	0.25	15	DDR2-533C
48	0.25	12	DDR2-667C
60	0.25	15	DDR2-667D
40	0.25	10	DDR2-800C
50	0.25	12.5	DDR2-800D
60	0.25	15	DDR2-800E

Calculation Examples for t_{AAmin}

SDRAM suppliers may support more CAS latency values than the JEDEC required minimum, so the calculations shown here should be performed for all supported CL values.

Example 1: DDR2-533B

- t_{CKmin} @ CL=3 is 3.75 ns
- t_{CKmin} @ CL=4 is 3.75 ns
- $t_{AAmin} = \min(3 * 3.75, 4 * 3.75) = 11.25$ ns

Example 2: DDR2-800D

- t_{CKmin} @ CL=4 is 3.75 ns
- t_{CKmin} @ CL=5 is 2.5 ns
- $t_{AAmin} = \min(4 * 3.75, 5 * 2.5) = 12.5$ ns

CAS Latency Calculation and Examples

CAS latency is not a purely analog value as DDR2 SDRAMs use the DLL to synchronize data and strobe outputs with the clock. All possible frequencies may not be tested, therefore an application should use the next smaller JEDEC standard tCKmin value (5.0, 3.75, 3.0, or 2.5 ns) when calculating CAS Latency. This section shows how the BIOS calculates CAS latency based on Bytes 11 ~ 14.

Step 1: The BIOS first determines the common operating frequency of all modules in the system, ensuring that the corresponding value of tCK (tCKactual) falls between tCKmin (Byte 11) and tCKmax (Byte 12). If tCKactual is not a JEDEC standard value, the next smaller standard tCKmin value is used for calculating CAS Latency.

Step 2: The BIOS then calculates the “desired” CAS Latency (CLdesired):

$$CL_{desired} = \text{ceiling} (tA_{min} / tCK_{actual})$$

where tAmin is defined in Byte 14. The ceiling function requires that the quotient be rounded up always.

Step 3: The BIOS then determines the “actual” CAS Latency (CLactual):

$$CL_{actual} = \text{max} (CL_{desired}, \text{min CL supported})$$

where min CL supported is found in the least significant nibble of Byte 13.

Example 1: DDR2-533C 4-4-4 module operating at 533

$$tA_{min} = 15 \text{ ns}$$

$$\text{Min CL} = 3, \text{ range} = 3 \text{ (CL} = 3, 4, 5 \text{ supported)}$$

$$tCK_{actual} = 3.75 \text{ ns (266 MHz Clock)}$$

$$CL_{desired} = \text{ceiling} (15 / 3.75) = 4$$

$$CL_{actual} = \text{max} (4, 3) = 4$$

Example 2: DDR2-667C 4-4-4 standard latency module operating at 533

$$tA_{min} = 12 \text{ ns}$$

$$\text{Min CL} = 4, \text{ range} = 3 \text{ (CL} = 4, 5, 6 \text{ supported)}$$

$$tCK_{actual} = 3.75 \text{ ns (266 MHz Clock)}$$

$$CL_{desired} = \text{ceiling} (12 / 3.75) = 4$$

$$CL_{actual} = \text{max} (4, 4) = 4$$

Example 3: DDR2-667 4-4-4 fast latency module operating at 533 (downshifting to 3-3-3)

$$tA_{min} = 11.25 \text{ ns (chosen to allow CL=3 at 533, exceeds value required to meet minimum JEDEC standard)}$$

$$\text{Min CL} = 3, \text{ range} = 3 \text{ (CL} = 3, 4, 5 \text{ supported)}$$

$$tCK_{actual} = 3.75 \text{ ns (266 MHz Clock)}$$

$$CL_{desired} = \text{ceiling} (11.25 / 3.75) = 3$$

$$CL_{actual} = \text{max} (3, 3) = 3$$

Example 4: DDR2-800D 5-5-5 module operating at 313 (debug & hardware bringup scenario)

$$tA_{min} = 12.5 \text{ ns}$$

$$\text{Min CL} = 4, \text{ range} = 3 \text{ (CL} = 4, 5, 6 \text{ supported)}$$

$$tCK_{actual} = 3.2 \text{ ns (156 MHz Clock) reduced to next lower JEDEC standard tCKmin} = 3.0 \text{ ns}$$

$$CL_{desired} = \text{ceiling} (12.5 / 3.0) = 5$$

$$CL_{actual} = \text{max} (5, 4) = 5$$

Byte 15: Write Recovery Times Supported

This field describes the Write Recovery (WR) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of WR, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support WR values of 2 and 3 would program a WR Range of 2 and a minimum WR of 2: 0010 0010 = 0x22.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
WR Range (clocks)	Minimum WR (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 All other values TBD	Bit [3, 2, 1, 0] : 0010 = 2 All other values TBD

Byte 16: Write Recovery Time (t_{WR})

This byte defines the SDRAM write recovery time in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Minimum Write Recovery Time (t_{WR}) MTB Units
Values defined from 1 to 255

Example:

t_{WR} (MTB units)	Timebase (ns)	t_{WR} Result (ns)	Use
60	0.25	15	All DDR2 speed grades

Byte 17: Write Latencies Supported

This field describes the Write Latency (WL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of WL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support WL values of 2, 3, and 4 would program a WL Range of 3 and a minimum WL of 2: 0011 0010 = 0x32.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
WL Range (clocks)	Minimum WL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 All other values TBD	Bit [3, 2, 1, 0] : 0010 = 2 All other values TBD

Byte 18: Additive Latencies Supported

This field describes the Additive Latency (AL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of AL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support AL values of 0, 1, 2, and 3 would program a AL Range of 4 and a minimum AL of 0: 0100 0000 = 0x40.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
AL Range (clocks)	Minimum AL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 All other values TBD	Bit [3, 2, 1, 0] : 0000 = 0 All other values TBD

Byte 19: Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (t_{RCD})

This byte defines the SDRAM RAS# to CAS# Delay in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Minimum RAS# to CAS# Delay (t_{RCD}) MTB Units
Values defined from 1 to 255

Examples:

tRCD (MTB units)	Timebase (ns)	tRCD Result (ns)	Use
60	0.25	15	3 clocks at DDR2-400B
80	0.25	20	4 clocks at DDR2-400C
45	0.25	11.25	3 clocks at DDR2-533B
60	0.25	15	4 clocks at DDR2-533C
48	0.25	12	4 clocks at DDR2-667C
60	0.25	15	5 clocks at DDR2-667D
40	0.25	10	4 clocks at DDR2-800C
50	0.25	12.5	5 clocks at DDR2-800D
60	0.25	15	6 clocks at DDR2-800E

Byte 20: Minimum Row Active to Row Active Delay (t_{RRD})

This byte defines the minimum SDRAM Row Active to Row Active Delay in medium timebase units.

Bit 7 ~ Bit 0
Minimum Row Active to Row Active Delay (t_{RRD}) MTB Units
Values defined from 1 to 255

Examples:

tRRD (MTB units)	Timebase (ns)	tRRD Result (ns)	Use
30	0.25	7.5	For SDRAMs with 1KB page size
40	0.25	10	For SDRAMs with 2KB page size

Byte 21: Minimum Row Precharge Time (t_{RP})

This byte defines the SDRAM minimum Row Precharge Time Delay in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Minimum Row Precharge Time (t_{RP}) MTB Units
Values defined from 1 to 255

Examples:

tRP (MTB units)	Timebase (ns)	tRP Result (ns)	Use
60	0.25	15	3 clocks at DDR2-400B
80	0.25	20	4 clocks at DDR2-400C
45	0.25	11.25	3 clocks at DDR2-533B
60	0.25	15	4 clocks at DDR2-533C
48	0.25	12	4 clocks at DDR2-667C
60	0.25	15	5 clocks at DDR2-667D
40	0.25	10	4 clocks at DDR2-800C
50	0.25	12.5	5 clocks at DDR2-800D
60	0.25	15	6 clocks at DDR2-800E

Byte 22: Upper Nibbles for t_{RAS} and t_{RC}

This byte defines the most significant nibbles for the values of t_{RAS} (byte 23) and t_{RC} (byte 24).

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
t_{RC} Most Significant Nibble	t_{RAS} Most Significant Nibble
See Byte 24 description	See Byte 23 description

Byte 23: Minimum Active to Precharge Time (t_{RAS})

The lower nibble of Byte 22 and the contents of Byte 23 combined create a 12-bit value which defines the SDRAM minimum Active to Precharge Time Delay in medium timebase (MTB) units. The most significant bit is Bit 3 of Byte 22, and the least significant bit is Bit 0 of Byte 23.

Byte 22 Bit 3 ~ Bit 0, Byte 23 Bit 7 ~ Bit 0
Minimum Active to Precharge Time (t_{RAS}) MTB Units
Values defined from 1 to 4095

Examples:

tRAS (MTB units)	Timebase (ns)	tRAS Result (ns)	Use
180	0.25	45	9 clocks at DDR2-400C 12 clocks at DDR2-533 15 clocks at DDR2-667 18 clocks at DDR2-800
160	0.25	40	8 clocks at DDR2-400B
320	0.125	40	16 clocks at DDR3-800 (e.g.)

Byte 24: Minimum Active to Active/Refresh Time (t_{RC})

The upper nibble of Byte 22 and the contents of Byte 24 combined create a 12-bit value which defines the SDRAM minimum Active to Active/Refresh Time Delay in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 22, and the least significant bit is Bit 0 of Byte 24.

Byte 22 Bit 7 ~ Bit 4, Byte 24 Bit 7 ~ Bit 0
Minimum Active to Active/Refresh Time (t_{RC}) MTB Units
Values defined from 1 to 4095

Examples:

tRC (MTB units)	Timebase (ns)	tRC Result (ns)	Use
260	0.25	65	13 clocks at DDR2-400C
220	0.25	55	11 clocks at DDR2-400B
240	0.25	60	16 clocks at DDR2-533C
225	0.25	56.25	15 clocks at DDR2-533B
240	0.25	60	20 clocks at DDR2-667D
228	0.25	57	19 clocks at DDR2-667C
220	0.25	55	22 clocks at DDR2-800E
210	0.25	52.5	21 clocks at DDR2-800D
200	0.25	50	20 clocks at DDR2-800C

Byte 25: Minimum Refresh Recovery Time Delay (t_{RFC}), Least Significant Bits
Byte 26: Minimum Refresh Recovery Time Delay (t_{RFC}), Most Significant Bits

The contents of Byte 25 and the contents of Byte 26 combined create a 16-bit value which defines the SDRAM minimum Refresh Recovery Time Delay in medium timebase (MTB) units. The most significant bit is Bit 7 of Byte 26, and the least significant bit is Bit 0 of Byte 25.

Byte 26 Bit 7 ~ Bit 0, Byte 25 Bit 7 ~ Bit 0
Minimum Refresh Recover Time Delay (t_{RFC}) MTB Units
Values defined from 1 to 65535

Examples:

tRFC (MTB units)	Timebase (ns)	tRFC Result (ns)	Use
300	0.25	75	15 clocks at DDR2-400 20 clocks at DDR2-533 25 clocks at DDR2-667 30 clocks at DDR2-800
420	0.25	105	21 clocks at DDR2-400 28 clocks at DDR2-533 35 clocks at DDR2-667 42 clocks at DDR2-800
510	0.25	127.5	25.5 clocks at DDR2-400 * 34 clocks at DDR2-533 42.5 clocks at DDR2-667 * 51 clocks at DDR2-800
780	0.25	195	39 clocks at DDR2-400 52 clocks at DDR2-533 65 clocks at DDR2-667 78 clocks at DDR2-800
1310	0.25	327.5	65.5 clocks at DDR2-400 * 87.3 clocks at DDR2-533 * 109.2 clocks at DDR2-667 * 131 clocks at DDR2-800
* Systems must round to the next higher integer value when calculating the number of clocks.			

Byte 27: Minimum Internal Write to Read Command Delay (t_{WTR})

This byte defines the SDRAM internal write to read time in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Internal Write to Read Delay Time (t_{WTR}) MTB Units
Values defined from 1 to 255

Examples:

t_{WTR} (MTB units)	Timebase (ns)	t_{WTR} Result (ns)	Use
40	0.25	10	DDR2-400
30	0.25	7.5	DDR2-533, DDR2-667, DDR2-800

Byte 28: Minimum Internal Read to Precharge Command Delay (t_{RTP})

This byte defines the SDRAM internal Read to Precharge delay time in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Internal Read to Precharge Delay Time (t_{RTP}) MTB Units
Values defined from 1 to 255

Examples:

t_{RTP} (MTB units)	Timebase (ns)	t_{RTP} Result (ns)	Use
30	0.25	7.5	All DDR2 speed bins

Byte 29: Burst Lengths Supported

This byte defines the read burst lengths supported by the SDRAM on this module.

Bit 7	Bit 6 ~ 2	Bit 1	Bit 0
Burst Chop	TBD	BL = 8	BL = 4
0 = Not Supported 1 = Supported		0 = Not Supported 1 = Supported	0 = Not Supported 1 = Supported

Byte 30: Terminations Supported

This byte defines the on-die termination values supported by the SDRAM on this module.

Bit 7 ~ Bit 3	Bit 2	Bit 1	Bit 0
TBD	50 Ω ODT	75 Ω ODT	150 Ω ODT
	0 = Not Supported 1 = Supported	0 = Not Supported 1 = Supported	0 = Not Supported 1 = Supported

Byte 31: Drivers Supported

This byte defines the optional drive strengths supported by the SDRAM on this module.

Bit 7 ~ Bit 1	Bit 0
TBD	Weak Driver
	0 = Not Supported 1 = Supported

Byte 32: Average SDRAM Refresh Interval (t_{REFI})

This byte describes the module's average refresh rate over the standard operating temperature range.

Bit 7	Bit 6	Bit 5 ~ Bit 4	Bit 3 ~ Bit 0
Double Refresh Requirement	High Temperature Self-Refresh	TBD	Average Refresh Interval (t_{REFI}) μ S
See bit description below	See bit description below		Bit [3, 2, 1, 0] : 0000 = 15.625 (normal) 0001 = 3.9 (reduced 0.25x) 0010 = 7.8 (reduced 0.5x) 0011 = 31.3 (extended 2x) 0100 = 62.5 (extended 4x) 0101 = 125 (extended 8x) All other values TBD

Bit 7 defines whether or not double refresh is required for SDRAM case temperature exceeding 85 °C.

Bit 7	Byte 32, Bit 7
0	Do not need double refresh rate for the proper operation at the SDRAM maximum case temperature above 85 °C. The SDRAM maximum case temperature is specified at Byte 33.
1	Requires double refresh rate for the proper operation at the SDRAM maximum case temperature above 85 °C. The SDRAM maximum case temperature is specified at Byte 33.

Bit 6 indicates DDR2 SDRAM "High Temperature Self-Refresh" support.

Bit 6	Byte 32, Bit 6
0	SDRAM does not support high temperature self-refresh entry. Controller must ensure SDRAM cool down to $T_{case} < 85$ °C before entering self-refresh
1	SDRAM high temperature self-refresh entry supported. When needed, controller may set SDRAM in high temperature self-refresh mode via EMRS(2) [A7] and be able to enter self-refresh above 85 °C T_{case} temperature

Byte 33: Tcasemax

This byte is split into two nibbles. The higher order nibble (bits 4:7) describes the SDRAM case temperature difference between maximum case temperature and the baseline maximum case temperature of 85 °C. Unit for this field is 2 °C. The SDRAM maximum case temperature is 85 °C plus the value in bits 4:7. If bits 4:7 is zero, the SDRAM device only supports up to 85 °C maximum case temperature and users must ensure the case temperature will not exceed 85 °C in any operation. If bits 4:7 is non-zero, the maximum case temperature range is extended and users must look at byte 32 bit 7 for the proper operation at this extended case temperature.

Byte 33: Tcasemax, Subfield A: 2 °C (Bits 7:4)										
Line #	Tcasemax (Unit: 2 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	0	0	0	0	0	See Subfield B	See Subfield B	See Subfield B	See Subfield B	0-
1A	2	0	0	0	1					1-
2A	4	0	0	1	0					2-
3A	6	0	0	1	1					3-
4A	8	0	1	0	0					4-
5A	10	0	1	0	1					5-
6A	12	0	1	1	0					6-
7A	14	0	1	1	1					7-
8A	16	1	0	0	0					8-
9A	18	1	0	0	1					9-
10A	20	1	0	1	0					A-
.
.
14A	28	1	1	1	0					E-
15A	Exceed 30	1	1	1	1					F-

The lower order nibble (bits 0:3) describes DT4R4W Delta (the SDRAM case temperature rise difference from ambient due to IDD4R/page open burst read vs. IDD4W/page open burst write operations) at VDD = 1.9 V, in unit of 0.4 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for the definitions of IDD4R and IDD4W operations. Please refer to Notes 5 & 6 of the "1.1 Address Map table" of this spec for calculation of temperature rise.

Byte 33: DT4R4W Delta, Subfield B: 0.4 °C (Bits 0:3)										
Line #	DT4R4W Delta (Granularity: 0.4 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Not Supported	See Subfield A	See Subfield A	See Subfield A	See Subfield A	0	0	0	0	-0
1A	0.4					0	0	0	1	-1
2A	0.8					0	0	1	0	-2
3A	1.2					0	0	1	1	-3
4A	1.6					0	1	0	0	-4
5A	2.0					0	1	0	1	-5
6A	2.4					0	1	1	0	-6
7A	2.8					0	1	1	1	-7
8A	3.2					1	0	0	0	-8
9A	3.6					1	0	0	1	-9
10A	4.0					1	0	1	0	-A
.
.
14A	5.6					1	1	1	0	-E
15A	Exceed 6.0					1	1	1	1	-F

Byte 34: Thermal Resistance of SDRAM Package from Top (Case) to Ambient ($\Psi_{T-A \text{ SDRAM}}$)

This byte describes the thermal resistance of SDRAM package from top (case) to ambient and it is based on JESD51-3 "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages" under JESD51-2 standard. Unit for this field is 0.5°C/W .

Byte 34: Thermal Resistance of SDRAM Package from Top (Case) to Ambient ($\Psi_{T-A \text{ SDRAM}}$)									
Psi T-A SDRAM (Granularity: 0.5°C/W)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Defined	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.
.
16.0	0	0	1	0	0	0	0	0	20
.
.
30.0	0	0	1	1	1	1	0	0	3C
.
.
127	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 35: SDRAM Case Temperature Rise from Ambient due to Activate-Precharge (DT0)

In this byte, bits 7:2 describe DT0 (SDRAM case temperature rise from ambient due to IDD0/activate-pre-charge operation minus 2.8 °C offset temperature), in units of 0.3 °C. This value plus 2.8 °C is the SDRAM case temperature rise from ambient. Please refer to JEDEC DDR2 SDRAM Component Specification for the definition of IDD0 operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise. Bits 1:0 are reserved for future use in describing SDRAM thermal characteristics.

Byte 35: DT0								
Line #	DT0 (Granularity: 0.3 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1 ~ Bit 0
0	Not Defined	0	0	0	0	0	0	
1	0.3	0	0	0	0	0	1	
2	0.6	0	0	0	0	1	0	
3	0.9	0	0	0	0	1	1	
4	1.2	0	0	0	1	0	0	
5	1.5	0	0	0	1	0	1	
6	1.8	0	0	0	1	1	0	Reserved
7	2.1	0	0	0	1	1	1	
8	2.4	0	0	1	0	0	0	
9	2.7	0	0	1	0	0	1	
10	3.0	0	0	1	0	1	0	
.	
.	
254	18.6	1	1	1	1	1	1	
255	Exceed 18.6	1	1	1	1	1	1	

Byte 36: SDRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)

For Unbuffered DIMM, this describes the SDRAM case temperature rise from ambient due to IDD2N/precharge standby operation (DT2N) at VDD = 1.9 V, in unit of 0.1 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for the definition of IDD2N operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

For Registered and Fully Buffered DIMMs, this byte describes the SDRAM case temperature rise from ambient due to IDD2Q/precharge quiet standby operation (DT2Q) at VDD = 1.9 V, in unit of 0.1 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for the definition of IDD2Q operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT2N/2Q (Granularity: 0.1 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.1	0	0	0	0	0	0	0	1	01
0.2	0	0	0	0	0	0	1	0	02
0.3	0	0	0	0	0	0	1	1	03
0.4	0	0	0	0	0	1	0	0	04
.
.
3.2	0	0	1	0	0	0	0	0	20
.
.
6.0	0	0	1	1	1	1	0	0	3C
.
.
25.4	1	1	1	1	1	1	1	0	FE
Exceed 25.5	1	1	1	1	1	1	1	1	FF

Byte 37: SDRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)

This byte describes the SDRAM case temperature rise from ambient due to IDD2P/precharge power-down operation at VDD = 1.9 V, in unit of 0.015 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for IDD2P operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT2P (Granularity: 0.015 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.015	0	0	0	0	0	0	0	1	01
0.030	0	0	0	0	0	0	1	0	02
0.045	0	0	0	0	0	0	1	1	03
0.060	0	0	0	0	0	1	0	0	04
.
.
0.480	0	0	1	0	0	0	0	0	20
.
.
0.900	0	0	1	1	1	1	0	0	3C
.
.
3.810	1	1	1	1	1	1	1	0	FE
Exceed 3.825	1	1	1	1	1	1	1	1	FF

Byte 38: SDRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)

This byte describes the SDRAM case temperature rise from ambient due to IDD3N/active standby operation at VDD = 1.9 V, in unit of 0.15 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for IDD3N operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT3N (Granularity: 0.15 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.15	0	0	0	0	0	0	0	1	01
0.30	0	0	0	0	0	0	1	0	02
0.45	0	0	0	0	0	0	1	1	03
0.60	0	0	0	0	0	1	0	0	04
.
.
4.80	0	0	1	0	0	0	0	0	32
.
.
9.00	0	0	1	1	1	1	0	0	3C
.
.
38.10	1	1	1	1	1	1	1	0	FE
Exceed 38.25	1	1	1	1	1	1	1	1	FF

Byte 39: SDRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)

This byte is split into two fields: bits 1:7 describes the SDRAM case temperature rise from ambient due to IDD4R/page open read operation at VDD = 1.9 V, in unit of 0.4 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for the definition of IDD4R operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise. Bit 0 specifies if DT4W (Case temperature rise from ambient due to page open burst write) is greater than or less than DT4R.

Byte 39: DT4R, Subfield A: 0.4 °C (Bits 1:7)									
Line #	DT4R (Granularity: 0.4 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	Not Supported	0	0	0	0	0	0	0	See Sub-field B
1A	0.4	0	0	0	0	0	0	1	
2A	0.8	0	0	0	0	0	1	0	
3A	1.2	0	0	0	0	0	1	1	
4A	1.6	0	0	0	0	1	0	0	
5A	2.0	0	0	0	0	1	0	1	
6A	2.4	0	0	0	0	1	1	1	
7A	2.8	0	0	0	1	0	0	0	
8A	3.2	0	0	0	1	0	0	1	
9A	3.6	0	0	0	1	0	1	0	
10A	4.0	0	0	0	1	0	1	1	
.	
.	
126A	50.4	1	1	1	1	1	1	0	
127A	Exceed 50.8	1	1	1	1	1	1	1	

Byte 39: DT4R4W Mode Bit, Subfield B: 0.4 °C (Bit 0)									
Line #	DT4R4W Mode Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	DT4W is greater than DT4R	See Subfield A							0
1A	DT4W is less than DT4R	See Subfield A							1

Byte 40: SDRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B)

This byte describes the SDRAM case temperature rise from ambient due to IDD5B/burst refresh operation at VDD = 1.9 V, in unit of 0.5 °C. Please refer to JEDEC DDR2 SDRAM Component Specification for the definition of IDD5B operation. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT5B (Granularity: 0.5 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.
.
16.0	0	0	1	0	0	0	0	0	20
.
.
30.0	0	0	1	1	1	1	0	0	3C
.
.
127.0	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 41: SDRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7)

This byte describes the SDRAM case temperature rise from ambient due to IDD7/bank interleave read with auto-precharge operation at VDD = 1.9 V, in unit of 0.5 °C. Please refer to Notes 5 & 6 of the “1.1 Address Map table” of this spec for calculation of temperature rise. Note that for four-bank devices, IDD7 is based on four activates per tRC. For eight-bank devices, IDD7 is based on four activates per tFAW. For the tFAW definition, see JEDEC Council Ballot JCB04-013.

DT7 (Granularity: 0.5 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.
.
16.0	0	0	1	0	0	0	0	0	20
.
.
30.0	0	0	1	1	1	1	0	0	3C
.
.
127.0	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Bytes 42-59: Reserved

An Illustration Example of DT in SPD

This section shows an example of programming SPD Bytes 33 ~ 41. All the numbers in the tables below are arbitrary and for the sole purpose of demonstrating how to program these bytes. They are NOT intended to reflect any actual device properties.

DT in SPD										Example For Reference Only			
BYTE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex	Parameter Description	Parameter Value	Byte Value	Byte Unit
33	0	0	0	0	0	0	1	0	02	Tcasemax / DT4R4W Delta = DT (7 mA)	85 °C/0.84 °C	0 / 2	0.4 °C
34	0	1	1	1	1	1	1	0	7E	Psi T-A SDRAM	63.2 °C/W	126	0.5 °C/W
35	0	1	0	0	0	1	0	0	44	DT0 = DT (65 mA)	4.98 °C	Bits 7:2 17	0.3 °C
36 (UDIMM)	0	0	1	0	0	0	1	0	22	DT2N = DT (28 mA)	3.35 °C	34	0.1 °C
36 (RDIMM or FB-DIMM)	0	0	0	1	0	1	1	1	17	DT2Q = DT (19 mA)	2.27 °C	23	0.1 °C
37	0	0	0	1	1	0	0	0	18	DT2P = DT (3 mA)	0.36 °C	24	0.015 °C
38	0	0	0	1	1	0	0	1	19	DT3N = DT (31 mA)	3.71 °C	25	0.15 °C
39	0	0	1	0	1	0	1	0	2A	DT4R = DT(70 mA) / DT4R4W Mode bit	8.38 °C/0	21	0.4 °C
40	0	0	0	1	1	1	1	1	1F	DT5B = DT (128 mA)	15.32 °C	31	0.5 °C
41	0	0	1	0	1	0	0	0	28	DT7 = DT (165 mA)	19.8 °C	40	0.5 °C

In the example listed in the table above, Psi T-A SDRAM true value is 63.2 °C/W and unit is 0.5 °C/W. The byte value is determined as follows: $63.2 / 0.5 = 126.4$. Since 126.4 is closer to 126 than it is to 127, the programmed SPD byte value is rounded off to 126.

Also in the example listed in the table above, SPD Byte value for DT0 is calculated as following:

$$DT0 = IDD0 \text{ fast} * 1.9 \text{ V} * \text{Programmed value of Psi T-A SDRAM}$$

$$= 65 \text{ mA} * 1.9 \text{ V} * (\text{Value in Byte 34} * \text{Byte 34 Unit})$$

$$= 65 \text{ mA} * 1.9 \text{ V} * (126 * 0.5 \text{ C/W})$$

$$= 7.78 \text{ °C}$$

Note that the DT0 parameter value is defined as (case temperature rise - 2.8 °C offset) = $7.78 - 2.8 = 4.98 \text{ °C}$

DT0 SPD byte unit is 0.3°C, $4.98 \text{ °C} / 0.3 \text{ °C} = 16.6$. Since 16.6 is closer to 17 than it is to 16, the resulting value is 17, which is programmed in SPD byte 35 (DT0) as hex value 44, assuming 0 values for bits 1 and 0).

2.2 Module-Specific Section: Bytes 60 to 116

This section contains fields which are specific to the Fully-Buffered DIMM.

Bytes 60-78: Reserved

Byte 79: FBD ODT Definition

This byte specifies the recommended values for the FBD ODT. ODT values defined here must be subset of the ODT defined in Byte 30 which is part of generic DRAM spec and describes ODT supported by DRAM.

If both ODT ranks are disabled (Byte 79 = 0x00), the BIOS should use SPD Byte 7 to lookup the recommended ODT values according to the FB-DIMM Design Specification. Note that the ODT values may not be optimal, and some designs may not be distinguishable from others.

Bits 7~6	Bit 5 ~ Bit 4	Bits 3~2	Bit 1 ~ Bit 0
TBD	Rank 1 ODT	TBD	Rank 0 ODT
	00 = Disabled 01 = 75 Ω 10 = 150 Ω 11 = 50 Ω		00 = Disabled 01 = 75 Ω 10 = 150 Ω 11 = 50 Ω

Byte 80: Reserved

Byte 81: Channel Protocols Supported, Least Significant Byte

Byte 82: Channel Protocols Supported, Most Significant Byte

This two-byte field describes the channel protocols that are supported by the module. DIMMs must support at least one of these modes and may support more than one. From this data the BIOS can infer the width of the northbound channel as well as the supported level of error correction.

Byte 82, Bit 7 ~ Bit 0, Byte 81, Bit 7 ~ Bit 2	Byte 81, Bit 1	Byte 81, Bit 0
TBD	DDR2 Base ECC Protocol (10 SB, 13 NB & 14 NB bit lanes)	DDR2 Base Non-ECC Protocol (10 SB, 12 NB bit lanes)
	0 = Not Supported 1 = Supported	0 = Not Supported 1 = Supported

Byte 83: Back-to-back Turnaround Cycles

This byte describes the minimum number of additional clock cycles required between specific SDRAM commands. “Additional clock cycles” are those required beyond the normal minimum command spacing for the same command sequences as documented in the SDRAM data sheet. Inserting additional clock cycles avoids contention on the DQS signals at higher bandwidths. Note that the read-to-read turnaround refers to consecutive reads from different ranks and is not applicable to single-rank modules. Read-to-write and write-to-read turnaround apply to single-rank or multi-rank modules.

Bit 7 ~ Bit 6	Bit 5 ~ Bit 4	Bit 3 ~ Bit 2	Bit 1 ~ Bit 0
TBD	Read-to-Write	Write-to-Read	Rank Read-to-Read
	00 = 0 additional clocks 01 = 1 additional clock 10 = 2 additional clocks 11 = Undefined	00 = 0 additional clocks 01 = 1 additional clock 1X = TBD	00 = 0 additional clocks 01 = 1 additional clock 1X = TBD

Byte 84: Buffer Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)

This field describes the buffer read access time for operation with AMB.LINKPARNXT[1:0] set to 11; this byte should be copied to register AMB.CMD2DATANXT when the AMB is operating in this mode. The access time is defined as the sum of all delays (less tCAS + tAL) from the time a southbound FB-DIMM channel command is received at the AMB to the time when the AMB can drive the read data onto the northbound FB-DIMM channel. This parameter excludes delays due to channel deskew and frame alignment as well as I/O cell delays for channel transmit and receive buffers. The high order nibble provides the coarse-granularity delay as measured in multiples of tCK. The lower-order nibble provides the fine-granularity delay as measured in FB-DIMM channel unit intervals (UI). One UI is equal to tCK/12.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Read Access Coarse Granularity (tCK)	Read Access Fine Granularity (UI)
0000 = 0 * tCK 0001 = 1 * tCK 0010 = 2 * tCK 0011 = 3 * tCK 0100 = 4 * tCK 0101 = 5 * tCK 0110 = 6 * tCK 0111 = 7 * tCK 1000 = 8 * tCK 1001 = 9 * tCK All other values TBD	0000 = 0 * UI 0001 = 1 * UI 0010 = 2 * UI 0011 = 3 * UI 0100 = 4 * UI 0101 = 5 * UI 0110 = 6 * UI 0111 = 7 * UI 1000 = 8 * UI 1001 = 9 * UI 1010 = 10 * UI 1011 = 11 * UI All other values TBD

Byte 85: Buffer Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)

This field describes the buffer read access time for operation with AMB.LINKPARNXT[1:0] set to 10; this byte should be copied to register AMB.CMD2DATANXT when the AMB is operating in this mode. See the byte description for Byte 84 to determine how to calculate buffer read access time. The high order nibble provides the coarse-granularity delay as measured in multiples of tCK. The lower-order nibble provides the fine-granularity delay as measured in FB-DIMM channel unit intervals (UI). One UI is equal to tCK/12.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Read Access Coarse Granularity (tCK)	Read Access Fine Granularity (UI)
0000 = 0 * tCK	0000 = 0 * UI
0001 = 1 * tCK	0001 = 1 * UI
0010 = 2 * tCK	0010 = 2 * UI
0011 = 3 * tCK	0011 = 3 * UI
0100 = 4 * tCK	0100 = 4 * UI
0101 = 5 * tCK	0101 = 5 * UI
0110 = 6 * tCK	0110 = 6 * UI
0111 = 7 * tCK	0111 = 7 * UI
1000 = 8 * tCK	1000 = 8 * UI
1001 = 9 * tCK	1001 = 9 * UI
All other values TBD	1010 = 10 * UI
	1011 = 11 * UI
	All other values TBD

Byte 86: Buffer Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)

This field describes the buffer read access time for operation with AMB.LINKPARNXT[1:0] set to 01; this byte should be copied to register AMB.CMD2DATANXT when the AMB is operating in this mode. See the byte description for Byte 84 to determine how to calculate buffer read access time. The high order nibble provides the coarse-granularity delay as measured in multiples of tCK. The lower-order nibble provides the fine-granularity delay as measured in FB-DIMM channel unit intervals (UI). One UI is equal to tCK/12.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Read Access Coarse Granularity (tCK)	Read Access Fine Granularity (UI)
0000 = 0 * tCK	0000 = 0 * UI
0001 = 1 * tCK	0001 = 1 * UI
0010 = 2 * tCK	0010 = 2 * UI
0011 = 3 * tCK	0011 = 3 * UI
0100 = 4 * tCK	0100 = 4 * UI
0101 = 5 * tCK	0101 = 5 * UI
0110 = 6 * tCK	0110 = 6 * UI
0111 = 7 * tCK	0111 = 7 * UI
1000 = 8 * tCK	1000 = 8 * UI
1001 = 9 * tCK	1001 = 9 * UI
All other values TBD	1010 = 10 * UI
	1011 = 11 * UI
	All other values TBD

Byte 87: Thermal Resistance of AMB Package from Top (Case) to Ambient ($\Psi_{T-A\ AMB}$)

This byte describes the thermal resistance of AMB package from top (case) to ambient and it is based on JESD51-3 “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages” under JESD51-2 standard. Unit for this byte is $0.5\ ^\circ\text{C}/\text{W}$.

Byte 87: Thermal Resistance of AMB Package from Top (Case) to Ambient ($\Psi_{T-A\ AMB}$)									
$\Psi_{T-A\ AMB}$ (Granularity: $0.5\ ^\circ\text{C}/\text{W}$)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
0.5	0	0	0	0	0	0	0	1	01
1.0	0	0	0	0	0	0	1	0	02
1.5	0	0	0	0	0	0	1	1	03
2.0	0	0	0	0	0	1	0	0	04
.
.
16.0	0	0	1	0	0	0	0	0	20
.
.
30.0	0	0	1	1	1	1	0	0	3C
.
.
127	1	1	1	1	1	1	1	0	FE
Exceed 127.5	1	1	1	1	1	1	1	1	FF

Byte 88: AMB Case Temperature Rise from Ambient due to AMB in Idle_0 State (DT AMB Idle_0)

This byte describes the AMB case temperature rise from ambient due to AMB in Idle_0 state with clock running within spec, in units of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of Idle_0 operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Byte 89: AMB Case Temperature Rise from Ambient due to AMB in Idle_1 State (DT AMB Idle_1)

This byte describes the AMB case temperature rise from ambient due to AMB in Idle_1 state with clock running within spec, in unit of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of Idle_1 operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Byte 90: AMB Case Temperature Rise from Ambient due to AMB in Idle_2 State (DT AMB Idle_2)

This byte describes the AMB case temperature rise from ambient due to AMB in Idle_2 state with clock running within spec, in unit of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of Idle_2 operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Byte 91: AMB Case Temperature Rise from Ambient due to AMB in Active_1 State (DT AMB Active_1)

This byte describes the AMB case temperature rise from ambient due to AMB in Active_1 state with clock running within spec, in unit of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of Active_1 operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Byte 92: AMB Case Temperature Rise from Ambient due to AMB in Active_2 State (DT AMB Active_2)

This byte describes the AMB case temperature rise from ambient due to AMB in Active_2 state with clock running within spec, in unit of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of Active_2 operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Byte 93: AMB Case Temperature Rise from Ambient due to AMB in L0s State (DT AMB L0s)

This byte describes the AMB case temperature rise from ambient due to AMB in L0s state with clock running within spec, in unit of 1.0 °C. Please refer to JEDEC AMB Component Specification for the definition of L0s operation.

Please refer to Notes 8 & 10 of the “1.1 Address Map table” of this spec for calculation of temperature rise.

DT AMB Idle_0 (Granularity: 1.0 °C)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not Supported	0	0	0	0	0	0	0	0	00
1.0	0	0	0	0	0	0	0	1	01
2.0	0	0	0	0	0	0	1	0	02
3.0	0	0	0	0	0	0	1	1	03
4.0	0	0	0	0	0	1	0	0	04
.
.
32.0	0	0	1	0	0	0	0	0	20
.
.
60.0	0	0	1	1	1	1	0	0	3C
.
.
254.0	1	1	1	1	1	1	1	0	FE
Exceed 255.0	1	1	1	1	1	1	1	1	FF

Bytes 94-97: Reserved

Byte 98: AMB Case Temperature Maximum (Tcase_max)

In this byte, bits 4~0 describe the maximum AMB Case Temperature (Tcase) allowed during operation. The encoding "00000" is a special case, and defaults to a Tcase_max of 110 °C, the maximum "package surface (case) temperature". Bits 7~5 are reserved for future use in describing AMB thermal characteristics.

Byte 98: Tcase_max						
Tcase_max (Granularity: 1 °C)	Bit 7~5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
110 °C (default)		0	0	0	0	0
95 °C (reserved)		0	0	0	0	1
96 °C (reserved)		0	0	0	1	0
97 °C (reserved)		0	0	0	1	1
...	
104 °C (reserved)		0	1	0	1	0
105 °C (reserved)		0	1	0	1	1
106 °C (reserved)		0	1	1	0	0
107 °C (reserved)	Reserved	0	1	1	0	1
108 °C (reserved)		0	1	1	1	0
109 °C (reserved)		0	1	1	1	1
110 °C		1	0	0	0	0
111 °C		1	0	0	0	1
112 °C		1	0	0	1	0
113 °C		1	0	0	1	1
...						
124 °C		1	1	1	1	0
125 °C or greater		1	1	1	1	1

Notes:

1. The rows from 95 °C to 109 °C are reserved for future use if and when needed, but are not currently conforming values for the approved version of the AMB specification. Current AMB specification for Tcase_max is 110 °C.
2. Tcase (Case Temperature); the surface temperature as measured at the back geometric center of the die (top of the package).

Bytes 99-100: Reserved**Bytes 101-106: AMB Personality Bytes: Pre-initialization**

This 6-byte field contains AMB-specific information that the BIOS is expected to copy directly to AMB registers. These bytes must be copied by the BIOS to registers AMB.PERSBYTE[0:5] before the link(s) to the AMB is (are) initialized. The specific definitions of these bytes should be defined in the data sheet for each manufacturer's AMB.

Bytes 107-114: AMB Personality Bytes: Post-initialization

This 8-byte field contains AMB-specific information that the BIOS is expected to copy directly to AMB registers. These bytes must be copied by the BIOS to registers AMB.PERSBYTE[6:13] after the link(s) to the AMB is (are) initialized. The specific definitions of these bytes should be defined in the data sheet for each manufacturer's AMB.

Byte 115: AMB Manufacturer ID Code, Least Significant Byte**Byte 116: AMB Manufacturer ID Code, Most Significant Byte**

This two-byte field indicates the manufacturer of the AMB on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 116, Bit 7 ~ Bit 0	Byte 115, Bit 7	Byte 115, Bit Bit 6 ~ Bit 0
Last non-zero byte, AMB Manufacturer	Odd parity for Byte 115, bits 6:0	Number of continuation codes, AMB Manufacturer
See JEP-106		See JEP-106

2.3 Unique Module ID: Bytes 117 to 125

Byte 117: Module Manufacturer ID Code, Least Significant Byte

Byte 118: Module Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 118, Bit 7 ~ Bit 0	Byte 117, Bit 7	Byte 117, Bit Bit 6 ~ Bit 0
Last non-zero byte, Module Manufacturer	Odd parity for Byte 117, bits 6:0	Number of continuation codes, Module Manufacturer
See JEP-106		See JEP-106

Byte 119: Module Manufacturing Location

The module manufacturer includes an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 120-121: Module Manufacturing Date

The module manufacturer includes a date code for the module. The JEDEC definitions for bytes 120 and 121 are year and week respectively. These bytes must be represented in Binary Coded Decimal (BCD). For example, week 47 in year 2003 would be coded as 03 (0000 0011) in byte 120 and 47 (0100 0111) in byte 121.

Bytes 122-125: Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

One method of achieving this is by assigning a byte in the field from 122-125 as a tester ID byte and using the remaining bytes as a sequential serial number. Bytes 117-125 will then result in a nine-byte unique module identifier. Note that part number is not included in this identifier: the supplier may not give the same value for Bytes 119:125 to more than one DIMM even if the DIMMs have different part numbers.

2.4 CRC: Bytes 126 to 127

Bytes 126-127: SPD Cyclical Redundancy Code (CRC)

This two-byte field contains the calculated 16-bit CRC-CCITT (polynomial $0x1021$) for previous bytes in the SPD. The following algorithm and data structures (shown in C) are to be followed in calculating and checking the code. Bit 7 of Byte 0 indicates which bytes are covered by the CRC. The polynomial calculated with this algorithm is $x^{16} + x^{12} + x^5 + 1$.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_126 = (char) (data16 & 0xFF);
SPD_byte_127 = (char) (data16 >> 8);
```

2.5 Other Manufacturer Fields and User Space: Bytes 128 to 255

Bytes 128-145: Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (0x20).

Bytes 146-147: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

Byte 148: SDRAM Manufacturer ID Code, Least Significant Byte

Byte 149: SDRAM Manufacturer ID Code, Most Significant Byte

This two-byte field indicates the manufacturer of the SDRAM on the module, encoded as follows: the first byte is the number of continuation bytes indicated in JEP-106; the second byte is the last non-zero byte of the manufacturer's ID code, again as indicated in JEP-106.

Byte 149, Bit 7 ~ Bit 0	Byte 148, Bit 7	Byte 148, Bit Bit 6 ~ Bit 0
Last non-zero byte, Module Manufacturer	Odd parity for Byte 148, bits 6:0	Number of continuation codes, Module Manufacturer
See JEP-106		See JEP-106

Bytes 150-175: Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Bytes 176-255: Open for Customer Use

These bytes are unused by the manufacturer and are open for customer use.

Appendix: ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

First Hex Digit in Pair	Second Hex Digit in Pair															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space							()					- Dash	.	
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

0x20 = Blank Space

0x34 = 4

0x41 = A

SPD Bytes 128-145	
Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D33323733344243442D323630592020

Revision Log

Date	Rev	Pages	Contents of Modification
Jan 2007	1.1	3, 36	Corrected typo: SPD byte 87 title
		4	Corrected typo: SPD byte 47 changed to SPD byte 87
		7	Added FB-DIMM height extension encoding to cover 40-50 mm (JC-45-06-243)
		3, 43	Changed AMB junction to case temperature (JC-45-06-297)
Mar. 2006	1.1	11	Extended range of CL
		15	Extended range of AL and WL
Jan. 2006	1.1	42	Added byte 98 (AMB Tjmax)
		32	Added byte 79 (Required ODT)
		28	Clarified sub-field indicators
		25	Corrected values for SPD entries, byte 35 (DT0)
		5	Changed revision from 1.0 to 1.1
Jan. 2005	1.0	All	Initial release