

**3.12.3 Silicon Pad Sequences**

**3.12.3.1 LPDRAM (SDR/DDR) Silicon Pad Sequence Guidelines  
(x16, x32, single/double-side, asymmetrical/ symmetrical design)**

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**3.12.3.1 LPDRAM (SDR/DDR) Silicon Pad Sequence Guidelines  
(x16, x32, single/double-side, asymmetrical/ symmetrical design)**

1. One pair VDDQ/VSSQ per 4DQs –place between DQ's (two DQs on each side of VDDQ/VSSQ)
2. DQS and DM must be within the data groups
  - 2B DQS and DM pairs located at end of data bytes toward center of die
  - 2C. DQ's should be in sequential order DQ [MAX:0]
  - 2D Sequential order of DQ's based on standard MCP and Pkg-on-Pkg electrical interfacialignmentand LPDRAM Status Register fixed lower word implementation
3. VDD/VSS core supply in center and at both edges of pad sequence, center may have multiple pairs.
4. VDDQ/VSSQ alternate across DQ groups for better routing
5. Clock needs to be at the die center for speed and symmetrical distribution.
  - 5A. One or two clk/clk# pairs are optional; if two, both pairs must be connected on silicon or package substrate.
6. Adjacent groups must be address and control, also for speed, the 5 non-address control lines (CKE, WE, CAS, RAS, CS) should be on the same side of the clock because of their inter-relations in the main chip state machine.
  - 6A.The Specific order of ctrl signals doesn't matter but should be CKE, WE, CAS, RAS, CS for standard purposes
7. Non-Standard signals (non-speed critical) should be located on outside ends of pad sequence on the less populated pad side (examples: TQ- Temp sense, DPD, etc.)
8. Keeping symmetry for x32 and x16 provides the added benefit of enabling a single design for the two widths
9. Doesn't need to conform to discrete LPDRAM ballout (non-stacked)
- 10.Address signals should be compatible to discrete LPSDR/DDR ballout [A4:15] and [A0:A3] groups

NOTE: NC pad locations may vary.

Seven examples are provided in Figures 3.12.3.1-1 through 7, for reference

- x32 Asymmetrical (example A)
- x16 Asymmetrical (example B)
- x16 Symmetrical (example C)
- x32 Symmetrical (example D)
- x32 Single Side (example E)
- x16 Single Side (example F)
- Super-bond layout pattern with Status Read Register locations (example G)



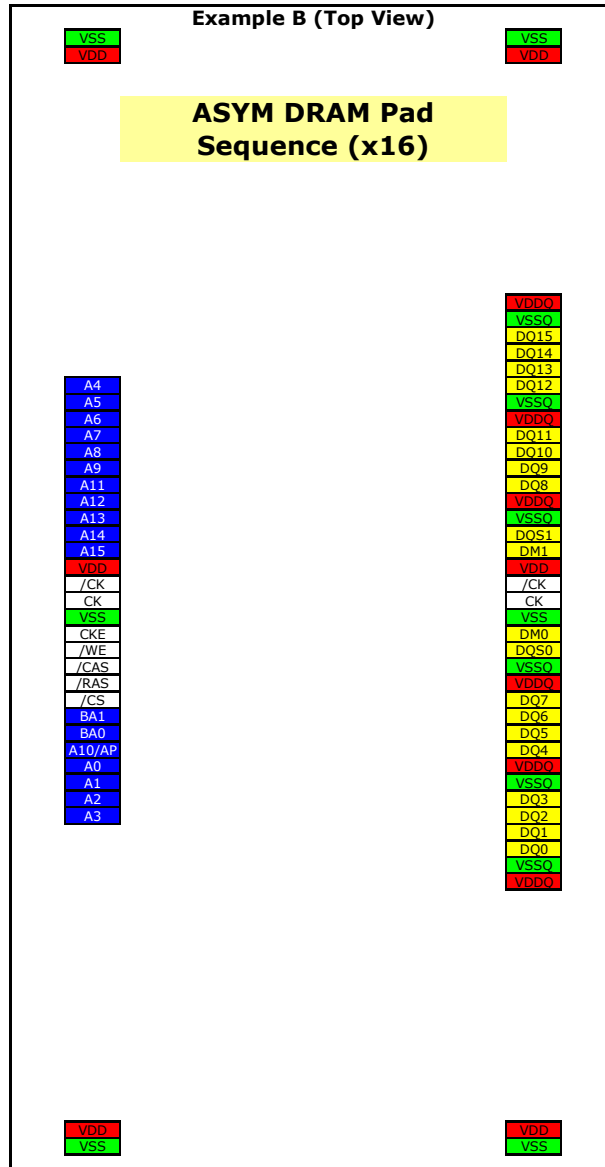


Figure 3.12.3.1-2 - Example B - Asymmetric DRAM Pad Sequence (x16)

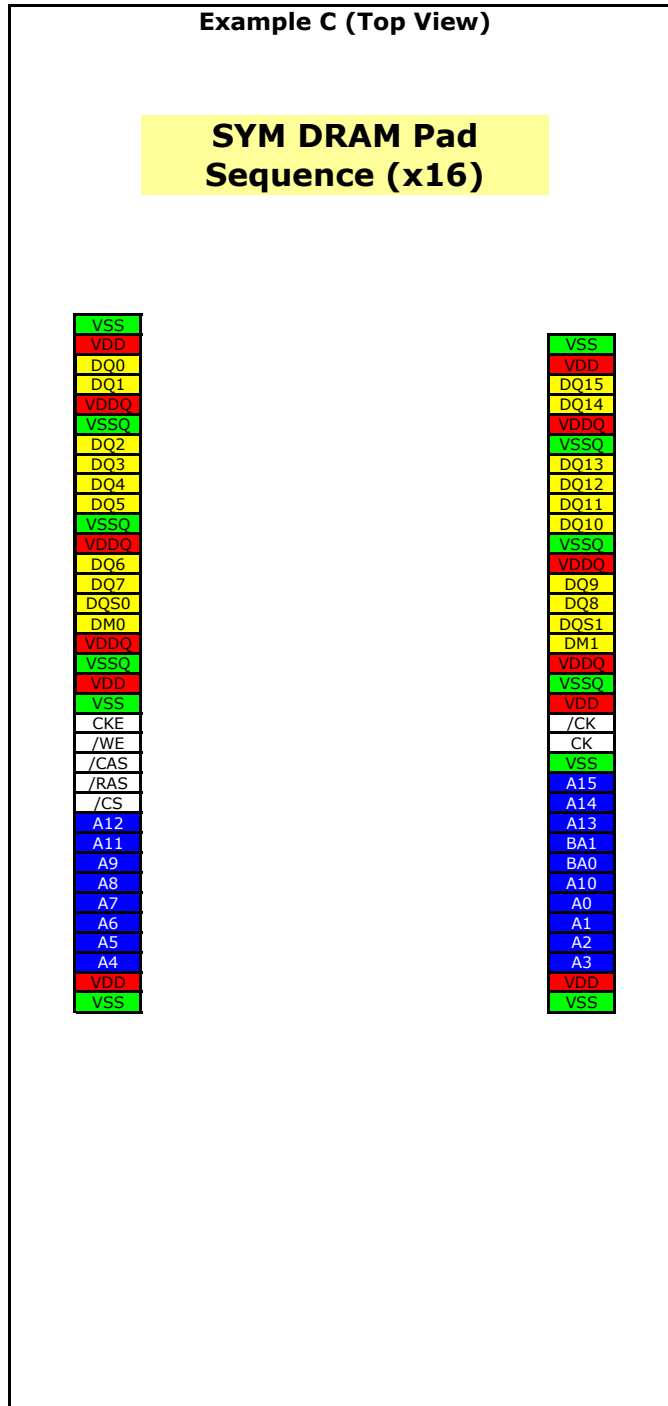


Figure 3.12.3.1-3 - Example C - Symetric DRAM Pad Sequence (x16)

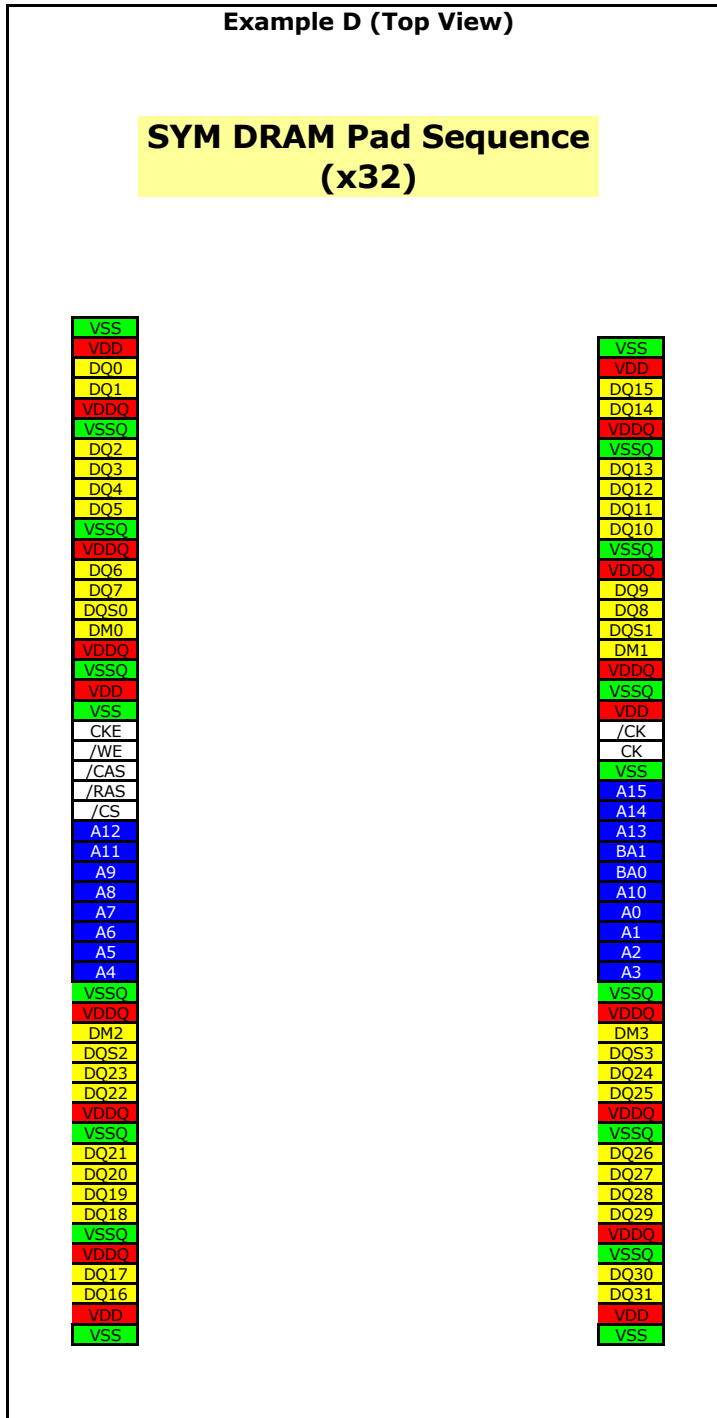


Figure 3.12.3.1-4 - Example D - Symetric DRAM Pad Sequence (x32)

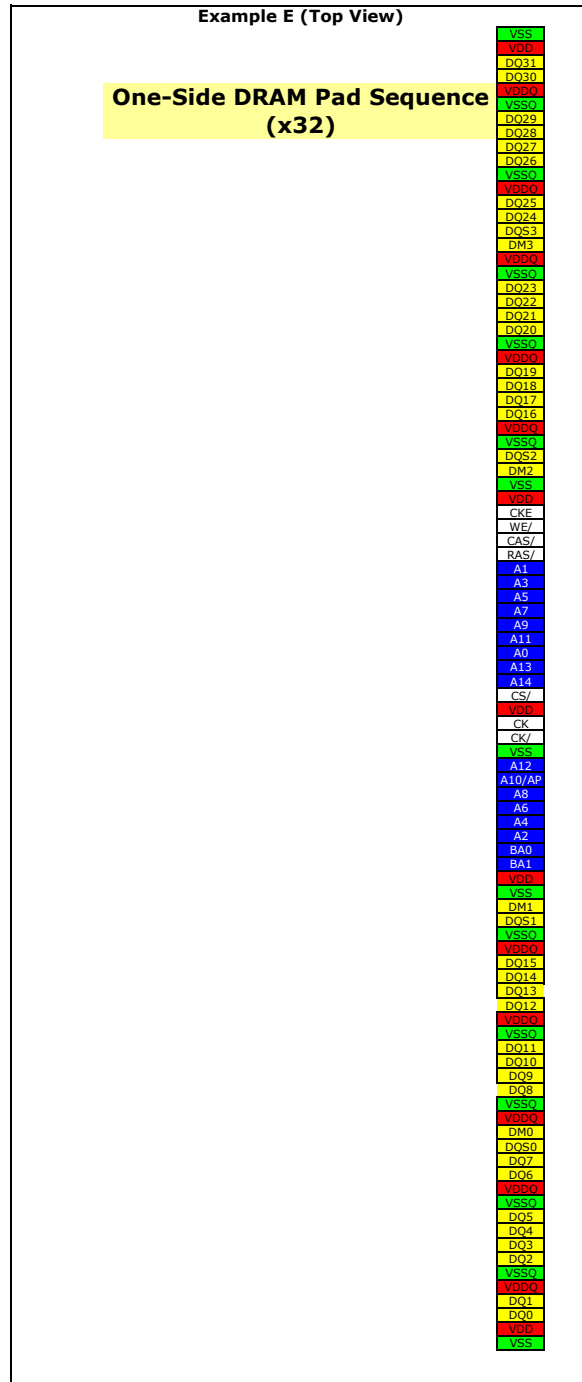


Figure 3.12.3.1-5 - Example E - One-Side DRAM Pad Sequence (x32)

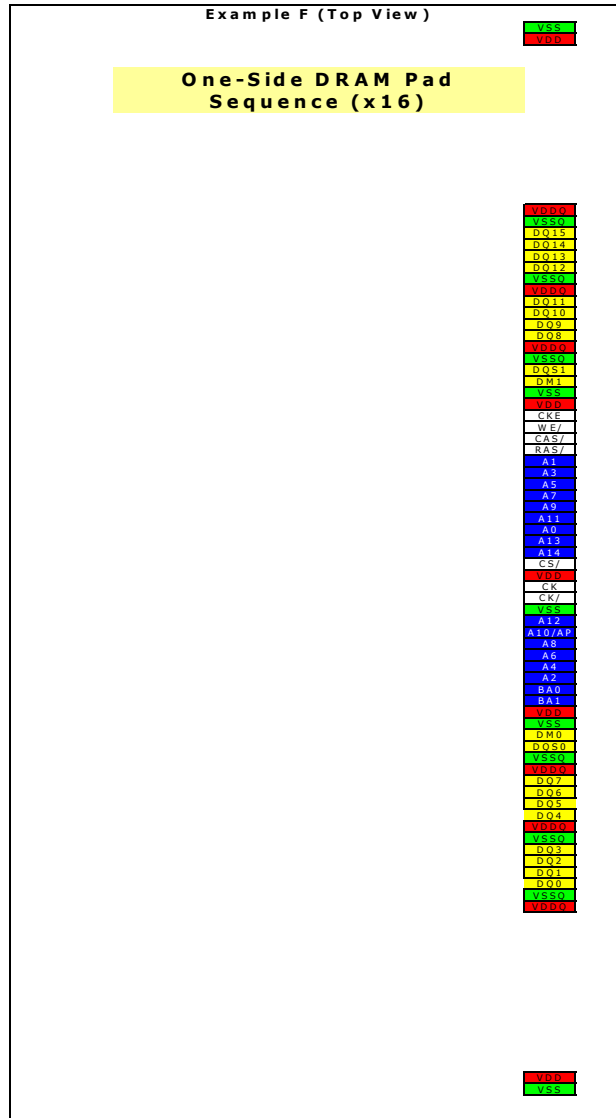


Figure 3.12.3.1-6 - Example F - One-Side DRAM Pad Sequence (x16)



3.12.3.2 x16 PSRAM Silicon Pad Sequence Order

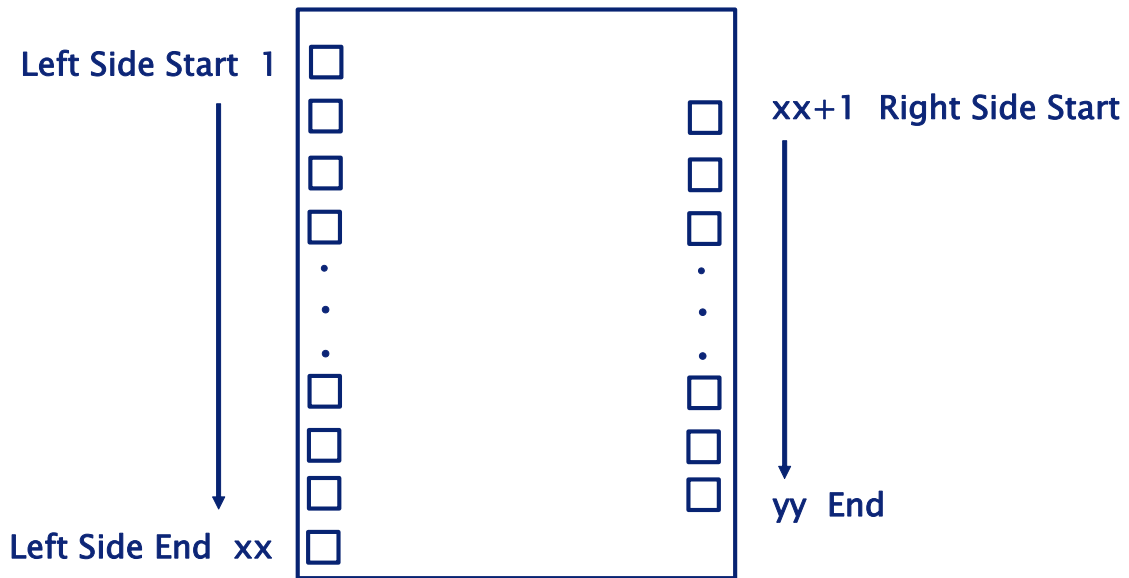


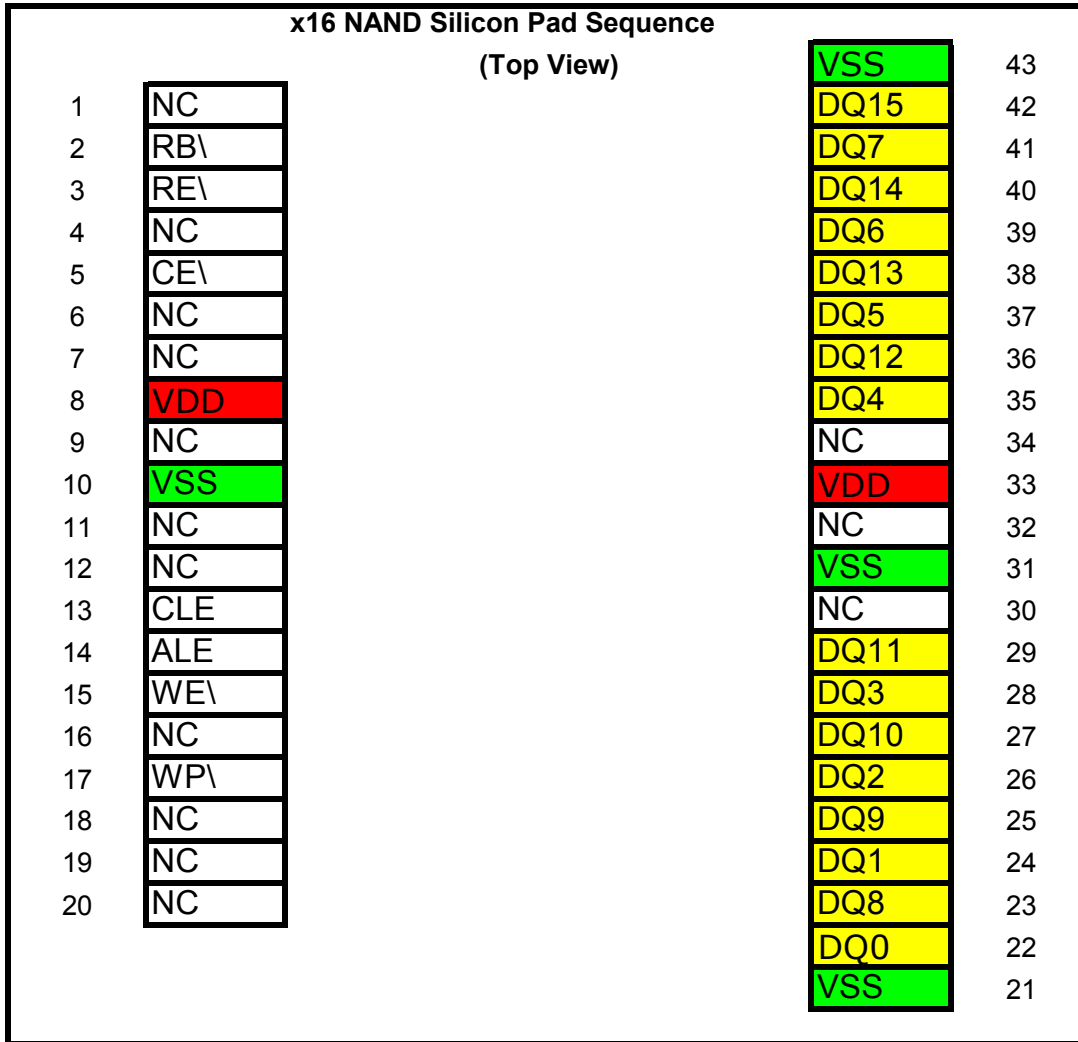
Figure 3.12.3.2-1 - x16 PSRAM Silicon Pad Order Reference (Top View)

<b>Left Side</b>		<b>Right Side</b>	
<u>Option A</u>	<u>Option B</u>	<u>Option A</u>	<u>Option B</u>
1. VDD	A16	41. VDD	WAIT (RDY)
2. VSS	A15	42. VSS	DQ15
3. A18	A14	43. DQ15	DQ7
4. A17	not present or VDD	44. DQ07	VDD
5. A16	not present or VSS	45. VDD	VSS
6. A15	A13	46. VSS	DQ14
7. A14	A12	47. DQ14	DQ6
8. VSS	A11	48. DQ06	DQ13
9. VDD	A10	49. VDD	DQ5
10. A13	not present or VDD	50. VSS	VDD
11. A12	not present or VSS	51. DQ13	VSS
12. A11	A9	52. DQ05	DQ12
13. A10	A8	53. VDD	DQ4
14. A09	A22	54. VSS	VSS
15. A21	A21	55. DQ12	VDD
16. A22	A20	56. DQ04	OE#
17. CE2	VSS	57. VSS	DQ11
18. WE#	VDD	58. VDD	DQ3
19. ADV#	CLK	59. CLK	VSS
20. VSS	WE#	60. WAIT#	VDD
21. VDD	ADV#	61. DQ11	DQ10
22. OE#	CRE/PS#/CS2	62. DQ03	DQ2
23. CE1#	UB#	63. VSS	DQ9
24. VSS	LB#	64. VDD	DQ1
25. VDD	CE#	65. DQ10	VSS
26. UB#	A19	66. DQ02	VDD
27. LB#	A18	67. VSS	DQ8
28. A20	A17	68. VDD	DQ0
29. A19	A7	69. DQ09	
30. A08	A6	70. DQ01	
31. VDD	not present or VSS	71. VSS	
32. VSS	not present or VDD	72. VDD	
33. A07	A5	73. DQ08	
34. A06	A4	74. DQ00	
35. A05	A3	75. A00	
36. A04	A2	76. A01	
37. A03	not present or VSS	77. A02	
38. VSS	not present or VDD	78. VSS	
39. VDD	A1	79. VDD	
40. -	A0		

Note: Die pad reference numbers used on this page are for the convenience of side by side comparison

**Figure 3.12.3.2-2 - X16 PSRAM Silicon Pad Order (Option A and B)**

3.12.33 x16 PSRAM Interfaced Memories Silicon Pad Sequence



NOTE: Pad and NC count may vary

Figure 3.12.3.3-1 - x16 NAND Interfaced Memories Silicon Pad Sequence  
(Top View)