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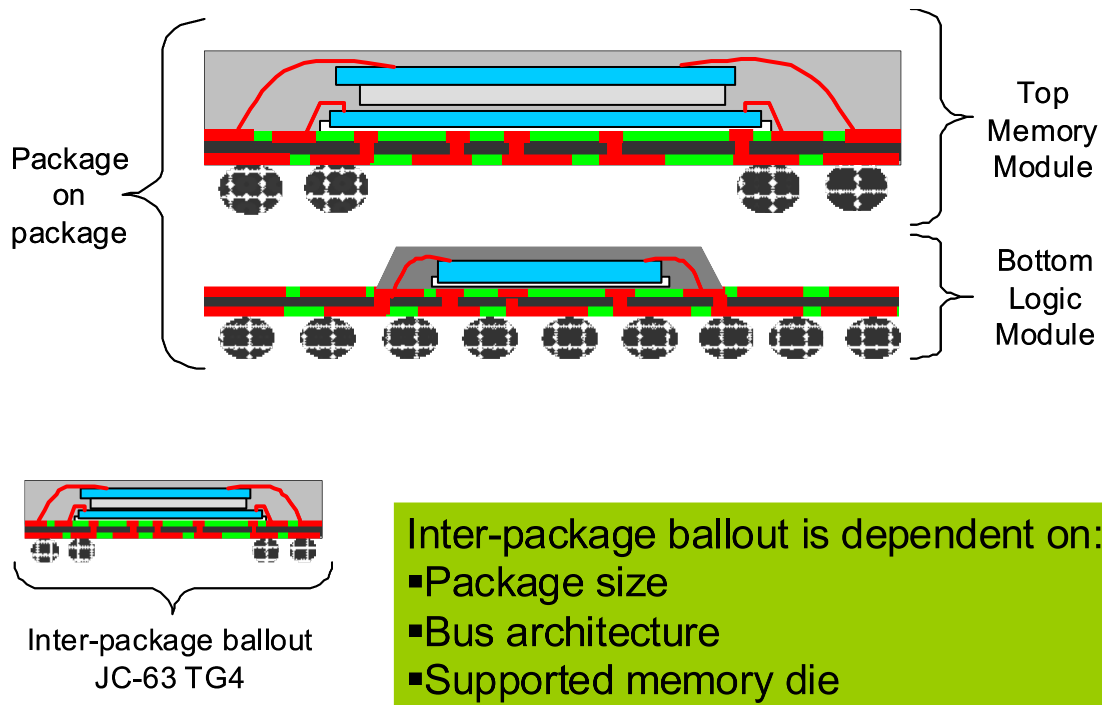


Figure 3.12.2-1 - Inter-Package Ballout

General Rules Used for Pattern Development

- "Consideration given to wire routing and layout to maximize performance
- "Consideration given to power and ground pairs to maximize performance
- "Alignment to silicon pad sequence standardization efforts for various technologies
- "Address & Data bus will be in sequential order where possible
- "Corner balls designated as NC - no connect - and should be used for mechanical stability."
- "Support multiple packages on a single test platform when possible

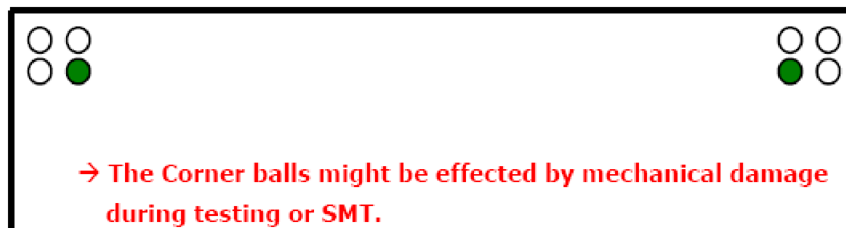
  * Fixed placement of ground balls
  * Strategic placement of ""RFU"" balls on larger package to support fewer
  * balls on smaller package
  * Outer row of larger package becomes inner row of smaller package

LPDDR2 PoP Design Guidelines (GL's)

- **GL1: VDD1/VDD2/VSS should be grouped together for good power delivery and match the silicon allocation and close location (Example: silicon contains these groups on top, center, and bottom of each side of die, package should reflect this distribution)**

- **GL2: 12PoP (0.5, 168ball) CA[4:0] should be reversed (vs silicon) as they wrap around ball package corners to provide better routing on memory top package.**

- **GL3: Assign 4 DU balls on the each corner. 3 would be acceptable w/ 4th ball as power delivery option if required, depending on design.**



- **GL4: Follow JEDEC PAD ordering to execute easy routing**

- **GL5: Number/location of Power/GND ball with matching ratio 1:1 (for every VSS/VSSQ, a matching VDD/VDDQ exists on 1:1 basis) To reduce the Power/GND Noise through balancing**

NOTE: Acceptable practice, actual ratio may vary depending on requirement

- **GL6: Assign VDDQ / VSSQ as diagonal type to shield signal lines by power lines**

- **GL7: Assign CLK /CLK# differential signals side/side within row with paired order to reduce noise effect. DQS# /DQS diagonal placement coupled with VSSQ/VDDQ (on other two balls within 4-ball group) for good noise isolation**

- **GL8: Vref balls should be placed with 2ea/Ch. (DQ-Vref and CA-Vref on each side) Vss should be assigned to Vref ball by pair to minimize power noise Single Vref may be shared per ch. but may limit performance/ spec, such occurrence should be noted and validated by system analysis.**

- **GL9: ZQ ball should be assigned by 1ea/Channel. 1 ZQ pin can access 2 different dies using time interval method (Single ZQ ball shared with two die in stack)**

- **GL10: VDDQ/VSSQ/DQ ratio needs to be 1/1/4. (1/1/4 (25%) is minimum ratio requirement, actual silicon is 14/14/32 (43%)**

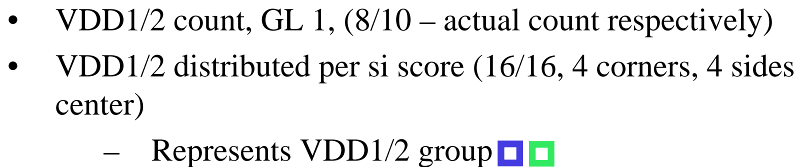
NOTE: Depends on design requirements, more data simulation required to use this practice as a minimum. Higher ratio the better.

- **GL11: minimize CA Length. CA ball group should be assigned at near area from Pad. The CS, CKE Balls might be place next to CA balls. (CS and CKE not as timing critical, so placement locate on side of CA channel vs in center may be acceptable)**

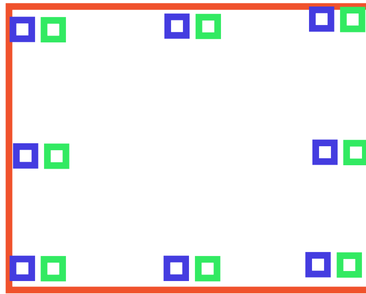
NOTE: Agree to minimize CA ball group trace length. No consensus on CS/CKE placement outside of CA channel

PoP Metric Examples

(used to evaluate new PoP proposals)
Example = 2 channel LPDDR2 PoP x32



- VDD1/2 count, GL 1, (8/10 – actual count respectively)
- VDD1/2 distributed per si score (16/16, 4 corners, 4 sides center)
  - Represents VDD1/2 group



- Vref, GL 6 (2/channel, 4 total for 2 independent x32 channels)

- IO Power delivery ratio, GL 10, (VDDQ/VSSQ pair per byte) 2.75:1
  - This ratio based on total of 11VDDQ/VSSQ pairs per x32 channel broken down per Byte

- Differential signals, GL 7,
  - DQS/DQS# and CLK/CLK# - Next to each other on inner/outer rows vs inner row

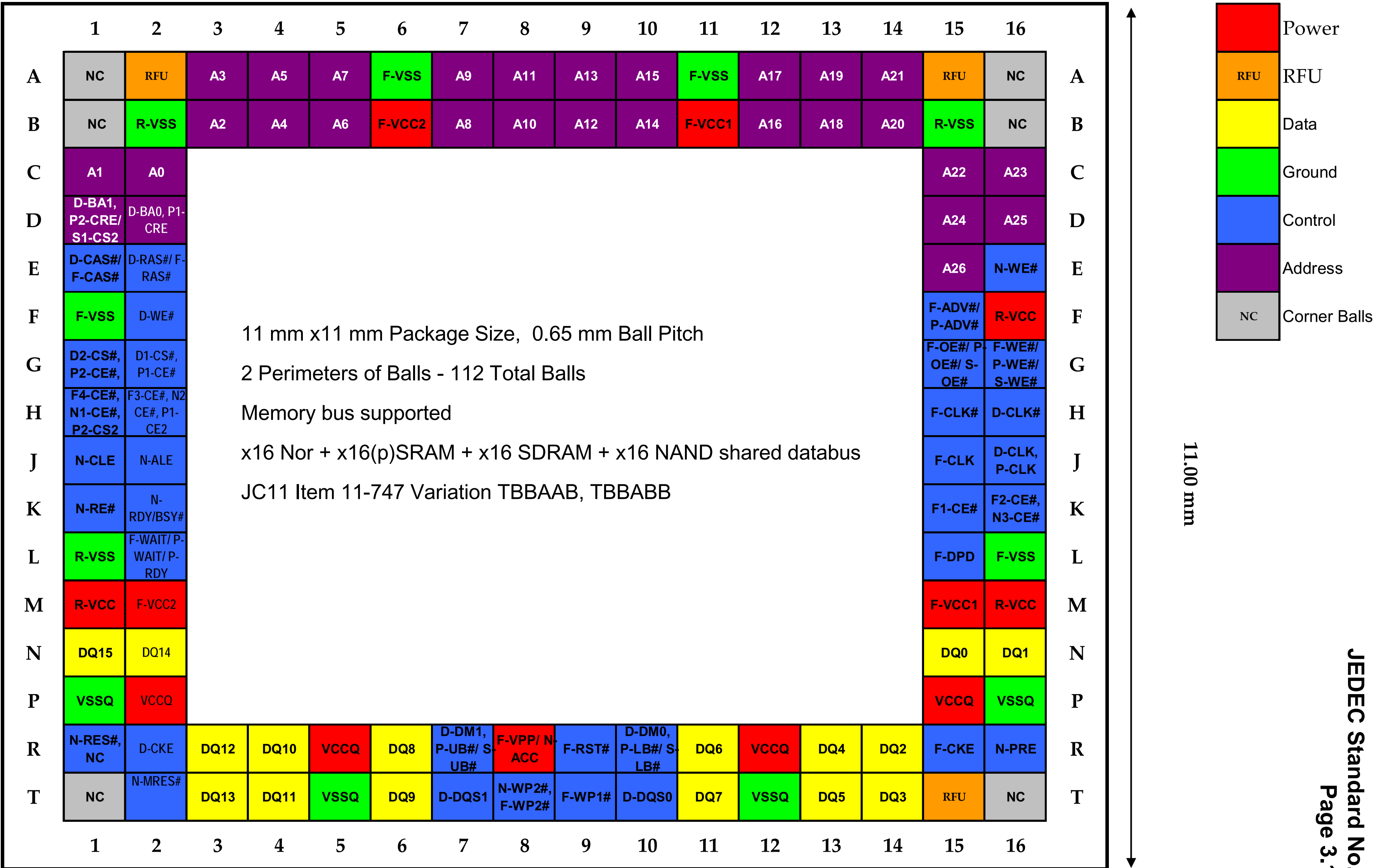


Figure 3.12.2-2
Ball Outline – 112-Ball BGA, 0.65 mm Pitch, 11 mm x 11 mm Package

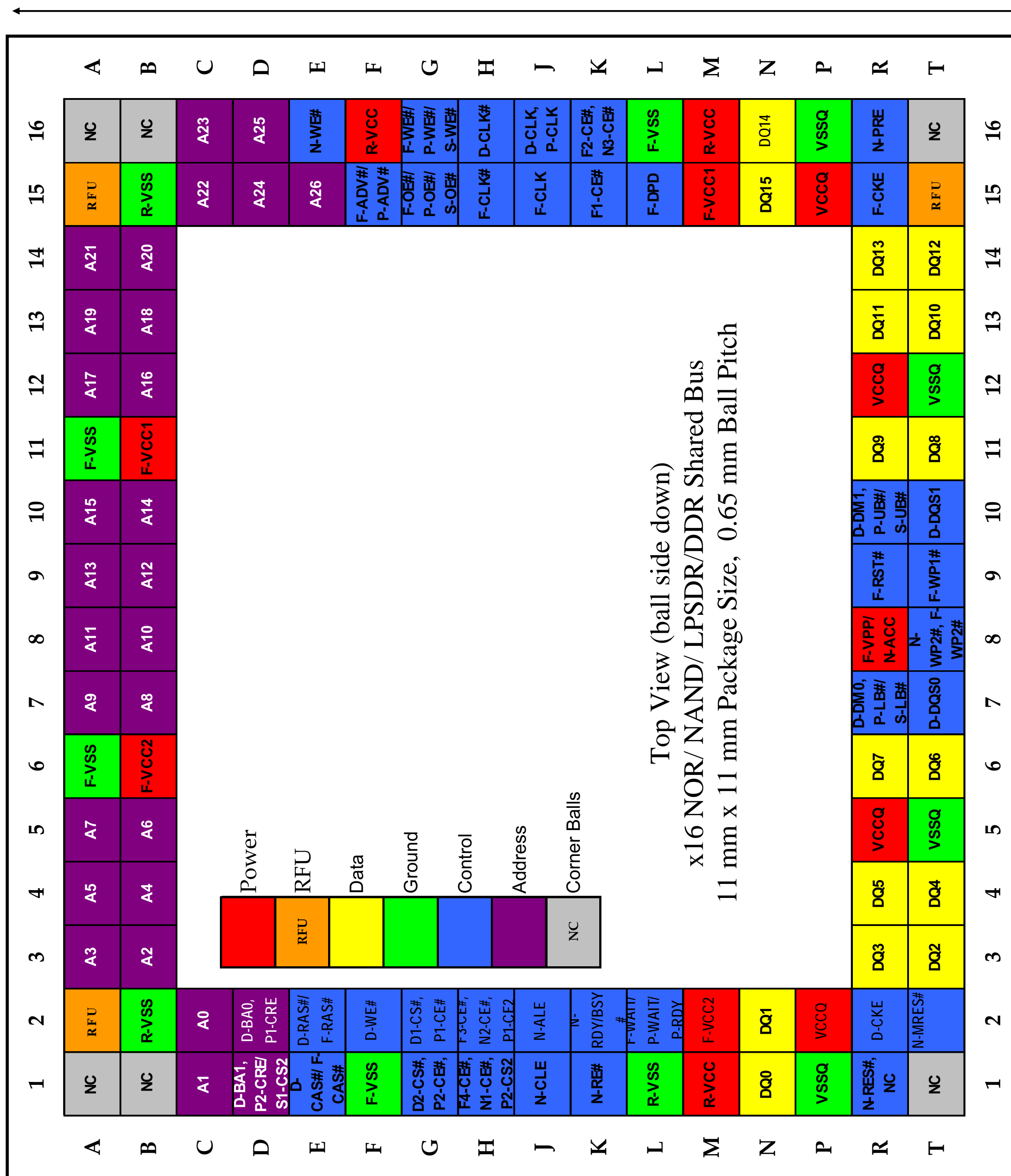


Figure 3.12.2-3
Ball Outline – Flipped DQ Sequence
112-Ball BGA, 0.65 mm Pitch, 11 mm x 11 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	RFU	A3	A3	B3	A2	R3	DQ12	T3	DQ13	A15	RFU	A16	NC
B1	NC	B2	R-VSS	A4	A5	B4	A4	R4	DQ10	T4	DQ11	B15	R-VSS	B16	NC
C1	A1	C2	A0	A5	A7	B5	A6	R5	VCCQ	T5	VSSQ	C15	A22	C16	A23
D1	D-BA1, P2-CRE/ S1-CS2	D2	D-BA0, P1-CRE	A6	F-VSS	B6	F-VCC2	R6	DQ8	T6	DQ9	D15	A24	D16	A25
E1	D-CAS#/ F-CAS#	E2	D-RAS#/ F-RAS#	A7	A9	B7	A8	R7	D-DM1, P-UB#/ S-UB#	T7	D-DQS1	E15	A26	E16	N-WE#
F1	F-VSS	F2	D-WE#	A8	A11	B8	A10	R8	F-VPP/ N-ACC	T8	N-WP2#, F-WP2#	F15	F-ADV#/ P-ADV#	F16	R-VCC
G1	D2-CS#, P2-CE#,	G2	D1-CS#, P1-CE#	A9	A13	B9	A12	R9	F-RST#	T9	F-WP1#	G15	F-OE#/ P-OE#/ S-OE#	G16	F-WE#/ P-WE#/ S-WE#
H1	F4-CE#, N1-CE#, P2-CS2	H2	F3-CE#, N2-CE#, P1-CE2	A10	A15	B10	A14	R10	D-DM0, P-LB#/ S-LB#	T10	D-DQS0	H15	F-CLK#	H16	D-CLK#
J1	N-CLE	J2	N-ALE	A11	F-VSS	B11	F-VCC1	R11	DQ6	T11	DQ7	J15	F-CLK	J16	D-CLK, P-CLK
K1	N-RE#	K2	N-RDY/BSY#	A12	A17	B12	A16	R12	VCCQ	T12	VSSQ	K15	F1-CE#	K16	F2-CE#, N3-CE#
L1	R-VSS	L2	F-WAIT/ P-WAIT/ P-RDY	A13	A19	B13	A18	R13	DQ4	T13	DQ5	L15	F-DPD	L16	F-VSS
M1	R-VCC	M2	F-VCC2	A14	A21	B14	A20	R14	DQ2	T14	DQ3	M15	F-VCC1	M16	R-VCC
N1	DQ15	N2	DQ14									N15	DQ0	N16	DQ1
P1	VSSQ	P2	VCCQ									P15	VCCQ	P16	VSSQ
R1	N-RES#, NC	R2	D-CKE									R15	F-CKE	R16	N-PRE
T1	NC	T2	N-MRES#									T15	RFU	T16	NC

Figure 3.12.2-4
Ball List - 112-Ball BGA, 0.65 mm Pitch, 11 mm X 11 mm Package

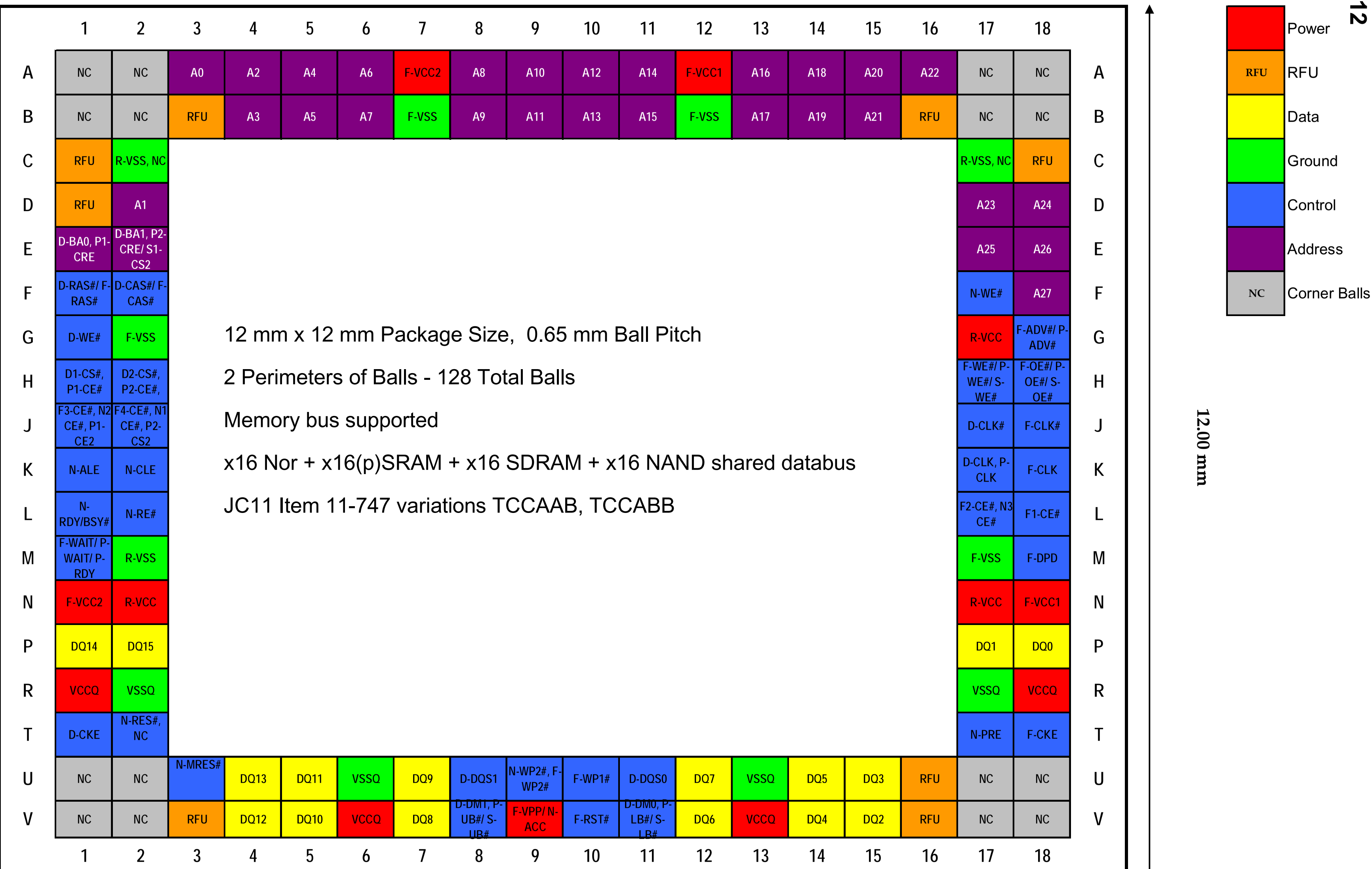


Figure 3.12.2-5
Ball Outline – 128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

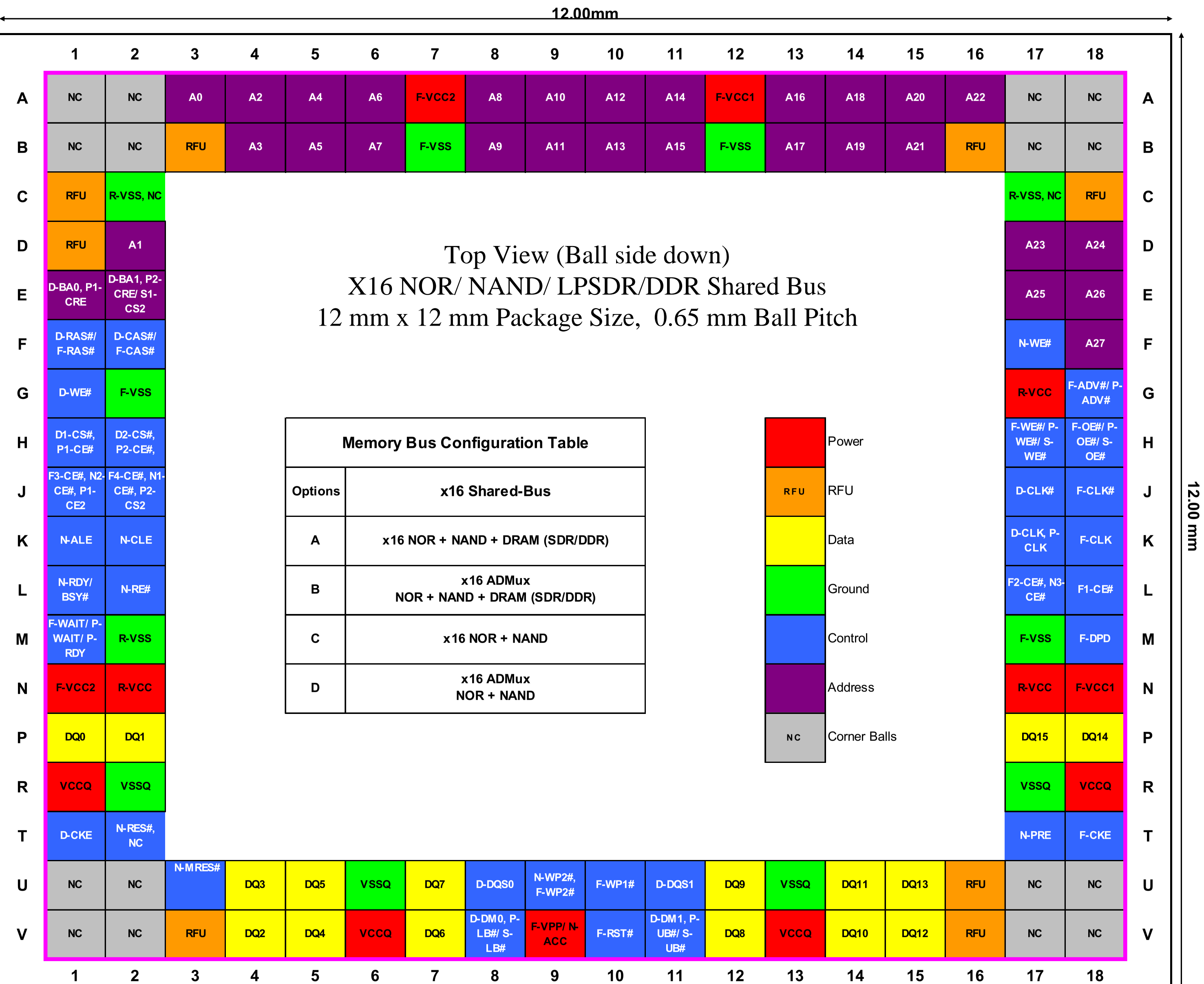
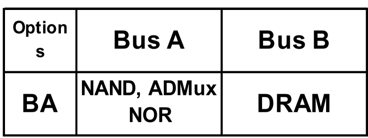


Figure 3.12.2-6
Ball Outline – Flipped DQ Sequence
128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	NC	NC	D-DQ1	D-VSS	F-VDD	N-CLE	A17	A19	A21	A23	A25	DPD	VPP/ACC	N-WE#	F-WE#	N2/F3-CE#	NC	NC
B	NC	D-VDDQ	D-DQ0	D-VDD	F-VSS	N-ALE	A16	A18	A20	A22	A24	A26,RFU	RST#	RE#	OE#	N1/F4-CE#	N-RY/BY#	NC
C	D-VSSQ	D-DQ2															F2/N3-CE#	WP2#
D	D-DQ3	D-DQ4															F1/N4-CE#	WP1#
E	D-DQ5	D-VDDQ															D-A0	D-A1
F	D-VSSQ	D-DQ6															D-A2	D-A3
G	D-DQ7	D-DQS0															D-BA0	D-BA1
H	D-DM0	D-CK															D1-CS#	D2-CS#
J	D-CK#	D-DQS1															D-RAS#	D-CAS#
K	D-DM1	D-DQ8															D-WE#	D1-CKE
L	D-DQ9	D-VDDQ															D-VDD	D2-CKE
M	D-VSSQ	D-DQ10															D-A4	D-VSS
N	D-DQ11	D-DQ12															D-A6	D-A5
P	D-DQ13	D-VDDQ															D-A8	D-A7
R	D-VSSQ	D-DQ14															D-A10	D-A9
T	D-DQ15	D-VDD															D-A12	D-A11
U	NC	D-VSS	F-VDD	ADQ0	ADQ2	VDDQ	ADQ4	ADQ6	F-CLK	F-VDD	ADQ8	ADQ10	VDDQ	ADQ12	ADQ14	D-A14	D-A13	NC
V	NC	NC	F-VSS	ADQ1	ADQ3	VSSQ	ADQ5	ADQ7	F-ADV#	F-VSS	ADQ9	ADQ11	VSSQ	ADQ13	ADQ15	F-WAIT	NC	NC

Legend	Description
B: Data	B: DDR DQ[15:0]
A: Addr	A: NOR Address
A: Data	A: NOR ADQ[15:0] shared with NAND DQ[15:0]
B: Addr	B: DDR Address
GND	Ground
PWR	Power
DDR Cntrl	Control for DDR
F/N Cntrl	Control for NOR/NAND
RFU	Reserved for Future Use
NC	No connect (Outriggers



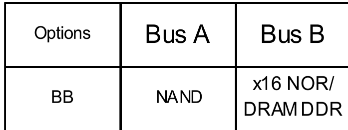
Options	Bus A	Bus B
BA	NAND, ADMux NOR	DRAM

MO-273 Var TCCAAB, TCCABB

Figure 3.12.2-7
Ball Outline - Option BA: (x16 AD Mux NOR/x16 NAND) + (x16 DDR LPSDRAM) split bus
128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	NC	NC	D/F-DQ1	D/F-VSS	N-VCC	CLE	RFU	RFU	RFU	RFU	RFU	RFU	VPP/ACC	N-WE#	F-WE#	N2-CE#	NC	NC
B	NC	D/F-VDDQ	D/F-DQ0	D/F-VDD	N-VSS	ALE	RFU	RFU	RFU	RFU	RFU	RFU	RST#	RE#	RFU	N1-CE#	N-RY/BY#	NC
C	D/F-VSSQ	D/F-DQ2															F2-CE#	N-WP#
D	D/F-DQ3	D/F-DQ4															F1-CE#	F-WP#
E	D/F-DQ5	D/F-VDDQ															D/F-A0	D/F-A1
F	D/F-VSSQ	D/F-DQ6															D/F-A2	D/F-A3
G	D/F-DQ7	D/F-DQS0															D/F-BA0	D/F-BA1
H	D/F-DM0	D/F-CLK															D1-CS#	D2-CS#
J	D/F-CLK#	D/F-DQS1															D/F-RAS#	D/F-CAS#
K	D/F-DM1	D/F-DQ8															D-WE#	D-CKE
L	D/F-DQ9	D/F-VDDQ															D/F-VDD	F-CKE
M	D/F-VSSQ	D/F-DQ10															D/F-A4	D/F-VSS
N	D/F-DQ11	D/F-DQ12															D/F-A6	D/F-A5
P	D/F-DQ13	D/F-VDDQ															D/F-A8	D/F-A7
R	D/F-VSSQ	D/F-DQ14															D/F-A10	D/F-A9
T	D/F-DQ15	D/F-VDD															D/F-A12	D/F-A11
U	NC	D/F-VSS	N-VCC	DQ0	DQ2	VCCQ	DQ4	DQ6	RFU	N-VCC	DQ8	DQ10	VCCQ	DQ12	DQ14	D/F-A14	D/F-A13	NC
V	NC	NC	N-VSS	DQ1	DQ3	VSSQ	DQ5	DQ7	RFU	N-VSS	DQ9	DQ11	VSSQ	DQ13	DQ15	RFU	NC	NC

Legend	Description
B: Data	B: DDR NOR/DRAM DQ[15:0]
A: Data	A: NAND DQ[15:0]
B: Addr	B: DDR Address
GND	Ground
PWR	Power
DDR Cntrl	Control for DDR DRAM/NOR
N Cntrl	Control for NAND
RFU	Reserved for Future Use
NC	No connect (Outriggers)



Options	Bus A	Bus B
BB	NAND	x16 NOR/ DRAM DDR

Proposed

MO-273 Var TCCAAB, TCCABB

Figure 3.12.2-8
Ball Outline - Option BB: (x16 NAND) + (x16 DDR NOR/LPSDRAM) split bus
128-Ball BGA, 0.65 mm Pitch, 12 mm x 12 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	NC	A3	A0	B3	A1, NC	U3	N-MRES#	V3	RFU	A17	NC	A18	NC
B1	NC	B2	NC	A4	A2	B4	A3	U4	DQ13	V4	DQ12	B17	NC	B18	NC
C1	RFU	C2	R-VSS, NC	A5	A4	B5	A5	U5	DQ11	V5	DQ10	C17	R-VSS, NC	C18	RFU
D1	RFU	D2	A1	A6	A6	B6	A7	U6	VSSQ	V6	VCCQ	D17	A23	D18	A24
E1	D-BA0, P1-CRE	E2	D-BA1, P2-CRE/ S1-CS2	A7	F-VCC2	B7	F-VSS	U7	DQ9	V7	DQ8	E17	A25	E18	A26
F1	D-RAS#/ F-RAS#	F2	D-CAS#/ F-CAS#	A8	A8	B8	A9	U8	D-DQS1	V8	D-DM1, P-UB#/ S-UB#	F17	N-WE#	F18	A27
G1	D-WE#	G2	F-VSS	A9	A10	B9	A11	U9	N-WP2#, F-WP2#	V9	F-VPP/ N-ACC	G17	R-VCC	G18	F-ADV#/ P-ADV#
H1	D1-CS#, P1-CE#	H2	D2-CS#, P2-CE#,	A10	A12	B10	A13	U10	F-WP1#	V10	F-RST#	H17	F-WE#/ P-WE#/ S-WE#	H18	F-OE#/ P-OE#/ S-OE#
J1	F3-CE#, N2-CE#, P1-CE2	J2	F4-CE#, N1-CE#, P2-CS2	A11	A14	B11	A15	U11	D-DQS0	V11	D-DM0, P-LB#/ S-LB#	J17	D-CLK#	J18	F-CLK#
K1	N-ALE	K2	N-CLE	A12	F-VCC1	B12	F-VSS	U12	DQ7	V12	DQ6	K17	D-CLK, P-CLK	K18	F-CLK
L1	N-RDY/BSY#	L2	N-RE#	A13	A16	B13	A17	U13	VSSQ	V13	VCCQ	L17	F2-CE#, N3-CE#	L18	F1-CE#
M1	F-WAIT/ P-WAIT/ P-RDY	M2	R-VSS	A14	A18	B14	A19	U14	DQ5	V14	DQ4	M17	F-VSS	M18	F-DPD
N1	F-VCC2	N2	R-VCC	A15	A20	B15	A21	U15	DQ3	V15	DQ2	N17	R-VCC	N18	F-VCC1
P1	DQ14	P2	DQ15	A16	A22	B16	RFU	U16	RFU	V16	RFU	P17	DQ1	P18	DQ0
R1	VCCQ	R2	VSSQ									R17	VSSQ	R18	VCCQ
T1	D-CKE	T2	N-RES#, NC									T17	N-PRE	T18	F-CKE
U1	NC	U2	NC									U17	NC	U18	NC
V1	NC	V2	NC									V17	NC	V18	NC

Figure 3.12.2-9
Ball List – 128-Ball BGA, 0.65 mm Pitch, 12 mm X 12 mm Package

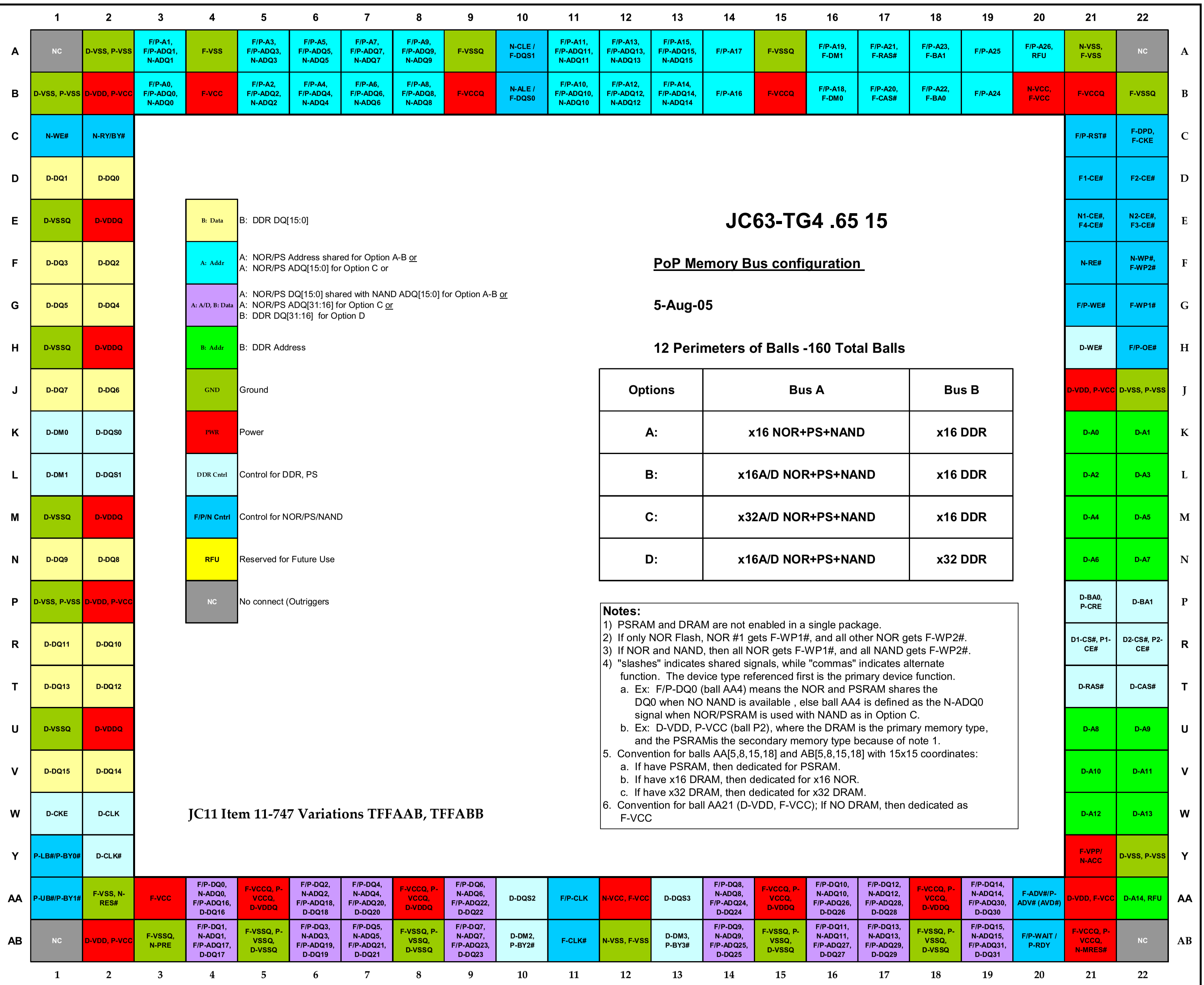


Figure 3.12.2-10
Ball Outline – 160-Ball BGA, 0.65 mm Pitch, 15 mm x 15 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	D-VSS, P-VSS NC	A3	F/P-A1, F/P-ADQ1, N-ADQ1	B3	F/P-A0, F/P-ADQ0, N-ADQ0	AA3	F-VCC	AB3	F-VSSQ, N-PRE	A21	N-VSS, F-VSS, NC	A22	NC
B1	D-VSS, P-VSS NC	B2	D-VDD, P-VCC	A4	F-VSS	B4	F-VCC	AA4	F/P-DQ0, N-ADQ0, F/P-ADQ16, D-DQ16	AB4	F/P-DQ1, N-ADQ1, F/P-ADQ17, D-DQ17	B21	F-VCCQ	B22	F-VSSQ NC
C1	N-WE#	C2	N-RY/BY#	A5	F/P-A3, F/P-ADQ3, N-ADQ3	B5	F/P-A2, F/P-ADQ2, N-ADQ2	AA5	F-VCCQ, P-VCCQ, D-VDDQ	AB5	F-VSSQ, P-VSSQ, D-VSSQ	C21	F/P-RST#	C22	F-DPD, F-CKE
D1	D-DQ1	D2	D-DQ0	A6	F/P-A5, F/P-ADQ5, N-ADQ5	B6	F/P-A4, F/P-ADQ4, N-ADQ4	AA6	F/P-DQ2, N-ADQ2, F/P-ADQ18, D-DQ18	AB6	F/P-DQ3, N-ADQ3, F/P-ADQ19, D-DQ19	D21	F1-CE#	D22	F2-CE#
E1	D-VSSQ	E2	D-VDDQ	A7	F/P-A7, F/P-ADQ7, N-ADQ7	B7	F/P-A6, F/P-ADQ6, N-ADQ6	AA7	F/P-DQ4, N-ADQ4, F/P-ADQ20, D-DQ20	AB7	F/P-DQ5, N-ADQ5, F/P-ADQ21, D-DQ21	E21	N1-CE#, F4-CE#	E22	N2-CE#, F3-CE#
F1	D-DQ3	F2	D-DQ2	A8	F/P-A9, F/P-ADQ9, N-ADQ9	B8	F/P-A8, F/P-ADQ8, N-ADQ8	AA8	F-VCCQ, P-VCCQ, D-VDDQ	AB8	F-VSSQ, P-VSSQ, D-VSSQ	F21	N-RE#	F22	N-WP#, F-WP2#
G1	D-DQ5	G2	D-DQ4	A9	F-VSSQ	B9	F-VCCQ	AA9	F/P-DQ6, N-ADQ6, F/P-ADQ22, D-DQ22	AB9	F/P-DQ7, N-ADQ7, F/P-ADQ23, D-DQ23	G21	F/P-WE#	G22	F-WP1#
H1	D-VSSQ	H2	D-VDDQ	A10	N-CLE / F-DQS1	B10	N-ALE / F-DQS0	AA10	D-DQS2	AB10	D-DM2, P-BY2#	H21	D-WE#	H22	F/P-OE#
J1	D-DQ7	J2	D-DQ6	A11	F/P-A11, F/P-ADQ11, N-ADQ11	B11	F/P-A10, F/P-ADQ10, N-ADQ10	AA11	F/P-CLK	AB11	F-CLK#	J21	D-VDD, P-VCC	J22	D-VSS, P-VSS
K1	D-DM0	K2	D-DQS0	A12	F/P-A13, F/P-ADQ13, N-ADQ13	B12	F/P-A12, F/P-ADQ12, N-ADQ12	AA12	N-VCC, F-VCC	AB12	N-VSS, F-VSS	K21	D-A0	K22	D-A1
L1	D-DM1	L2	D-DQS1	A13	F/P-A15, F/P-ADQ15, N-ADQ15	B13	F/P-A14, F/P-ADQ14, N-ADQ14	AA13	D-DQS3	AB13	D-DM3, P-BY3#	L21	D-A2	L22	D-A3
M1	D-VSSQ	M2	D-VDDQ	A14	F/P-A17	B14	F/P-A16	AA14	F/P-DQ8, N-ADQ8, F/P-ADQ24, D-DQ24	AB14	F/P-DQ9, N-ADQ9, F/P-ADQ25, D-DQ25	M21	D-A4	M22	D-A5
N1	D-DQ9	N2	D-DQ8	A15	F-VSSQ	B15	F-VCCQ	AA15	F-VCCQ, P-VCCQ, D-VDDQ	AB15	F-VSSQ, P-VSSQ, D-VSSQ	N21	D-A6	N22	D-A7
P1	D-VSS, P-VSS	P2	D-VDD, P-VCC	A16	F/P-A19, F-DM1	B16	F/P-A18, F-DM0	AA16	F/P-DQ10, N-ADQ10, F/P-ADQ26, D-DQ26	AB16	F/P-DQ11, N-ADQ11, F/P-ADQ27, D-DQ27	P21	D-BA0, P-CRE	P22	D-BA1
R1	D-DQ11	R2	D-DQ10	A17	F/P-A21, F-RAS#	B17	F/P-A20, F-CAS#	AA17	F/P-DQ12, N-ADQ12, F/P-ADQ28, D-DQ28	AB17	F/P-DQ13, N-ADQ13, F/P-ADQ29, D-DQ29	R21	D1-CS#, P1-CE#	R22	D2-CS#, P2-CE#
T1	D-DQ13	T2	D-DQ12	A18	F/P-A23, F-BA1	B18	F/P-A22, F-BA0	AA18	F-VCCQ, P-VCCQ, D-VDDQ	AB18	F-VSSQ, P-VSSQ, D-VSSQ	T21	D-RAS#	T22	D-CAS#
U1	D-VSSQ	U2	D-VDDQ	A19	F/P-A25	B19	F/P-A24	AA19	F/P-DQ14, N-ADQ14, F/P-ADQ30, D-DQ30	AB19	F/P-DQ15, N-ADQ15, F/P-ADQ31, D-DQ31	U21	D-A8	U22	D-A9
V1	D-DQ15	V2	D-DQ14	A20	F/P-A26, RFU	B20	N-VCC, F-VCC	AA20	F-ADV#/P-ADV# (AVD#)	AB20	F/P-WAIT / P-RDY	V21	D-A10	V22	D-A11
W1	D-CKE	W2	D-CLK									W21	D-A12	W22	D-A13
Y1	P-LB#/P-BY0#	Y2	D-CLK#									Y21	F-VPP/ N-ACC	Y22	D-VSS, P-VSS
AA1	P-UB#/P-BY1# NC	AA2	F-VSS, N-RES#									AA21	D-VDD, F-VCC	AA22	D-A14, RFU NC
AB1	NC	AB2	D-VDD, P-VCC NC									AB21	F-VCCQ, P-VCCQ, N-MRES#, NC	AB22	NC

Figure 3.12.2-11
Ball List – 160-Ball BGA, 0.65 mm Pitch, 15 mm X 15 mm Package

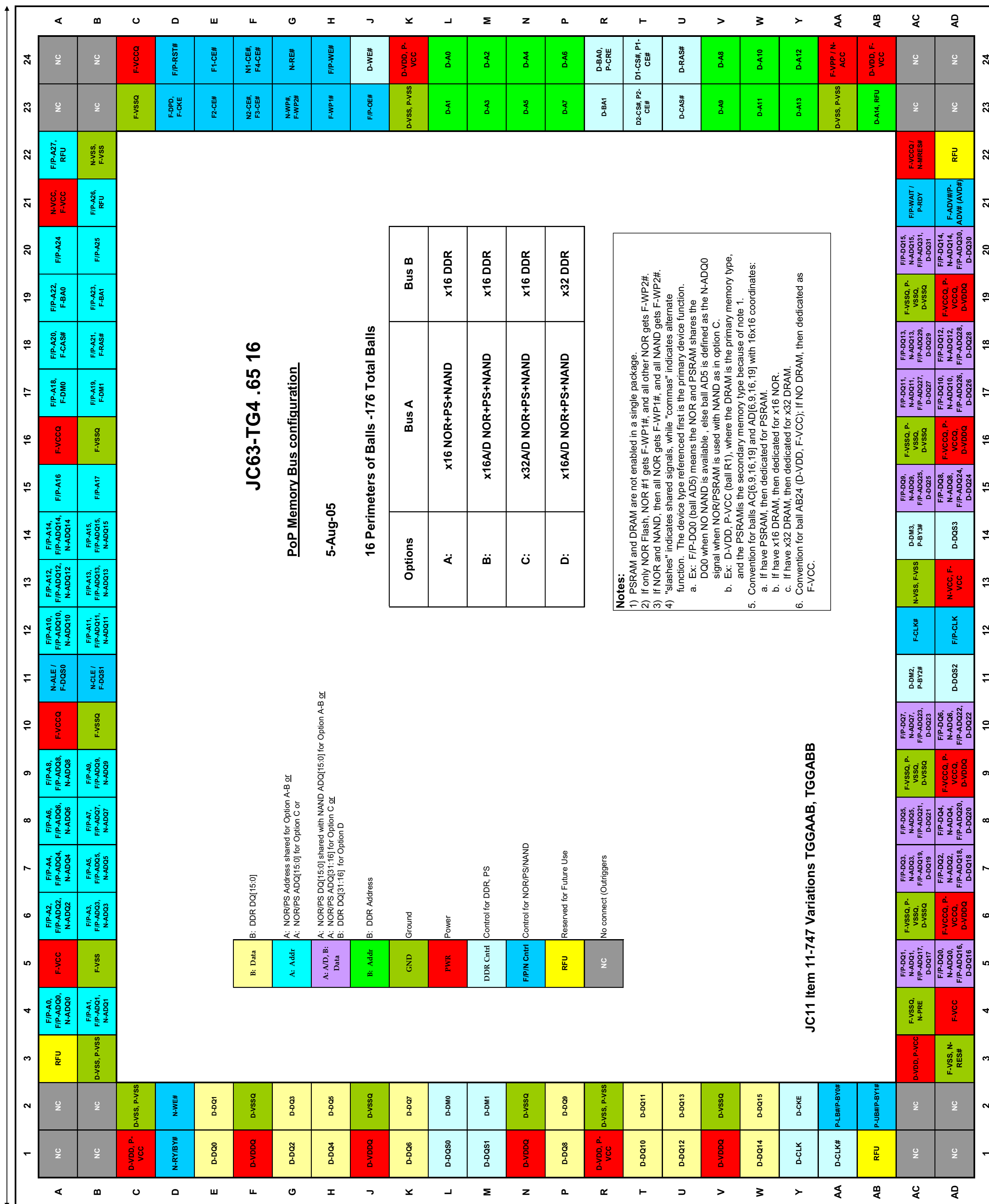


Figure 3.12.2-12
Ball Outline – 176-Ball BGA, 0.65 mm Pitch, 16 mm x 16 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	NC	A3	RFU	B3	D-VSS, P-VSS	AC3	D-VDD, P-VCC	AD3	F-VSS, N-RES#	A23	NC	A24	NC
B1	NC	B2	NC	A4	F/P-A0, F/P-ADQ0, N-ADQ0	B4	F/P-A1, F/P-ADQ1, N-ADQ1	AC4	F-VSSQ, N-PRE	AD4	F-VCC	B23	NC	B24	NC
C1	D-VDD, P-VCC	C2	D-VSS, P-VSS	A5	F-VCC	B5	F-VSS	AC5	F/P-DQ1, N-ADQ1, F/P-ADQ17, D-DQ17	AD5	F/P-DQ0, N-ADQ0, F/P-ADQ16, D-DQ16	C23	F-VSSQ	C24	F-VCCQ
D1	N-RY/BY#	D2	N-WE#	A6	F/P-A2, F/P-ADQ2, N-ADQ2	B6	F/P-A3, F/P-ADQ3, N-ADQ3	AC6	F-VSSQ, P-VSSQ, D-VSSQ	AD6	F-VCCQ, P-VCCQ, D-VDDQ	D23	F-DPD, F-CKE	D24	F/P-RST#
E1	D-DQ0	E2	D-DQ1	A7	F/P-A4, F/P-ADQ4, N-ADQ4	B7	F/P-A5, F/P-ADQ5, N-ADQ5	AC7	F/P-DQ3, N-ADQ3, F/P-ADQ19, D-DQ19	AD7	F/P-DQ2, N-ADQ2, F/P-ADQ18, D-DQ18	E23	F2-CE#	E24	F1-CE#
F1	D-VDDQ	F2	D-VSSQ	A8	F/P-A6, F/P-ADQ6, N-ADQ6	B8	F/P-A7, F/P-ADQ7, N-ADQ7	AC8	F/P-DQ5, N-ADQ5, F/P-ADQ21, D-DQ21	AD8	F/P-DQ4, N-ADQ4, F/P-ADQ20, D-DQ20	F23	N2-CE#, F3-CE#	F24	N1-CE#, F4-CE#
G1	D-DQ2	G2	D-DQ3	A9	F/P-A8, F/P-ADQ8, N-ADQ8	B9	F/P-A9, F/P-ADQ9, N-ADQ9	AC9	F-VSSQ, P-VSSQ, D-VSSQ	AD9	F-VCCQ, P-VCCQ, D-VDDQ	G23	N-WP#, F-WP2#	G24	N-RE#
H1	D-DQ4	H2	D-DQ5	A10	F-VCCQ	B10	F-VSSQ	AC10	F/P-DQ7, N-ADQ7, F/P-ADQ23, D-DQ23	AD10	F/P-DQ6, N-ADQ6, F/P-ADQ22, D-DQ22	H23	F-WP1#	H24	F/P-WE#
J1	D-VDDQ	J2	D-VSSQ	A11	N-ALE / F-DQS0	B11	N-CLE / F-DQS1	AC11	D-DM2, P-BY2#	AD11	D-DQS2	J23	F/P-OE#	J24	D-WE#
K1	D-DQ6	K2	D-DQ7	A12	F/P-A10, F/P-ADQ10, N-ADQ10	B12	F/P-A11, F/P-ADQ11, N-ADQ11	AC12	F-CLK#	AD12	F/P-CLK	K23	D-VSS, P-VSS	K24	D-VDD, P-VCC
L1	D-DQS0	L2	D-DM0	A13	F/P-A12, F/P-ADQ12, N-ADQ12	B13	F/P-A13, F/P-ADQ13, N-ADQ13	AC13	N-VSS, F-VSS	AD13	N-VCC, F-VCC	L23	D-A1	L24	D-A0
M1	D-DQS1	M2	D-DM1	A14	F/P-A14, F/P-ADQ14, N-ADQ14	B14	F/P-A15, F/P-ADQ15, N-ADQ15	AC14	D-DM3, P-BY3#	AD14	D-DQS3	M23	D-A3	M24	D-A2
N1	D-VDDQ	N2	D-VSSQ	A15	F/P-A16	B15	F/P-A17	AC15	F/P-DQ9, N-ADQ9, F/P-ADQ25, D-DQ25	AD15	F/P-DQ8, N-ADQ8, F/P-ADQ24, D-DQ24	N23	D-A5	N24	D-A4
P1	D-DQ8	P2	D-DQ9	A16	F-VCCQ	B16	F-VSSQ	AC16	F-VSSQ, P-VSSQ, D-VSSQ	AD16	F-VCCQ, P-VCCQ, D-VDDQ	P23	D-A7	P24	D-A6
R1	D-VDD, P-VCC	R2	D-VSS, P-VSS	A17	F/P-A18, F-DM0	B17	F/P-A19, F-DM1	AC17	F/P-DQ11, N-ADQ11, F/P-ADQ27, D-DQ27	AD17	F/P-DQ10, N-ADQ10, F/P-ADQ26, D-DQ26	R23	D-BA1	R24	D-BA0, P-CRE
T1	D-DQ10	T2	D-DQ11	A18	F/P-A20, F-CAS#	B18	F/P-A21, F-RAS#	AC18	F/P-DQ13, N-ADQ13, F/P-ADQ29, D-DQ29	AD18	F/P-DQ12, N-ADQ12, F/P-ADQ28, D-DQ28	T23	D2-CS#, P2-CE#	T24	D1-CS#, P1-CE#
U1	D-DQ12	U2	D-DQ13	A19	F/P-A22, F-BA0	B19	F/P-A23, F-BA1	AC19	F-VSSQ, P-VSSQ, D-VSSQ	AD19	F-VCCQ, P-VCCQ, D-VDDQ	U23	D-CAS#	U24	D-RAS#
V1	D-VDDQ	V2	D-VSSQ	A20	F/P-A24	B20	F/P-A25	AC20	F/P-DQ15, N-ADQ15, F/P-ADQ31, D-DQ31	AD20	F/P-DQ14, N-ADQ14, F/P-ADQ30, D-DQ30	V23	D-A9	V24	D-A8
W1	D-DQ14	W2	D-DQ15	A21	N-VCC, F-VCC	B21	F/P-A26, RFU	AC21	F/P-WAIT / P-RDY	AD21	F-ADV#/P-ADV# (AVD#)	W23	D-A11	W24	D-A10
Y1	D-CLK	Y2	D-CKE	A22	F/P-A27, RFU	B22	N-VSS, F-VSS	AC22	F-VCCQ / N-MRES#	AD22	RFU	Y23	D-A13	Y24	D-A12
AA1	D-CLK#	AA2	P-LB#/P-BY0#									AA23	D-VSS, P-VSS	AA24	F-VPP / N-ACC
AB1	RFU	AB2	P-UB#/P-BY1#									AB23	D-A14, RFU	AB24	D-VDD, F-VCC
AC1	NC	AC2	NC									AC23	NC	AC24	NC
AD1	NC	AD2	NC									AD23	NC	AD24	NC

Figure 3.12.2-13
Ball List – 176-Ball BGA, 0.65 mm Pitch, 16 mm x 16 mm Package

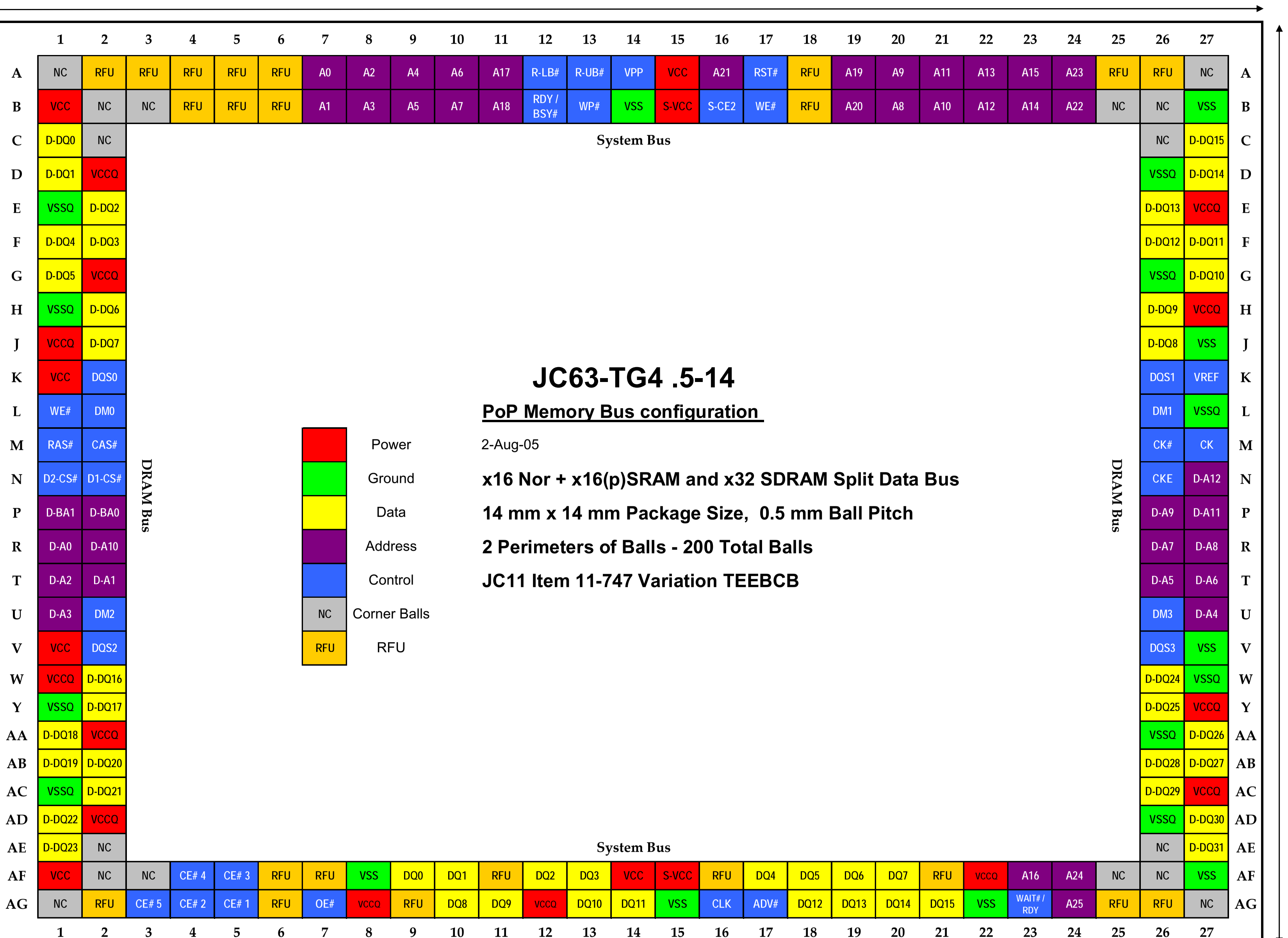


Figure 3.12.2-14
Ball Outline – 200-Ball BGA, 0.5 mm Pitch, 14 mm x 14 mm Package

Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names	Ball Location	Signal Names
A1	NC	A2	RFU	A3	RFU	B3	NC	AF3	NC	AG3	CE# 5	A26	RFU	A27	NC
B1	VCC	B2	NC	A4	RFU	B4	RFU	AF4	CE# 4	AG4	CE# 2	B26	NC	B27	VSS
C1	D-DQ0	C2	NC	A5	RFU	B5	RFU	AF5	CE# 3	AG5	CE# 1	C26	NC	C27	D-DQ15
D1	D-DQ1	D2	VCCQ	A6	RFU	B6	RFU	AF6	RFU	AG6	RFU	D26	VSSQ	D27	D-DQ14
E1	VSSQ	E2	D-DQ2	A7	A0	B7	A1	AF7	RFU	AG7	OE#	E26	D-DQ13	E27	VCCQ
F1	D-DQ4	F2	D-DQ3	A8	A2	B8	A3	AF8	VSS	AG8	VCCQ	F26	D-DQ12	F27	D-DQ11
G1	D-DQ5	G2	VCCQ	A9	A4	B9	A5	AF9	DQ0	AG9	RFU	G26	VSSQ	G27	D-DQ10
H1	VSSQ	H2	D-DQ6	A10	A6	B10	A7	AF10	DQ1	AG10	DQ8	H26	D-DQ9	H27	VCCQ
J1	VCCQ	J2	D-DQ7	A11	A17	B11	A18	AF11	RFU	AG11	DQ9	J26	D-DQ8	J27	VSS
K1	VCC	K2	DQS0	A12	R-LB#	B12	RDY / BSY#	AF12	DQ2	AG12	VCCQ	K26	DQS1	K27	VREF
L1	WE#	L2	DM0	A13	R-UB#	B13	WP#	AF13	DQ3	AG13	DQ10	L26	DM1	L27	VSSQ
M1	RAS#	M2	CAS#	A14	VPP	B14	VSS	AF14	VCC	AG14	DQ11	M26	CK#	M27	CK
N1	D2-CS#	N2	D1-CS#	A15	VCC	B15	S-VCC	AF15	S-VCC	AG15	VSS	N26	CKE	N27	D-A12
P1	D-BA1	P2	D-BA0	A16	A21	B16	S-CE2	AF16	RFU	AG16	CLK	P26	D-A9	P27	D-A11
R1	D-A0	R2	D-A10	A17	RST#	B17	WE#	AF17	DQ4	AG17	ADV#	R26	D-A7	R27	D-A8
T1	D-A2	T2	D-A1	A18	RFU	B18	RFU	AF18	DQ5	AG18	DQ12	T26	D-A5	T27	D-A6
U1	D-A3	U2	DM2	A19	A19	B19	A20	AF19	DQ6	AG19	DQ13	U26	DM3	U27	D-A4
V1	VCC	V2	DQS2	A20	A9	B20	A8	AF20	DQ7	AG20	DQ14	V26	DQS3	V27	VSS
W1	VCCQ	W2	D-DQ16	A21	A11	B21	A10	AF21	RFU	AG21	DQ15	W26	D-DQ24	W27	VSSQ
Y1	VSSQ	Y2	D-DQ17	A22	A13	B22	A12	AF22	VCCQ	AG22	VSS	Y26	D-DQ25	Y27	VCCQ
AA1	D-DQ18	AA2	VCCQ	A23	A15	B23	A14	AF23	A16	AG23	WAIT# / RDY	AA26	VSSQ	AA27	D-DQ26
AB1	D-DQ19	AB2	D-DQ20	A24	A23	B24	A22	AF24	A24	AG24	A25	AB26	D-DQ28	AB27	D-DQ27
AC1	VSSQ	AC2	D-DQ21	A25	RFU	B25	NC	AF25	NC	AG25	RFU	AC26	D-DQ29	AC27	VCCQ
AD1	D-DQ22	AD2	VCCQ									AD26	VSSQ	AD27	D-DQ30
AE1	D-DQ23	AE2	NC									AE26	NC	AE27	D-DQ31
AF1	VCC	AF2	NC									AF26	NC	AF27	VSS
AF1	NC	AF2	RFU									AG26	RFU	AG27	NC

Figure 3.12.2-15
Ball List – 200-Ball BGA, 0.5 mm Pitch, 14 mm x 14 mm Package

Table 3.12.2-1 - PoP Signal Name Glossary

Signal Name	Signal Type	Description
#	Rule	Pound Sign - When appended to a pin name - Indicates TRUE = L signal - Alternate to " \ "
,	Rule	Comma - Seperator used between signal names indicating an alternate function. The device referenced first is the primary device function.
/	Rule	Forward Slash - Separator used between signal names indicating shared signals
\	Rule	Back Slash - When appended to a pin name - Indicates TRUE = L signal
D-	Rule	Prefix for DRAM specific signal
DNU	Rule	Do Not Use
F-	Rule	Prefix for FLASH specific signal
N-	Rule	Prefix for NAND specific signal
NC	Rule	No Connection
P-	Rule	Prefix for pSRAM specific Signal
RFU	Rule	Reserved for Future Use
S-	Rule	Prefix for SRAM specific Signal
A/DQ0 ~ A/DQ15	I/O	ADDRESS input for x16 bus width/DATA INPUT/OUTPUT 0- Inputs data and commands during write cycles, outputs data during read cycles
A/DQ16 ~ A/DQ31	I/O	ADDRESS input for x32 bus width/DATA INPUT/OUTPUT - Inputs data and commands during write cycles, outputs data during read cycles
A0 ~ Amax	I	Address input during read and write operations for x16 bus width
ADV#	I	ADDRESS DATA VALID: Low-true input during synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first.
ALE	I	Address Latch Enable - Address is latched to the address register through NAND I/O ports on the rising edge of WE# when ALE is High
BA0	I	BANK ADDRESS INPUT 0: Select the bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
BA1	I	BANK ADDRESS INPUT 1: Select the bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
CAS#	I	COLUMN ADDRESS STROBE: Low-true input selects the columns of the address location selected
CE0#	I	CHIP ENABLE 0: Low-true input selects the associated memory die
CE1#	I	CHIP ENABLE 1: Low-true input selects the associated memory die
CE2	I	CHIP ENABLE 2: High-true input selects the associated memory die
CE2#	I	CHIP ENABLE 2: Low-true input selects the associated memory die
CE3#	I	CHIP ENABLE 3: Low-true input selects the associated memory die
CKE	I	CLOCK ENABLE: CKE activates (HIGH) and deactivates (LOW) the CLK signal
CLE	I	Command Latch Enable - Commands are latched to the command register through NAND I/O ports on the rising edge of WE# when CLE is High
CLK	I	CLOCK: Synchronizes the memory chip with the system memory bus clock during burst operations.
CLK#	I	DDR CLOCK: Complement of CLK for DDR-enabled memory
CRE	I	CONTROL REGISTER ENABLE: High-true input when active write operations load the Refresh Control Register or Bus Control Register
DM0	I/O	INPUT/OUTPUT MASK 0: DM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses (DQ7-0)
DM1	I/O	INPUT/OUTPUT MASK 0: DM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses (DQ15-8)
DPD	I	Deep Power Down. Control pin used with some flash memory
DQ0 ~ DQ31	I/O	DATA INPUT/OUTPUT - Inputs data and commands during write cycles, outputs data during read cycles
D-VCC	Power	SDRAM CORE VOLTAGE: SDRAM single power supply
D-VCCQ (VDDQ)	Power	SDRAM INPUT/OUTPUT VOLTAGE: Supply power for the input and output buffers
D-VSS	Power	SDRAM CORE GROUND: Connect to system ground - do not float
D-VSSQ	Power	SDRAM INPUT/OUTPUT GROUND: Connect to system ground – do not float
LB#	I	LOWER BYTE ENABLE: Low-true input enables the lower bytes for RAM (DQ7-0)
N-I/O0 ~ N-I/O7	I/O	Command, Address, Data input/output for NAND Flash
N-I/O8 ~ N-I/O15	I/O	Data input/output for NAND Flash
N-PRE	I	Power on auto read enable. Connect to VSS or NC
N-MRES#	O	Output reset signal to CPU when power on auto read mode and auto read mode are activated in certain AND memory.
N-RES#	I	RES# should be low when power is on. Device is initialized upon L to H transition. RES# = L puts the device in deep standby. Used with certain AND memory
OE#	I	OUTPUT ENABLE: Low-true input enables the output buffers when low. When OE# is high, the output buffers are disabled.
RAS#	I	ROW ADDRESS STROBE: Low-true input selects the rows of the address location selected
RDY/BSY#	O	Ready / Busy indicates status of device operation. When Low a program, erase, or read is in progress. It is usually and open-drain signal.
RE#	I	Read Enable. Active low. Controls read timing. Clocking RE# increments the internal address and reads out data
RST#	I	HARDWARE RESET: Low-true input initializes internal circuitry to reading array data
UB#	I	UPPER BYTE ENABLE: Low-true input enables the upper bytes for RAM (DQ15-8)
V-Ref	O	SSTL-2 reference voltage. Voltage reference for data output.
VCC	Power	CORE VOLTAGE: single power supply
VCCQ (VDDQ)	Power	INPUT/OUTPUT VOLTAGE: Supply power for the input and output buffers
VPP (ACC)	I	ACCELERATED VOLTAGE LEVEL: At VHH, accelerates programming and automatically places device in unlock bypass mode. At VIL, disables all program and erase functions, VIH for all other operations.
VSS	Power	CORE GROUND: Connect to system ground - do not float
VSSQ	Power	INPUT/OUTPUT GROUND: Connect to system ground – do not float
WAIT (RDY)/DQS0	O	DEVICE READY: Indicates the status of the burst read operation/DATA STROBE PIN 0: Edge detector for when data is available on the bus (DQ7-0)
WAIT/DQS0	O	WAIT: Indicates the status of the burst read operation/DATA STROBE PIN 0: Edge detector for when data is available on the bus (DQ7-0)
WE#	I	WRITE ENABLE: Low-true input controls the write operations to the selected die by determining whether a given cycle is a write cycle.
WP1#	I	HARDWARE WRITE PROTECT: Low-true input controls the associated flash memory die(s). If only NOR Flash, NOR #1 gets F-WP1#, and all other NOR gets F-WP2#. If NOR and NAND, then all NOR gets F-WP1#, and all NAND gets F-WP2#.
WP2#	I	HARDWARE WRITE PROTECT: Low-true input controls the associated flash memory die(s). If only NOR Flash, NOR #1 gets F-WP1#, and all other NOR gets F-WP2#. If NOR and NAND, then all NOR gets F-WP1#, and all NAND gets F-WP2#.

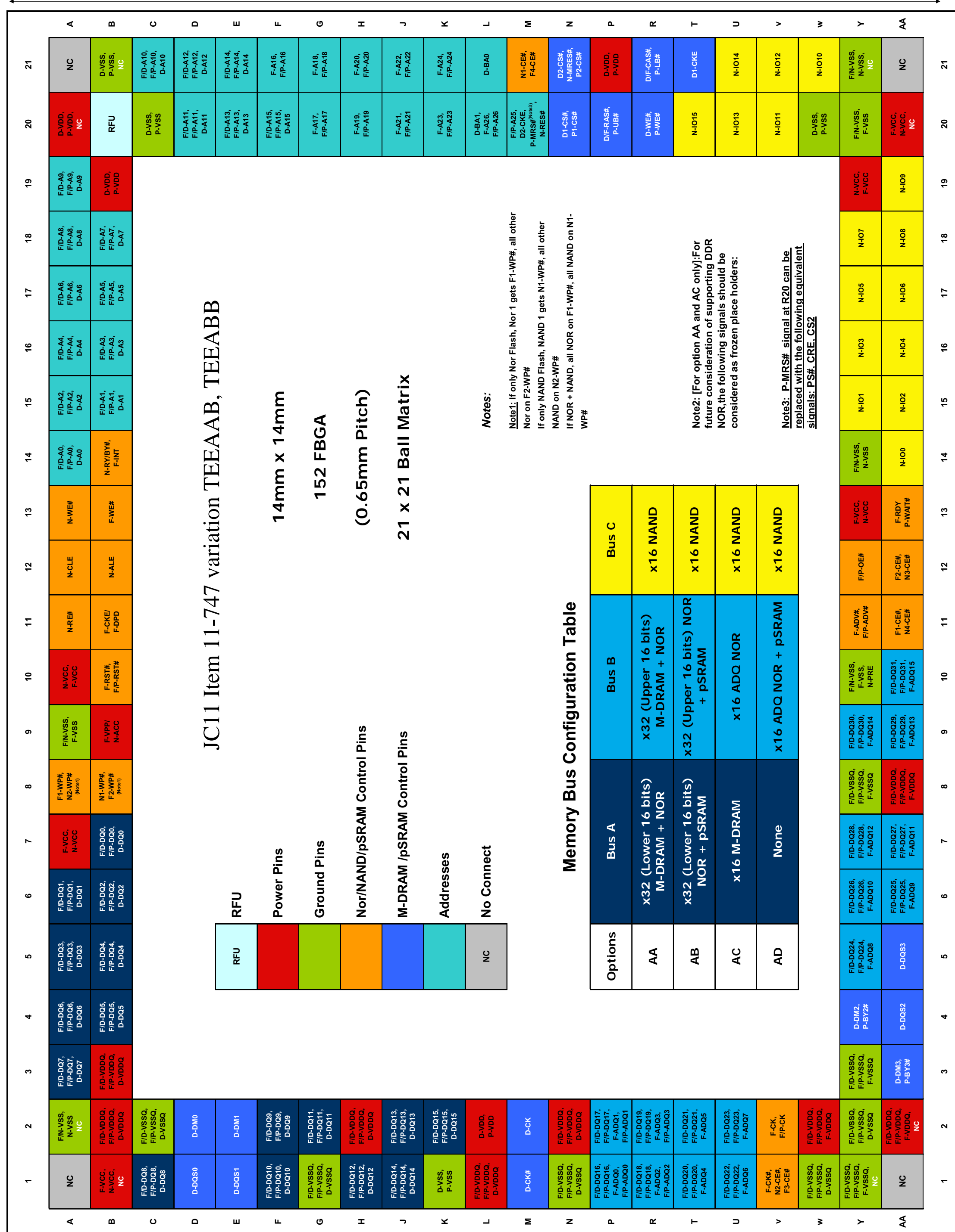
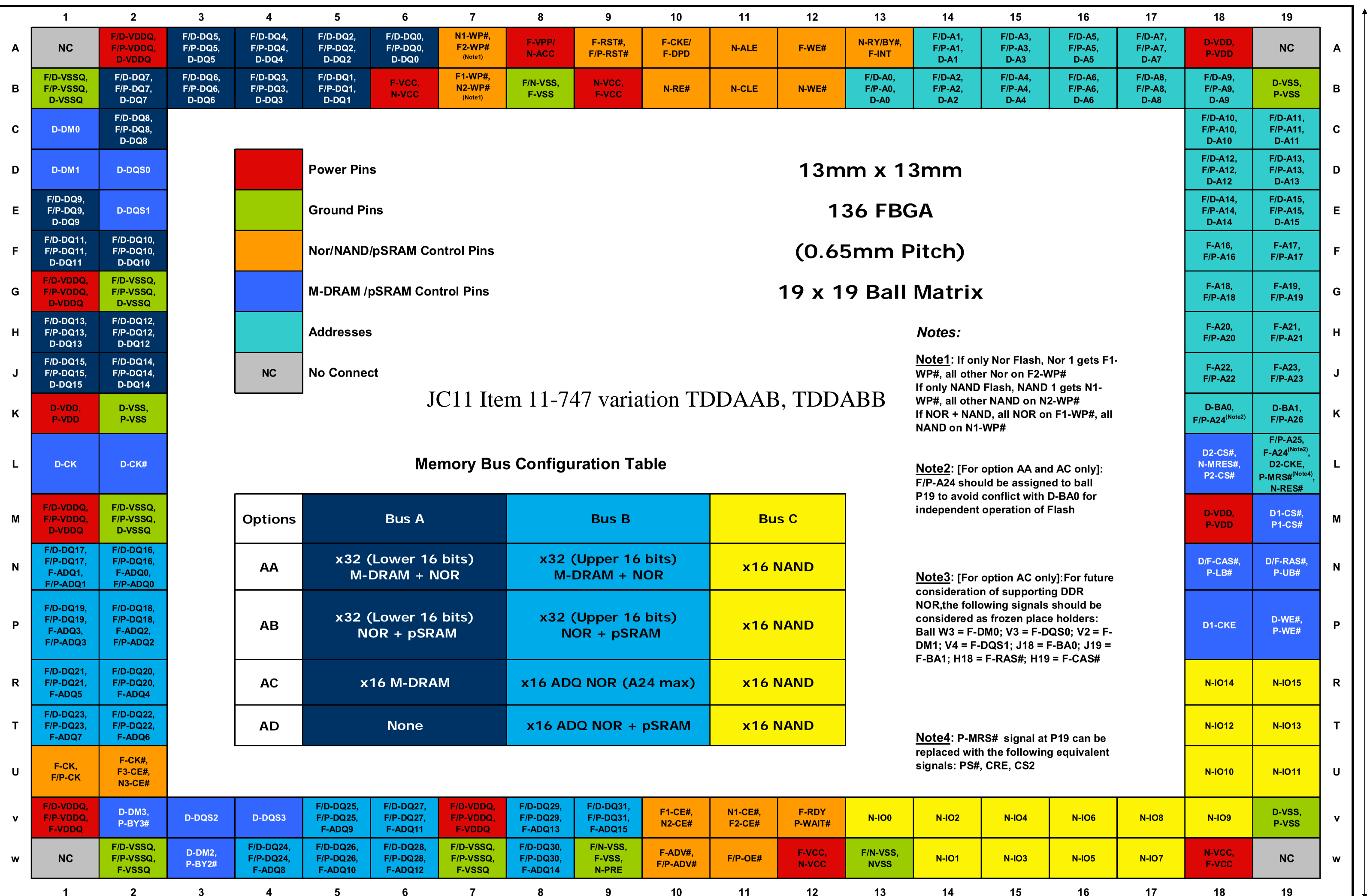


Figure 3.12.2-16
Ball Outline – 152-Ball FBGA, 0.65 mm Pitch, 14 mm x 14 mm Package



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	NC	F/D-VDDQ, F/P-VDDQ, D-VDDQ	F/D-DQ5, F/P-DQ5, D-DQ5	F/D-DQ4, F/P-DQ4, D-DQ4	F/D-DQ2, F/P-DQ2, D-DQ2	F/D-DQ0, F/P-DQ0, D-DQ0	N1-WP#, F2-WP# (Note1)	F-VPP/ N-ACC	F-RST#, F/P-RST#	F-CKE/ F-DPD	N-ALE	F-WE#	N-RY/BY#, F-INT	F/D-A1, F/P-A1, D-A1	F/D-A3, F/P-A3, D-A3	F/D-A5, F/P-A5, D-A5	F/D-A7, F/P-A7, D-A7	D-VDD, P-VDD	NC
B	F/D-VSSQ, F/P-VSSQ, D-VSSQ	F/D-DQ7, F/P-DQ7, D-DQ7	F/D-DQ6, F/P-DQ6, D-DQ6	F/D-DQ3, F/P-DQ3, D-DQ3	F/D-DQ1, F/P-DQ1, D-DQ1	F-VCC, N-VCC	F1-WP#, N2-WP# (Note1)	F/N-VSS, F-VSS	N-VCC, F-VCC	N-RE#	N-CLE	N-WE#	F/D-A0, F/P-A0, D-A0	F/D-A2, F/P-A2, D-A2	F/D-A4, F/P-A4, D-A4	F/D-A6, F/P-A6, D-A6	F/D-A8, F/P-A8, D-A8	F/D-A9, F/P-A9, D-A9	D-VSS, P-VSS
C	D-DM0	F/D-DQ8, F/P-DQ8, D-DQ8																F/D-A10, F/P-A10, D-A10	F/D-A11, F/P-A11, D-A11
D	D-DM1	D-DQS0																F/D-A12, F/P-A12, D-A12	F/D-A13, F/P-A13, D-A13
E	F/D-DQ9, F/P-DQ9, D-DQ9	D-DQS1																F/D-A14, F/P-A14, D-A14	F/D-A15, F/P-A15, D-A15
F	F/D-DQ11, F/P-DQ11, D-DQ11	F/D-DQ10, F/P-DQ10, D-DQ10																F-A16, F/P-A16	F-A17, F/P-A17
G	F/D-VDDQ, F/P-VDDQ, D-VDDQ	F/D-VSSQ, F/P-VSSQ, D-VSSQ																F-A18, F/P-A18	F-A19, F/P-A19
H	F/D-DQ13, F/P-DQ13, D-DQ13	F/D-DQ12, F/P-DQ12, D-DQ12																F-A20, F/P-A20	F-A21, F/P-A21
J	F/D-DQ15, F/P-DQ15, D-DQ15	F/D-DQ14, F/P-DQ14, D-DQ14																F-A22, F/P-A22	F-A23, F/P-A23
K	D-VDD, P-VDD	D-VSS, P-VSS																D-BA0, F/P-A24 (Note2)	D-BA1, F/P-A26
L	D-CK	D-CK#																D2-CS#, N-MRES#, P2-CS#	F/P-A25, F-A24 (Note2), D2-CKE, P-MRS# (Note4), N-RES#
M	F/D-VDDQ, F/P-VDDQ, D-VDDQ	F/D-VSSQ, F/P-VSSQ, D-VSSQ																D-VDD, P-VDD	D1-CS#, P1-CS#
N	F/D-DQ17, F/P-DQ17, F-ADQ1, F/P-ADQ1	F/D-DQ16, F/P-DQ16, F-ADQ0, F/P-ADQ0																D/F-CAS#, P-LB#	D/F-RAS#, P-UB#
P	F/D-DQ19, F/P-DQ19, F-ADQ3, F/P-ADQ3	F/D-DQ18, F/P-DQ18, F-ADQ2, F/P-ADQ2																D1-CKE	D-WE#, P-WE#
R	F/D-DQ21, F/P-DQ21, F-ADQ5	F/D-DQ20, F/P-DQ20, F-ADQ4																N-IO14	N-IO15
T	F/D-DQ23, F/P-DQ23, F-ADQ7	F/D-DQ22, F/P-DQ22, F-ADQ6																N-IO12	N-IO13
U	F-CK, F/P-CK	F-CK#, F3-CE#, N3-CE#																N-IO10	N-IO11
V	F/D-VDDQ, F/P-VDDQ, F-VDDQ	D-DM3, P-BY3#	D-DQS2	D-DQS3	F/D-DQ25, F/P-DQ25, F-ADQ9	F/D-DQ27, F/P-DQ27, F-ADQ11	F/D-VDDQ, F/P-VDDQ, F-VDDQ	F/D-DQ29, F/P-DQ29, F-ADQ13	F/D-DQ31, F/P-DQ31, F-ADQ15	F1-CE#, N2-CE#	N1-CE#, F2-CE#	F-RDY P-WAIT#	N-IO0	N-IO2	N-IO4	N-IO6	N-IO8	N-IO9	D-VSS, P-VSS
W	NC	F/D-VSSQ, F/P-VSSQ, F-VSSQ	D-DM2, P-BY2#	F/D-DQ24, F/P-DQ24, F-ADQ8	F/D-DQ26, F/P-DQ26, F-ADQ10	F/D-DQ28, F/P-DQ28, F-ADQ12	F/D-VSSQ, F/P-VSSQ, F-VSSQ	F/D-DQ30, F/P-DQ30, F-ADQ14	F/N-VSS, F-VSS, N-PRE	F-ADV#, F/P-ADV#	F/P-OE#	F-VCC, N-VCC	F/N-VSS, NVSS	N-IO1	N-IO3	N-IO5	N-IO7	N-VCC, F-VCC	NC

Options	Bus A	Bus B	Bus C
AA	x32 (Lower 16 bits) M-DRAM + NOR	x32 (Upper 16 bits) M-DRAM + NOR	x16 NAND
AB	x32 (Lower 16 bits) NOR + pSRAM	x32 (Upper 16 bits) NOR + pSRAM	x16 NAND
AC	x16 M-DRAM	x16 ADQ NOR (A24 max)	x16 NAND
AD	None	x16 ADQ NOR + pSRAM	x16 NAND

Figure 3.12.2-17
Ball Outline – 136-Ball FBGA, 0.65 mm Pitch, 13 mm x 13 mm Package

Table 3.12.2-2 – Signal Descriptions

Signal Name	Signal Type	Description (JESD21C for additional information)
D-CS#	I	CHIP SELECT : Low input enables and high input disables the command decoder
D-RAS#	I	ROW ADDRESS STROBE : Low-true input selects the rows of the address location selected
D-CAS#	I	COLUMN ADDRESS STROBE : Low-true input selects the columns of the address location selected
D-WE#	I	WRITE ENABLE : Low-true input controls the write operations to the selected die by determining whether a given cycle is a write cycle
D-A0~D-A14	I	Address input during read and write operation
D-BA0~D-BA1	I	BANK ADDRESS INPUT : Select the bank. ACTIVE, READ, WRITE or PRECHARGE command is being applied
D-DM0~D-DM3	I/O	INPUT/OUTPUT MASK : DM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses (Byte control)
D-DQ0~D-DQ31	I/O	DATA INPUT/OUTPUT-Inputs data and commands during write cycles, outputs data during read cycles
D-DQS0~D-DQS3	I/O	DATA STROBE: Output with Read, Input with Write. Edge-aligned with Read, Center-aligned with Write. Used to capture Write Data
VDD,VCC	Power	CORE VOLTAGE : single power supply
VDDQ	Power	INPUT/OUTPUT VOLTAGE : Supply power for the input and output buffers
VSS	Power	CORE GROUND : Connect to system ground - do not float
VSSQ	Power	INPUT/OUTPUT GROUND : Connect to system ground -do not float
N-CE#	I	CHIP ENABLE : Low-true input selects the associated memory die
N-RE#	I	READ ENABLE : Active low. Controls read timing. Clocking RE# increments the internal address and read out data
N-WP#	I	HARDWARE WRITE PROTECT : Low true input controls the associated flash memory die(s).
N-WE#	I	WRITE ENABLE : Low-true input controls the write operations to the selected die by determining whether a given cycle is a write cycle
N-ALE	I	ADDRESS LATCH ENABLE-Address is latched to the address register through NAND I/O ports on the rising edge of WE# when ALE is HIGH
N-I/O0~N-I/O15	I/O	Command, Address, Data input/output for NAND flash
N-RY/BY#	O	Ready/Busy indicates status of device operation. When low a program, erase, or read is in progress. It is usually and open-drain signal
N-CLE	I	COMMAND LATCH ENABLE-Command are latched to the command register through NAND I/O ports on the rising edge of WE# when CLE is High
N-PRE	I	Power on Auto Read Enable. Connect to VSS or NC
N-RES#	I	RES# should be low when power is on.
N-MRES#	O	Output reset signal to CPU when power on auto read mode and auto read mode are activated in certain AND memory
F-CK	I	CLOCK : Synchronize the memory chip with the system memory bus clock during burst operations
F-A0~F-A25	I	Address input during read and write operation
F-WP#	I	HARDWARE WRITE PROTECT : Low-true input controls the associated flash memory die(s).
F-CE#	I	CHIP ENABLE : Low-true input selects the associated memory die
F-OE#	I	OUTPUT ENABLE : Low-true input enables the output buffer when low
F-RST#	I	HARDWARE RESET : Low- true input initializes internal circuitry to reading array data
F-WE#	I	WRITE ENABLE : Low-true input controls the write operations to the selected die by determing whether a given cycle is a write cycle.

Signal Name	Signal Type	Description (JESD21C for additional information)
F-DPD	i	DEEP POWER DOWN. Controls pin used with some flash memory-enter/exit deep power down mode
F-VPP	I	ACCELERATED VOLTAGE LEVEL : At VHH, accelerates programming and automatically places device in unlock bypass mode. At VIL, disables all program and erase functions, VIH for all other operations
F-INT	O	Notify the host when a command has been completed
D-CK	I	CLOCK : Synchronize the memory chip with the system memory bus clock during burst operations
D-CK#	I	DDR CLOCK : Complement of CLK for DDR-enabled memory
D-CKE	I	CLOCK ENABLE : CKE activates(HIGH) and deactivates(LOW) the CLK signal

Table 3.12.2-3 – ADM Signal Description Table

A/DQ0 ~ A/DQ15	I/O	ADDRESS input for x16 bus width/DATA INPUT/OUTPUT 0- Inputs data and commands during write cycles, outputs data during read cycles
A/DQ16 ~ A/DQ31	I/O	ADDRESS input for x32 bus width/DATA INPUT/OUTPUT - Inputs data and commands during write cycles, outputs data during read cycles
A0 ~ Amax	I	Address input during read and write operations for x16 bus width
ADV#	I	ADDRESS DATA VALID: Low-true input during synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first.
ALE	I	Address Latch Enable - Address is latched to the address register through NAND I/O ports on the rising edge of WE# when ALE is High
BA0	I	BANK ADDRESS INPUT 0: Select the bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
BA1	I	BANK ADDRESS INPUT 1: Select the bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied
CAS#	I	COLUMN ADDRESS STROBE: Low-true input selects the columns of the address location selected
E0#	I	CHIP ENABLE: Low-true input selects the associated memory die
CKE	I	CLOCK ENABLE: CKE activates (HIGH) and deactivates (LOW) the CLK signal
CLE	I	Command Latch Enable - Commands are latched to the command register through NAND I/O ports on the rising edge of WE# when CLE is High
CK	I	CLOCK: Synchronizes the memory chip with the system memory bus clock during burst operations.
CK#	I	DDR CLOCK: Complement of CLK for DDR-enabled memory
CRE/ PMODE	I	CONTROL REGISTER ENABLE: High-true input when active write operations load the Refresh Control Register or Bus Control Register
D/F-DQS0:1	I	DDR Data strobe
D/F-DM0	I/O	INPUT/OUTPUT MASK 0: DM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses (DQ7-0)
D/F-DM1	I/O	INPUT/OUTPUT MASK 0: DM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses (DQ15-8)
DPD	I	Deep Power Down. Control pin used with some flash memory - enter/exit deep power down mode
DQ0 ~ DQ31	I/O	DATA INPUT/OUTPUT - Inputs data and commands during write cycles, outputs data during read cycles
D-VDD	Power	SDRAM CORE VOLTAGE: SDRAM single power supply
D-VDDQ	Power	SDRAM INPUT/OUTPUT VOLTAGE: Supply power for the input and output buffers
D-VSS	Power	SDRAM CORE GROUND: Connect to system ground - do not float
D-VSSQ	Power	SDRAM INPUT/OUTPUT GROUND: Connect to system ground – do not float

Table 3.12.2-3 – ADM Signal Description Table (Cont.)

LB#	I	LOWER BYTE ENABLE: Low-true input enables the lower bytes for RAM (DQ7-0)
N-I/O0 ~ N-I/O7	I/O	Command, Address, Data input/output for NAND Flash
N-I/O8 ~ N-I/O15	I/O	Data input/output for NAND Flash
N-PRE	I	Power on auto read enable. Connect to VSS or NC
N-MRES#	O	Output reset signal to CPU when power on auto read mode and auto read mode are activated in certain AND memory.
N-RES#	I	RES# should be low when power is on. Device is initialized upon L to H transition. RES# = L puts the device in deep standby. Used with certain AND memory
OE#	I	OUTPUT ENABLE: Low-true input enables the output buffers when low. When OE# is high, the output buffers are disabled.
RAS#	I	ROW ADDRESS STROBE: Low-true input selects the rows of the address location selected
RY/BY#	O	Ready / Busy indicates status of device operation. When Low a program, erase, or read is in progress. It is usually and open-drain signal.
RE#	I	Read Enable. Active low. Controls read timing. Clocking RE# increments the internal address and reads out data
RST#	I	HARDWARE RESET: Low-true input initializes internal circuitry to reading array data
UB#	I	UPPER BYTE ENABLE: Low-true input enables the upper bytes for RAM (DQ15-8)
V-Ref	O	SSTL-2 reference voltage. Voltage reference for data output.
VDD	Power	CORE VOLTAGE: single power supply
VDDQ	Power	INPUT/OUTPUT VOLTAGE: Supply power for the input and output buffers
VPP (ACC)	I	ACCELERATED VOLTAGE LEVEL: At VHH, accelerates programming and automatically places device in unlock bypass mode. At VIL, disables all program and erase functions, VIH for all other operations.
VSS	Power	CORE GROUND: Connect to system ground - do not float
VSSQ	Power	INPUT/OUTPUT GROUND: Connect to system ground – do not float
WAIT (RDY)/DQS0	O	DEVICE READY: Indicates the status of the burst read operation/DATA STROBE PIN 0: Edge detector for when data is available on the bus (DQ7-0)
WAIT	O	WAIT: Indicates the status of the burst read operation/DATA STROBE PIN 0: Edge detector for when data is available on the bus (DQ7-0)
WE#	I	WRITE ENABLE: Low-true input controls the write operations to the selected die by determining whether a given cycle is a write cycle.
WP1#	I	HARDWARE WRITE PROTECT: Low-true input controls the associated flash memory die(s). If only NOR Flash, NOR #1 gets F-WP1#, and all other NOR gets F-WP2#. If NOR and NAND, then all NOR gets F-WP1#, and all NAND gets F-WP2#.
WP2#	I	HARDWARE WRITE PROTECT: Low-true input controls the associated flash memory die(s). If only NOR Flash, NOR #1 gets F-WP1#, and all other NOR gets F-WP2#. If NOR and NAND, then all NOR gets F-WP1#, and all NAND gets F-WP2#.

ISM Details

- ISM Memory Configuration
- 256Mb/512Mb SDRAM x32 DDR
- ~ 98 external I/O including pwr/gnd on single side as shown below
- Nominal 12 mm x 12 mm x 0.38mm
- ISM Package Details (pad array for reference only)

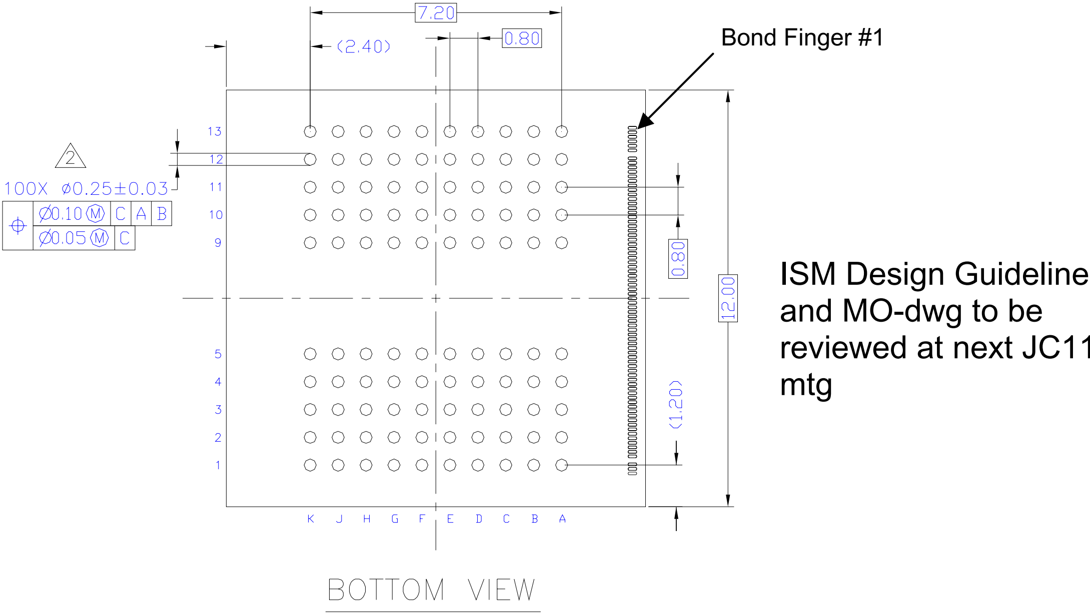


Figure 3.12.2-18 - SDRAM Internal Stacking Module

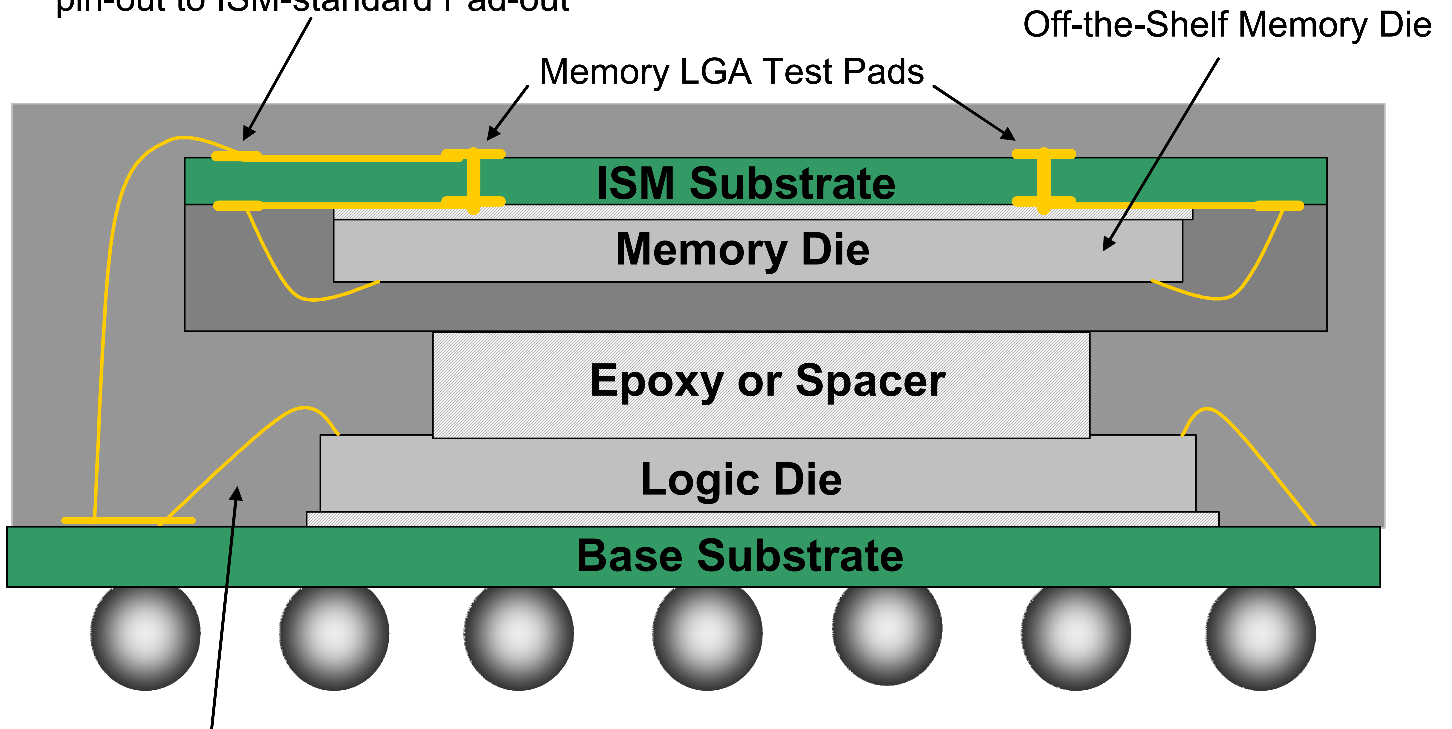


Figure 3.12.2-19 - Explanation of ISM Standardization Concept

- Proposal below is for external bond finger pad-out for a 256Mb/512Mb SDRAM x32 DDR ISM substrate
- ISM package test pad array and netlist is per memory supplier's preference

ISM BF Netlist	Bond Finger	ISM BF Netlist	Bond Finger	ISM BF Netlist	Bond Finger	ISM BF Netlist	Bond Finger
vss	BF1	dq19	BF26	vdd	BF51	dq10	BF76
vdd	BF2	dq18	BF27	clk	BF52	dq9	BF77
pwrdwn	BF3	dq17	BF28	clkb	BF53	dq8	BF78
dq31	BF4	dq16	BF29	vss	BF54	vssq	BF79
dq30	BF5	vddq	BF30	a12	BF55	vddq	BF80
vddq	BF6	vssq	BF31	a10	BF56	dm0	BF81
vssq	BF7	dqs2	BF32	a8	BF57	dqs0	BF82
dq29	BF8	dm2	BF33	a6	BF58	dq7	BF83
dq28	BF9	vss	BF34	a4	BF59	dq6	BF84
dq27	BF10	vdd	BF35	a2	BF60	vddq	BF85
dq26	BF11	cke	BF36	ba0	BF61	vssq	BF86
vssq	BF12	web	BF37	ba1	BF62	dq5	BF87
vddq	BF13	casb	BF38	vdd	BF63	dq4	BF88
dq25	BF14	rasb	BF39	vss	BF64	dq3	BF89
dq24	BF15	a1	BF40	dm1	BF65	dq2	BF90
dqs3	BF16	a3	BF41	dqs1	BF66	vssq	BF91
dm3	BF17	a5	BF42	vssq	BF67	vddq	BF92
vddq	BF18	a7	BF43	vddq	BF68	dq1	BF93
vssq	BF19	a9	BF44	dq15	BF69	dq0	BF94
dq23	BF20	a11	BF45	dq14	BF70	ts0	BF95
dq22	BF21	a0	BF46	dq13	BF71	ts1	BF96
dq21	BF22	a13 (512Mb only)	BF47	dq12	BF72	vdd	BF97
dq20	BF23	a14 (512Mb only)	BF48	vddq	BF73	vss	BF98
vssq	BF24	cs	BF49	vssq	BF74		
vddq	BF25	hi-v	BF50	dq11	BF75		

vddq
vssq
vdd
vss
dq
Address

Figure 3.12.2-20- Pad-Out Proposal

Design Criteria for Pad-out Proposal

- One Vssq/Vddq pair with every 4 data lines (DQx, x=0..31). This is optimal for reducing switching noise/ground bounce.
- All the data lines (DQ pads) are in the two outer sides. The critical control signals (clk, WE, Cas, Ras etc) are towards the middle of the Stacked Memory Interface (SMI) bus.
- All adjacent address lines are separated (A(x), A(x+2)) – this reduces cross talk among the high activity lines
- Clk and clkb have a Vss/Vdd line on either side
- The nonstandard pins are kept on the very outside ends.
- The DMx/DQSx are set up with the ‘x’ data byte (X=0..3)
- VDDQ/VSSQ swapping across DQ groups for better routing

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	NU	NU	D-VDDQ	D-DMb	D-DQb	D-DQb	VSS	D-DQb	D-DQb	D-DQc	D-DQc	D-CK	VSS	D-DMc	D-VDDQ	D-DQc	D-DQc	D-DMd	D-DQSd	NU	NU
B	NU	RFU,NC	D-DQa	D-DQa	D-VDDQ	D-DQb	D-DQb	D-DQSb	D-DQb	D-DQb	D-DQc	D-DQc	D-CK#	VSS	D-DQSc	D-VDD	D-DQc	D-DQc	D-DQd	RFU,NC	NU
C	VSS	D-DQSa																		D-DQd	D-DQd
D	D-DQa	D-DQa																		D-DQd	D-DQd
E	D-DQa	D-DQa																		D-DQd	D-DQd
F	VSS	D-VDDQ																		VSS	D-VDDQ
G	D-DQa	D-DQa																		D-A0	D-DQd
H	D-DMa	VSS																		VSS	D-VDD
J	D-VDD	F-ADQ14																		D-A2	D-A3
K	F-WE	F-ADQ15																		D-A1	D-A9
L	F-CK	F-OE#																		D-VDDQ	VSS
M	F-ADQ13	VSS																		D-A7	D-A6
N	F-ADQ10	F-VDD																		D-A8	D-A11
P	F-ADQ12	F-ADQ11																		VSS	D-VDD
R	F-ADQ8	VSS																		D-A5	D-A12
T	F-ADQ9	F-VDD																		D-CS1#	D-CS0#
U	F-ADQ1	F-ADQ0																		D-CAS#	D-A4
V	F-ADQ3	F-ADQ2																		D-BA1	D-RAS#
W	F-CE1#	DU																		VSS	D-VDDQ
Y	NU	RFU,NC	F-ADQ6	F-ADQ7	F-WP#	VSS	F-VDD	F-WAIT1,	DU	F-WAIT0,	VSS	D-A14	D-CKE1	D-VDD	D-CKE0	D-A10	VSS	D-WE#	VSS	RFU,NC	NU
AA	NU	NU	F-ADQ4	F-ADQ5	F-RST#, RP#	F-VDD	VSS	F-CE0#	F-ADV#,	F-NBE0,	D-VDD	D-TQ	VSS	D-VDDQ	D-A13	VSS	D-VDD	D-BA0	D-VDDQ	NU	NU

14X14 mm 152 Ball PACKAGE 0.65 mm pad pitch

A1 in Top Left, Top View

Legend:

- Dram DQ Byte a
- Dram DQ Byte c
- Dram DQ Byte b
- Dram DQ Byte d
- DRAM Address/Control
- DRAM VDD
- DRAM VDDQ
- VSS
- DRAM TQ

- Flash Mutiplexed Data/Address
- Flash Control
- Flash VDD
- Flash VDDQ
- VSS
- NU
- DU or RFU,NC

X16 is also supported with Byte b and Byte c

Figure 3.12.2-21
PoP 14X14 mm body size, 0.65 mm pad pitch based on a true split DRAM and Non-volatile bus structure

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NU	NU	D-DQc	D-VDDQ	D-DQc	D-DMc	D-VDDQ	D-DQc	D-DQc	D-VDDQ	D-CK	D-VDD	D-DQb	D-DQb	D-VDDQ	D-DQb	D-DMb	D-VDDQ	D-DQb	D-DMd	D-DQd	NU	NU
B	NU	RFU,NC	D-DQc	D-VSSQ	D-DQc	D-DQSc	D-VSSQ	D-DQc	D-DQc	D-VSSQ	D-CK#	VSS	D-DQb	D-DQb	D-VSSQ	D-DQb	D-DQSb	D-VSSQ	D-DQb	D-DQSd	D-DQd	RFU, NC	NU
C	D-Dma	D-DQSa																				D-VSSQ	D-VDDQ
D	D-DQa	D-DQa																				D-DQd	D-DQd
E	D-VDDQ	D-VSSQ																				D-DQd	D-DQd
F	D-DQa	D-DQa																				D-VSSQ	D-VDDQ
G	D-DQa	D-DQa																				D-DQd	D-DQd
H	D-VDDQ	D-VSSQ																				VSS	D-VDD
J	D-DQa	D-DQa																				D-CKE0	D-CKE1
K	D-VDD	VSS																				VSS	D-WE#
L	F-VDD	VSS																				D-CAS#	D-RAS#
M	F-ADQ1	F-ADQ0																				D-CS0#	D-CS1#
N	F-ADQ3	F-ADQ2																				D-A0	D-A1
P	F-VDDQ	F-VSSQ																				D-A2	D-A3
R	F-ADQ5	F-ADQ4																				D-A4	D-A5
T	F-ADQ7	F-ADQ6																				D-A6	D-A7
U	F-VDD	VSS																				D-A8	D-A9
V	F-WE#	F-OE#																				D-A10	D-A11
W	F-ADV#, ALE#	F-CK																				D-A12	D-A13
Y	F-CE1#	F-CE0#																				D-A14	D-VDD
AA	F-VDD	VSS																				VSS	D-VDD
AB	NU	RFU,NC	F-ADQ8	F-ADQ10	F-VSSQ	F-ADQ12	F-ADQ14	VSS	DU	F-WP#	F-RST#, RP#	F-WAIT0, RY0	VSS	DU	F-A17	F-A19	F-A21	F-A23	F-A25	DU	D-BA0	RFU,NC	NU
AC	NU	NU	F-ADQ9	F-ADQ11	F-VDDQ	F-ADQ13	F-ADQ14	F-VDD	DU	F-WAIT1, RY1	F-VPP	F-NBE0, CLE0	F-VDD	D-TQ	F-A16	F-A18	F-A20	F-A22	F-A24	DU	D-BA1	NU	NU

168 PACKAGE TOP SIDE

A1 in Top Left, Top View

12X12 mm Pad pitch=0.5mm

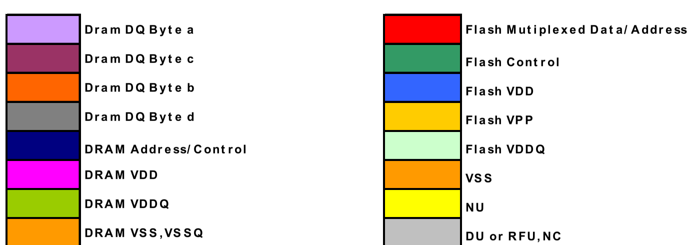


Figure 3.12.2-22
PoP 12X12 mm body size, 0.50 mm pad pitch based on a true split DRAM and Non-volatile bus structure

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	DNU	VSS_a/b	VDD2_a/b	DQ30_a	DQ29_a	VSSQ_a	DQ26_a	DQ25_a	VSSQ_a	DQS3_c_a	VSSQ_a	DQ14_a	DQ13_a	VSS_a	VDD1_a	VDD2_a	DQ11_a	DQ10_a	DQ9_a	DQS1_t_a	DM1_a	VDDQ_a	DQS0_t_a	DQ7_a	DQ6_a	DQ4_a	DQ3_a	VSS_a/b	DNU
B	VSSQ_b/VSS	VACC	DQ31_a	VDDQ_a	DQ28_a	DQ27_a	VDDQ_a	DQ24_a	VDDQ_a	DQS3_t_a	DM3_a	DQ15_a	VDDQ_a	VSSQ_a	Vref(DQ)_a	VDD2_a	DQ12_a	VDDQ_a	DQ8_a	DQS1_c_a	VSSQ_a	DM0_a	DQS0_c_a	VSSQ_a	VDDQ_a	DQ5_a	DQ2_a	VACC	VSSQ_a
C	VDD1_a/b	DQ16_b																										VDD1_a	VDD2_a/b
D	DQ17_b	VDDQ_b																										DQ1_a	VDDQ_a
E	DQ18_b	DQ19_b																										VSSQ_a	DQ0_a
F	VSSQ_b	DQ20_b																										DM2_a	VDDQ_a
G	DQ21_b	VDDQ_b																										DQS2_t_a	DQS2_c_a
H	DQ22_b	DQ23_b																										VSSQ_a	DQ23_a
J	VSSQ_b	VDDQ_b																										VDDQ_a	DQ22_a
K	DQS2_c_b	DQS2_t_b																										DQ20_a	DQ21_a
L	DM2_b	DQ0_b																										DQ19_a	VSSQ_a
M	DQ1_b	VSSQ_b																										VDDQ_a	DQ18_a
N	DQ2_b	VDD1_b																										DQ16_a	DQ17_a
P	VSS_b	VSS_b																										VDD2_b	VDD1_b
R	VDD1_b	Vref(DQ)_b																										VSS_b	CA0_b
T	VDD2_b	VDD2_b																										VDDCA_b	CA1_b
U	VDDQ_b	DQ3_b																										Vref(CA)_b	CA2_b
V	DQ4_b	VSSQ_b																										VSSCA_b	CA3_b
W	DQ6_b	DQ5_b																										CA4_b	CSB1_b
Y	VDDQ_b	DQ7_b																										CSB0_b	CKE1_b
AA	DQS0_t_b	DQS0_c_b																										VSSCA_b	CKE0_b
AB	DM0_b	VSSQ_b																										CK_t_b	CK_c_b
AC	VDDQ_b	DM1_b																										VDDCA_b	CA5_b
AD	DQS1_c_b	DQS1_t_b																										CA7_b	CA6_b
AE	DQ8_b	VSSQ_b																										CA8_b	VDDCA_b
AF	DQ9_b	VDDQ_b																										VSSCA_b	CA9_b
AG	DQ10_b	DQ11_b																										VDD2_a/b	ZQ_b
AH	VSSQ_b	VDD1_a/b	VDD2_a/b	DQ13_b	VSSQ_b	DQ15_b	DM3_b	DQS3_t_b	VDDQ_b	DQ26_b	DQ27_b	VDDQ_b	DQ30_b	VSSQ_b	VDD2_a	Vref_(CA)_a	CA9_a	VSSCA_a	CA7_a	CA6_a	CK_c_a	VDDCA_a	CKE0_a	CSB0_a	CA3_a	CA2_a	CA1_a	VDD1_a/b	VSSCA_a
AJ	DNU	VSS_a/b	DQ12_b	VDDQ_b	DQ14_b	VDDQ_b	VSSQ_b	DQS3_c_b	DQ24_b	DQ25_b	VSSQ_b	DQ28_b	DQ29_b	DQ31_b	VDD1_a	VSS_a	ZQ_a	CA8_a	VDDCA_a	CA5_a	CK_t_a	VSSCA_a	CKE1_a	CSB1_a	CA4_a	VDDCA_a	CA0_a	VSS_a/b	DNU

Channel b
Channel a
Power
Ground
Do not use
ZQ

12X12 mm, 0.4mm pitch, 29 rows
216 Ball Count
Top View A1 in Top Left Corner

Figure 3.12.2-23
PoP 12X12 mm body size, 0.40 mm pad pitch for a two channel LPDDR2 PoP memory.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	DNU	DNU	RDY,R/B#, WAIT,WAI T#,CMDm	CLK CLKm	ADQ11 DAT6m	VCCmm	ADQ10 DAT4m	ADQ9 DAT2m	VCCQmm	ADQ8 DAT0m	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_C	VDD1	VSS	DNU	DNU
B	DNU	DNU	VDD1	ADQ3 DAT7m	VSSmm	ADQ2 DAT5m	ADQ1 DAT3m	VSSmm	ADQ0 DAT1m	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_T	VDDQ	DM3	VDD2	DNU	DNU
C	VSS	VDD2																				DQ15	VSSQ
D	ADQ12	ADQ4																				VDDQ	DQ14
E	ADQ13	ADQ5																				DQ12	DQ13
F	VCCQmm VDDImm	VSSmm																				DQ11	VSSQ
G	ADQ14	ADQ6																				VDDQ	DQ10
H	ADQ15	ADQ7																				DQ8	DQ9
J	VCCmm	VSSmm																				DQS1_T	VSSQ
K	WE#	OE#/ RE#																				VDDQ	DQS1_C
L	RP#, RST_n, CLE,DPD	AVD#, ADV#, ALE																				VDD2	DM1
M	CE#	VSS																				VREF (DQ)	VSS
N	INT#,WP#	VDD1																				VDD1	DM0
P	ZQ	VREF (CA)																				DQS0_C	VSSQ
R	VSS	VDD2																				VDDQ	DQS0_T
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK_C	CK_T																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	DNU	DNU	CS0_N	CS1_N	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_T	VDDQ	DM2	VDD2	DNU	DNU
AC	DNU	DNU	CKE0	CKE1	VSS	CA0	CA2	VDDCA	VSSmm	VCCmm	VACC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_C	VDD1	VSS	DNU	DNU

VCCmm	3	(3V or 1.8V depending on technology)	VSSmm	5
VCCQmm	2	(includes VDDI)		
VDD2	8		VSS	10
VDD1	7			
VDDCA	3		VSSCA	2
VDDQ	12		VSSQ	12
VREF	2			
VACC	1			
NC	16			

Color	Legend
Light blue	x32 LPDDR2 DQs
Yellow	LPDDDR2 CMD/Address
Magenta	Flash Memory (eMMC/MuxOneNAND/NAND/AADMuxNOR) ADQ/CTRL
Red	Power
Green	Ground

Ball Location	MUX One-NAND	eMMC	Raw NAND	AAD-Mux NOR	Comment
A3	RDY / WAIT#	CMDm	R/B#	WAIT	
A4	CLK	CLKm	NC	CLK	
K1	WE#	NC	WE#	WE#	
K2	OE#	NC	RE#	OE#	
L1	RP#	**RST_n (Ver 4.4)**	CLE	RST# / DPD	DPD must be configured active high via ECR
L2	AVD#	NC	ALE	ADV#	
N1	INT	NC	WP#	WP#	

Figure 3.12.2-24
LPDDR2 12X12 PoP 0.50 mm ball pitch one-channel x32 + SDR NVM Ballout

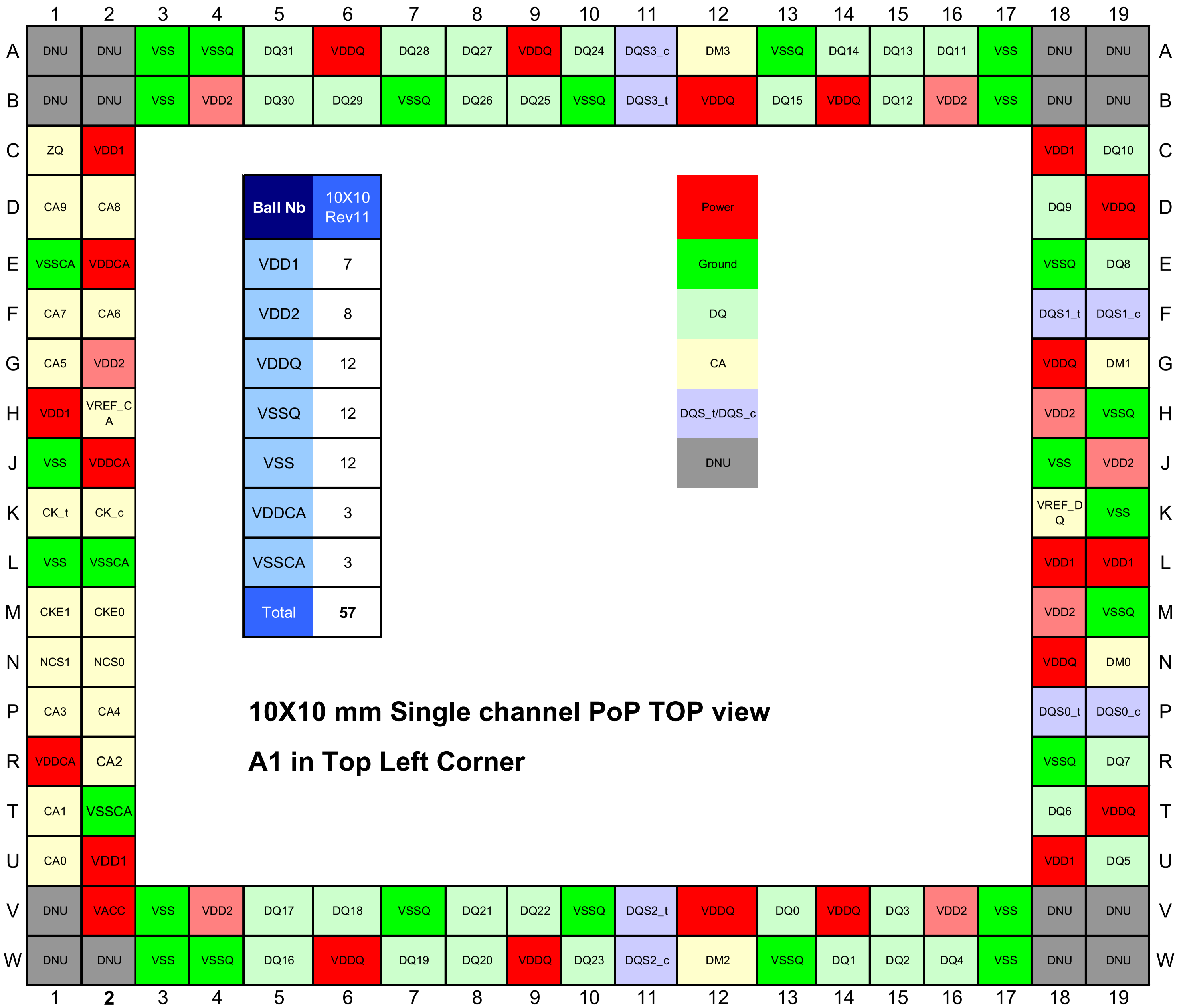


Figure 3.12.2-25
PoP 10X10 mm body size, 0.50 mm pad pitch for a single Channel LPDDR2 only

Top View – ball side down

	1	2	3	4	5	6	7	8	9
A	NC	CA9	VDD2	VDD 1	VSSQ	DQ14	DQ12	VDD2	NC
B	CA7	CA8	ZQ	VSS	DQ15	DQ13	VDD Q	VSS Q	DQ11
C	CA5	CA6						DQ10	DQ9
D	VDDC A	VSSC A		CKE2 CS3#	VSSQ	DQS1		DQ8	VDD Q
E	VDD2	VREF (CA)		CKE1	VDD Q	DQS1 #		DM1	VSS
F	VSS	VSSC A		CKE0	VSS	VDD1		VDD2	VREF (DQ)
G	VDDC A	CK		CS1#	VSSQ	DQS0 #		DM0	VDD1
H	CK#	CS0#		CS2#	VDD Q	DQS0		DQ7	VDD Q
J	CA4	CA3						DQ5	DQ6
K	CA2	CA1	VAC C	VSS	DQ0	DQ2	VDD Q	VSS Q	DQ4
L	NC	CA0	VDD2	VDD 1	VSSQ	DQ1	DQ3	VDD2	NC

Note: The ZQ ball used when operating above 200 Mhz is limited to a 5pf load (typically 2 die using CKE0,1 and CS0,1)

Figure 3.12.2-26
LPDDR2 x16 (NVM/DRAM) 79-ball 0.5 mm pitch

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
A	DNU	VSS_a/b	VDD2_a/b	DQ31_a	VDDQ_a	VSSQ_a	DQ26_a	DQ24_a	DQS3_t_a	DM3_a	DQ15_a	DQ13_a	VSSQ_a	VDDQ_a	DQ8_a	VSSQ_a	Vref(DQ)_a	VDD1_a/b	VDDQ_a	VSSQ_a	DQ7_a	DQ5_a	VSSQ_a	VDDQ_a	VDD1_a/b	VSSQ_a	DNU
B	VSSQ_b	VACC	VSSQ_a	DQ30_a	DQ29_a	DQ27_a	VDDQ_a	VSSQ_a	DQS3_c_a	VSSQ_a	DQ14_a	DQ12_a	DQ11_a	DQ9_a	DQS1_c_a	VDDQ_a	VSS_a/b	VDD2_a/b	DQS0_c_a	DM0_a	DQ6_a	DQ4_a	DQ3_a	DQ1_a	DQ0_a	VACC	VSS_a/b
C	VDD1_a/b	DQ16_b			DQ28_a		DQ25_a		VDDQ_a		VDDQ_a		DQ10_a		DQS1_t_a		DM1_a		DQS0_t_a		VDDQ_a		DQ2_a			DM2_a	VDD2_a/b
D	DQ17_b	VDDQ_b																								VDDQ_a	DQS2_c_a
E	DQ18_b	DQ19_b	VSSQ_b																						VSSQ_a	DQS2_t_a	DQ23_a
F	DQ20_b	DQ21_b																								DQ22_a	VDDQ_a
G	VDDQ_b	DQ22_b	DQ23_b																						DQ21_a	DQ20_a	VSSQ_a
H	VSSQ_b	DQS2_t_b																								DQ19_a	DQ18_a
J	DQS2_c_b	VDDQ_b	DM2_b																						VDDQ_a	DQ17_a	DQ16_a
K	VSSQ_b	DQ0_b																								VSSQ_a	VDD2_a/b
L	DQ1_b	VDDQ_b	DQ2_b																						CA0_b	VDD1_a/b	VSS_a/b
M	DQ3_b	VSSQ_b																								CA1_b	VSSCA_b
N	DQ4_b	DQ5_b	VDDQ_b																						CA3_b	CA2_b	VDDCA_b
P	DQ6_b	DQ7_b																								CA4_b	CSB1_b
R	VDDQ_b	DQS0_t_b	DQS0_c_b																						CKE0_b	CSB0_b	CKE1_b
T	VSSQ_b	VSS_a/b																								CK_c_b	CK_t_b
U	Vref(DQ)_b	VSS_a/b	DM0_b																						VDD2_a/b	VDDCA_b	VSSCA_b
V	VDD1_a/b	VDD1_a/b																								VSS_a/b	Vref(CA)_b
W	DM1_b	VDD2_a/b	VDD2_a/b																						CA5_b	VDDCA_b	VSSCA_b
Y	VDDQ_b	VSSQ_b																								CA7_b	CA6_b
AA	DQS1_c_b	DQS1_t_b	DQ8_b																						VDD2_a/b	CA9_b	CA8_b
AB	VDDQ_b	DQ9_b																								VSS_a/b	ZQ_b
AC	DQ10_b	DQ11_b	VSSQ_b																						DNU	DNU	VDD1_a/b
AD	DQ13_b	DQ12_b																								DNU	DNU
AE	VDD1_a/b	DQ14_b			VSSQ_b		DQ27_b		DQ30_b		VDD2_a/b		CA6_a		CA5_a		VDD2_a/b		CA4_a		VSS_a/b		DNU			DNU	DNU
AF	VSSQ_b	VDDQ_b	DQ15_b	VDDQ_b	DQS3_t_b	DQ25_b	DQ26_b	DQ28_b	VDDQ_b	VSSQ_b	VSS_a/b	CA9_a	CA7_a	VDDCA_a	VSS_a/b	VDDCA_a	CK_t_a	CKE0_a	CSB0_a	CA2_a	VSSCA_a	CA0_a	VDD2_a/b	DNU	DNU	DNU	DNU
AG	DNU	VSS_a/b	VDD2_a/b	DM3_b	DQS3_c_b	DQ24_b	VDDQ_b	VSSQ_b	DQ29_b	DQ31_b	VDD1_a/b	ZQ_a	CA8_a	VSSCA_a	Vref(CA)_a	VSSCA_a	CK_c_a	CKE1_a	CSB1_a	CA3_a	VDDCA_a	CA1_a	VDD1_a/b	DNU	DNU	DNU	DNU

14X14 mm, 0.5mm pitch, 27 rows

240 Ball Count

Top View A1 in Top Left Corner

Channel b
Channel a
Power
Ground
Do not use
ZQ

Figure 3.12.2-27
Dual LPDDR2 Package-on-Package, 240-ball,14 mm x 14 mm, 0.5 mm pitch

Dual LPDDR2 Package Definition

- Uses mechanical outline MO-273, variation VEEBDC
- 240 balls
- Internal row partially populated

Table 3.12.2-4 — Dual LPDDR2 Ball Count

Ball Type	Ball Count	Comment
DQ	64	
DQS	16	
DM	8	
CS	4	
CKE	4	
CA	20	
ZQ	2	
CK	4	
VDD1	10	
VDD2	12	
VDDQ	24	
VDDCA	6	
VSS	12	Shared by VDD1 and VDD2
VSSQ	24	
VSSCA	6	
VREF	4	
VACC	2	
DNU	18	Do not use
Total	240	