3.12 Multi-Chip Packages (MCP)

Section 3.12 contains primarily electrical interface items related to Multi-Chip Packages (MCP) and Stacked-Chip Scale Packages (SCSP) of mixed memory technologies including Flash (NOR and NAND), SRAM, PSRAM, LPDRAM, etc. These items include die-on-die stacking within a single encapsulated package, package-on-package or module-in-package technologies, etc. Section 3.12 also contains Silicon Pad Sequence information for the various memory technologies to aid in the design and electrical optimization of the memory sub-system or complete memory stacked solution.

MCP standards published prior to 2005 are located in the appropriate sections of 21C; they will be moved into this section in a future Release of 21C.

Section 3.12.1 MCP

Section 3.12.2 Package-on-Package (PoP) and Internal Stacked Module (ISM)

Section 3.12.3 Silicon Pad Sequences