

### 3.11.5.7 – GDDR3 Specific SGRAM Functions

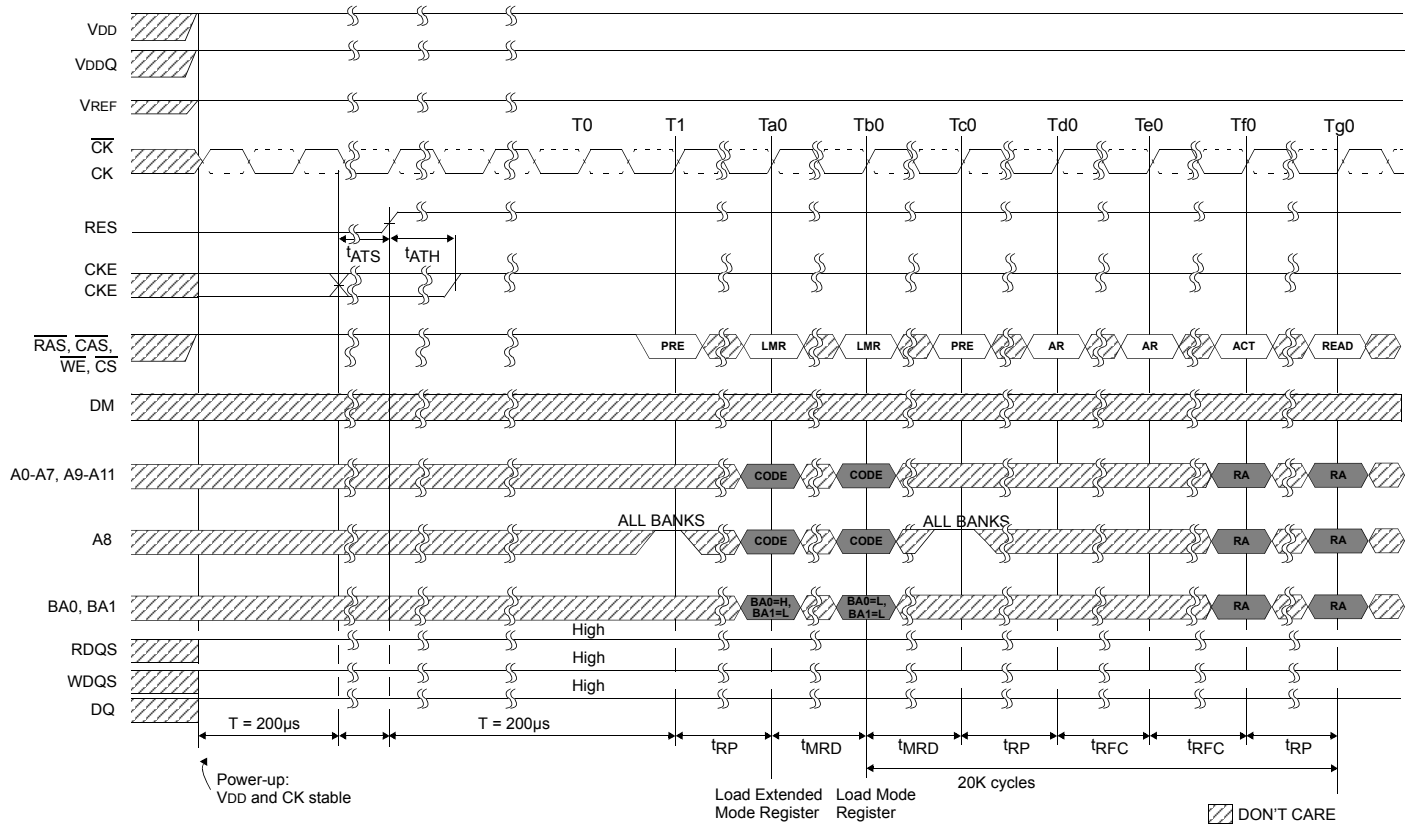
#### Initialization and Power Up

GDDR3 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simultaneously, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200 $\mu$ s before the RES pin transitions to high. Upon power-up and after the clock is stable, the on die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200 $\mu$ s is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state.

After the RES pin transitions from LOW to HIGH wait until a 200 $\mu$ s delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 20k clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SGRAM is ready for normal operation.



## ODT Control

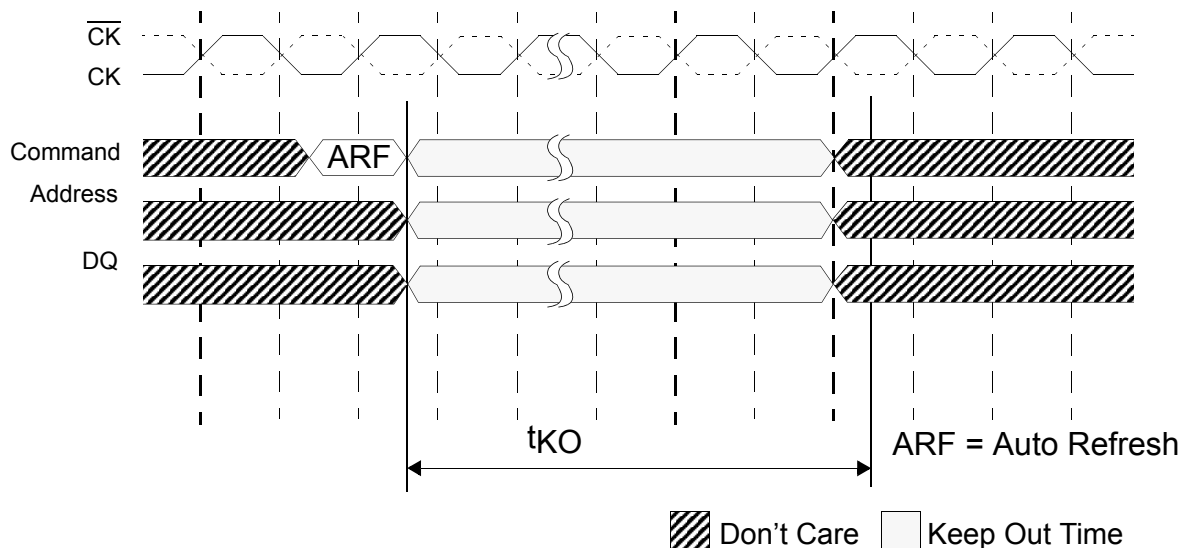
Bus snooping for READ commands excluding CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ on die terminations when a READ command is detected regardless of the state of CS#. The on die terminations are disabled  $x$  clocks after the READ command where  $x$  equals  $CL - 1$  and stay off for a duration of  $BL/2 + 2tCK$ . In a two-rank system, DRAM devices on both ranks snoop the bus for READ commands to devices on either rank and all DRAMs will disable the on die terminations, for the DQ pins if a READ command is detected. The on die terminations for input pins on the device such as command (except RES), address, WDQS and DM are always on for both a single-rank system and a dual-rank system unless it is turned off in the EMRS.

## ODT Updating

The GDDR3 SGRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSSQ. The value of the resistor must be six times the desired driver impedance. For example, a 240  $\Omega$ . resistor is required for an output impedance of 40  $\Omega$ . To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210  $\Omega$  to 270  $\Omega$  (35 $\Omega$  – 45  $\Omega$  output impedance).

The output impedance and on die termination is updated during every AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SGRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is  $9 \times 7.8$  us (70.2 us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SGRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries. During the minimum keep out time of tKO after AUTO REFRESH command, DES (i.e. /CS HIGH) should be issued on the command bus, and no activity on the address or data bus is recommended, because the signal integrity on the bus can not be guaranteed during this period.



## Definition of Terminology

Hereafter are defined terminologies used in the GDDR3 SGRAM specification.

Although GDDR3 might be operated in ODT Disable Mode, it is not recommended and the specification describes the ODT Enable Mode only. Should a system be designed to operate the GDDR3 in ODT Disable Mode, the system should comprehend the effect of the discrepancies between this specification and its own design.

If it is stated that a bus is in one of the following state, it should be interpreted as described.

Following are three terminologies defined for ODT Enable Mode.

**High {terminated}**: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

**Hi-z {terminated}**: No driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

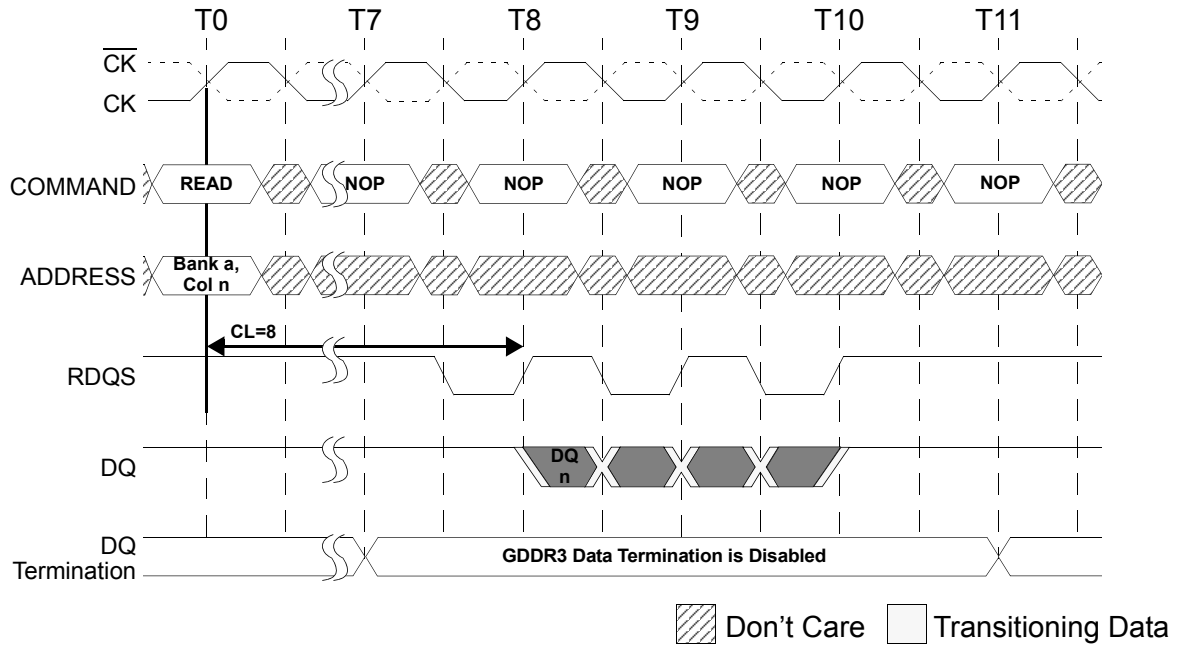
**Low {terminated}**: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VOL(DC).

Corresponding terminologies for ODT Disable Mode are defined below. As mentioned before, ODT Disable Mode is not an intended mode of operation. However, there exist situations where ODT Enable Mode can not be guaranteed for a short period of time, like during power up, yet is indeed an intended mode of operation

**High {unterminated}**: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VDDQ.

**Hi-z {unterminated}**: No driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be undefined, because the bus would be floating.

**Low {unterminated}**: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VSSQ.



## READ Timing

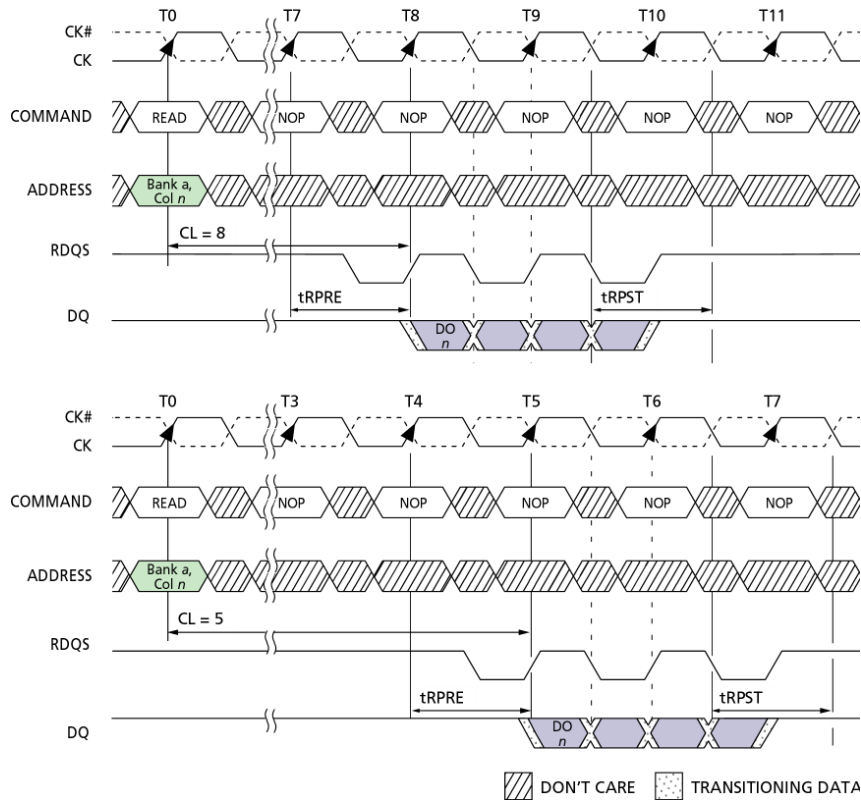
The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after  $t_{RAS}$  min has been met.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edges. The GDDR3 SGRAM drives the output data edge aligned to RDQS. The initial HIGH transitioning LOW of RDQS is known as the read preamble; the half cycle coincident with the last data-out element is known as the read postamble. The GDDR3 devices starts to drive the preamble 1/2 clock cycle prior to the first falling edge of RDQS and continues to drive RDQS until 1/2 clock cycle after the last rising edge of the Postamble. RDQS also can only toggle when there is valid data on the bus.

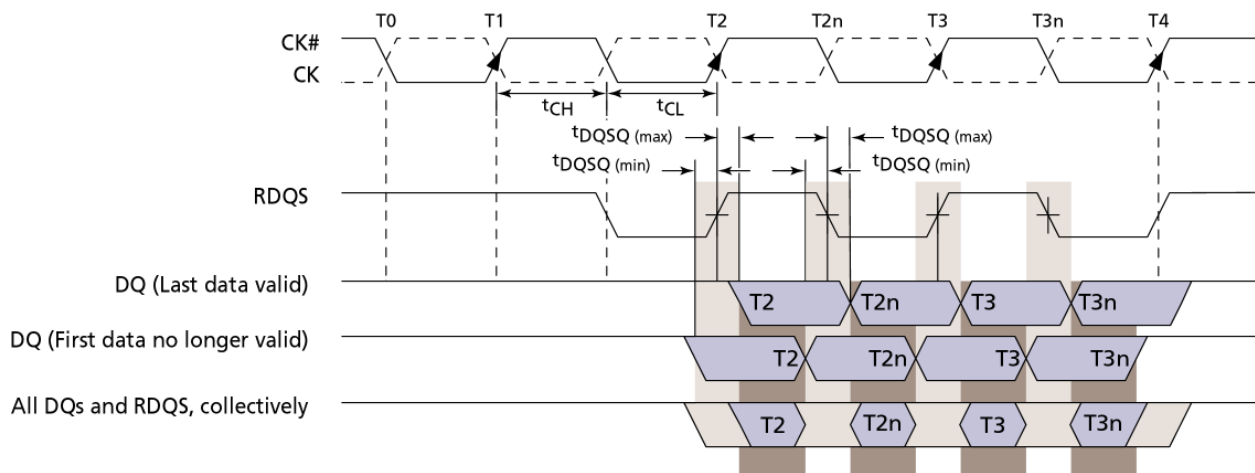
Upon completion of a burst, assuming no other commands have been initiated, the DQs will go to VDD do to the on die termination.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued  $x$  cycles after the first READ command, where  $x$  equals  $2x$  the number of data element nibbles depending on the burst length. READ data cannot be terminated or truncated.

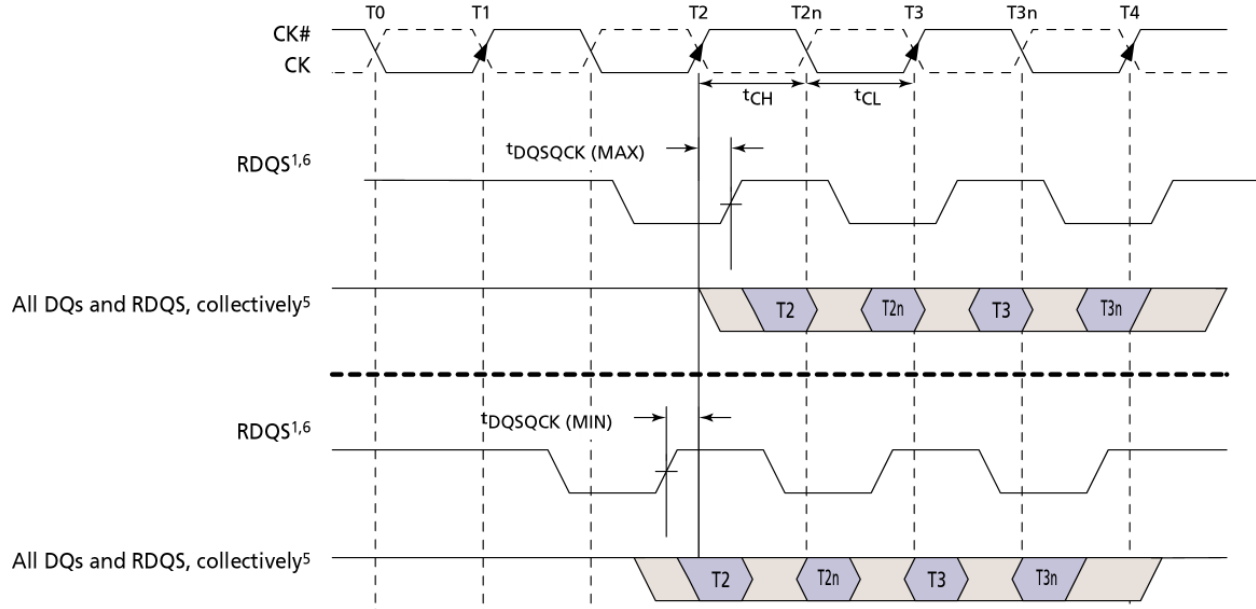
## READ Data



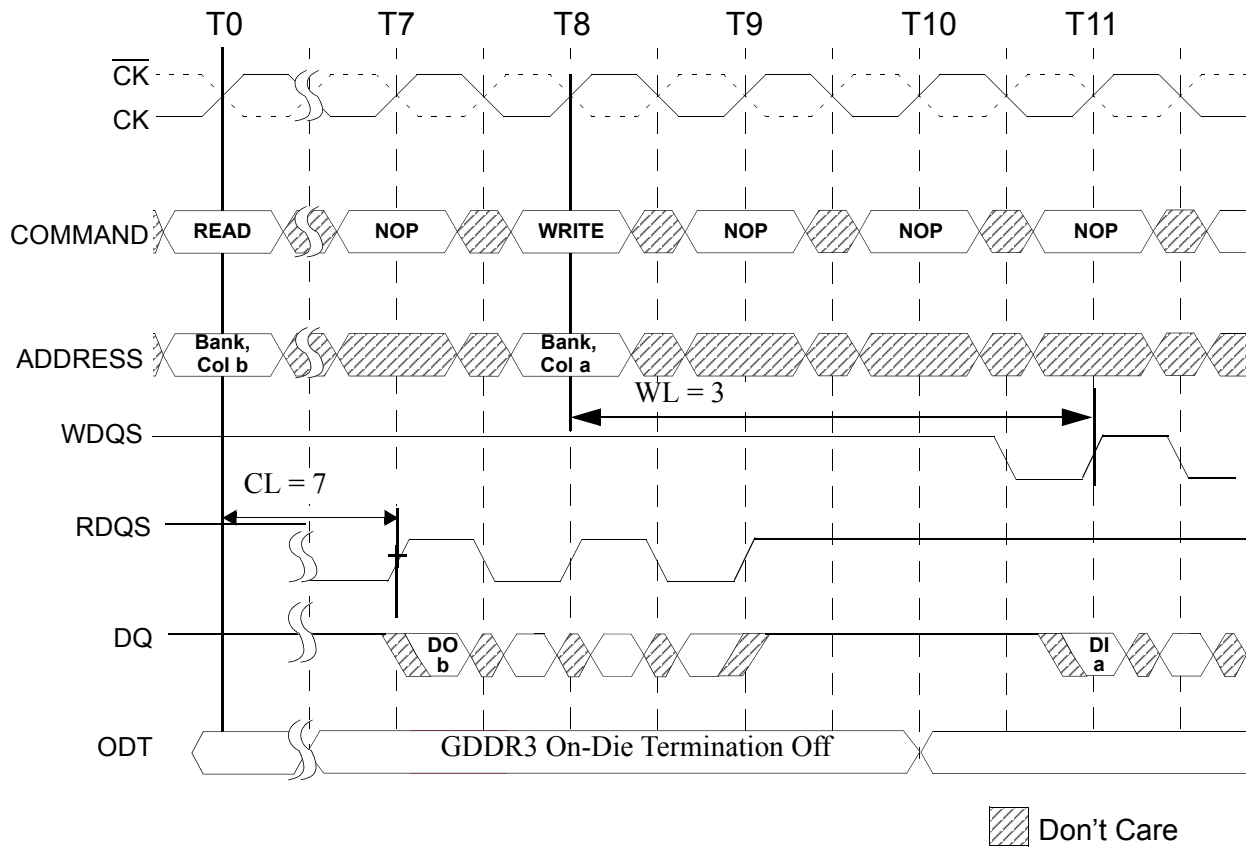
## Byte Lane Timing



Byte Lane to CK/CK#



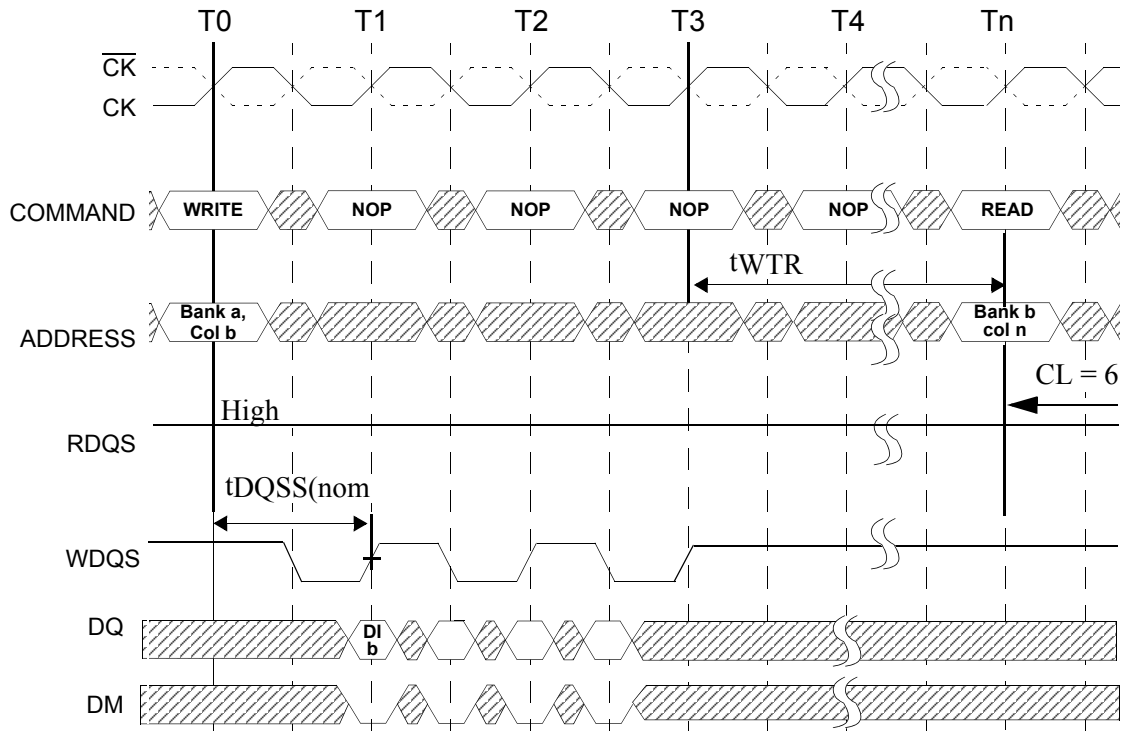
## READ To WRITE




### Notes

1. Write data can not be driven onto the DQ bus for 2 clock cycles after the READ data is off the bus.
2. The timing diagram covers a READ to a WRITE command from different banks on the same part or the same row in the same bank.

## WRITE to READ Timing



 Don't Care

1. DI b = Data In for column b
2. Three subsequent elements of Data In are applied following DI b
3. tWTR is referenced from the first positive CK edge after the last Data In
4. The READ and WRITE commands may be to any bank.
5. WRITE Latency is set to 1.
6. RDQS level is High.

## Mirror Function

The GDDR3 SGRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines, assisting in routing devices back to back. The MF ball will affect RAS#, CAS#, WE#, CS# and CKE on balls H3, F4, H9, F9 and H4 respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0 and BA1 on balls K4, H2, K3, M4, K9, H11, K10, L9, K11, M9, K2, L4, G4 and G9 respectively. MF is LVCMOS input and the MF ball should be tied directly to VSS or VDD depending on the control line orientation desired.

When the MF ball is tied low the ball orientation is as follows, RAS# - H3, CAS# - F4, WE# - H9, CS# - F9, CKE - H4, A0 - K4, A1 - H2, A2 - K3, A3 - M4, A4 - K9, A5 - H11, A6 - K10, A7 - L9, A8 - K11, A9 - M9, A10 - K2, A11 - L4, BA0 - G4 and BA1 - G9. The high condition on the MF ball will change the location of the control balls as follows; CS# - F4, CAS# - F9, RAS# - H10, WE# - H4, CKE - H9, A0 - K9, A1 - H11, A2 - K10, A3 - M9, A4 - K4, A5 - H2, A6 - K3, A7 - L4, A8 - K2, A9 - M4, A10 - K11, A11 - L9, BA0 - G9 and BA1 - G4.

PINS	MF Logic State	
	HIGH	LOW
RAS#	H10	H3
CAS#	F9	F4
WE#	H4	H9
CS#	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

## IO and ODT Drive Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners

1. Nominal 1.8V (VDD/VDDQ)
2. Power the GDDR3 device and calibrate the output drivers and termination to eliminate process variation at 25°C
3. Reduce temperature to 10°C recalibrate.
4. Reduce temperature to 0°C and take the fast corner measurement.
5. Raise temperature to 75°C and recalibrate
6. Raise temperature to 85°C and take the slow corner measurement

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN	MAX
0.1	2.144	3.366
0.2	4.268	6.516
0.3	6.373	9.454
0.4	8.449	12.185
0.5	10.505	14.715
0.6	12.542	17.051
0.7	14.540	19.400
0.8	16.509	21.828
0.9	18.449	24.219
1.0	20.341	26.580
1.1	22.203	28.913
1.2	24.017	31.222
1.3	25.783	33.508
1.4	27.480	35.813
1.5	29.119	38.213
1.6	30.671	40.551
1.7	31.387	42.900
1.8	31.648	45.176

Pull-Up Characteristic at 40ohms		
Voltage (V)	MIN	MAX
0.1	-2.377	-2.946
0.2	-4.705	-5.829
0.3	-6.984	-8.644
0.4	-9.283	-11.383
0.5	-11.524	-14.038
0.6	-13.803	-16.599
0.7	-16.015	-19.051
0.8	-18.285	-21.630
0.9	-20.302	-24.143
1.0	-22.223	-26.605
1.1	-24.066	-29.005
1.2	-25.773	-31.353
1.3	-27.344	-33.619
1.4	-28.683	-35.803
1.5	-29.731	-37.883
1.6	-30.691	-39.882
1.7	-31.544	-42.003
1.8	-32.311	-44.063

On Die termination Values

Pull-Up Characteristic at 60ohms		
Voltage (V)	MIN	MAX
0.1	-1.58	-1.96
0.2	-3.14	-3.89
0.3	-4.66	-5.76
0.4	-6.19	-7.59
0.5	-7.68	-9.36
0.6	-9.20	-11.07
0.7	-10.68	-12.70
0.8	-12.19	-14.42
0.9	-13.53	-16.10
1.0	-14.82	-17.74
1.1	-16.04	-19.34
1.2	-17.18	-20.90
1.3	-18.23	-22.41
1.4	-19.12	-23.87
1.5	-19.82	-25.26
1.6	-20.46	-26.59
1.7	-21.03	-28.00
1.8	-21.54	-29.38

Pull-Up Characteristic at 120ohms		
Voltage (V)	MIN	MAX
0.1	-0.79	-0.98
0.2	-1.57	-1.94
0.3	-2.33	-2.88
0.4	-3.09	-3.79
0.5	-3.84	-4.68
0.6	-4.60	-5.53
0.7	-5.34	-6.35
0.8	-6.09	-7.21
0.9	-6.77	-8.05
1.0	-7.41	-8.87
1.1	-8.02	-9.67
1.2	-8.59	-10.45
1.3	-9.11	-11.21
1.4	-9.56	-11.93
1.5	-9.91	-12.63
1.6	-10.23	-13.29
1.7	-10.51	-14.00
1.8	-10.77	-14.69

Pull-Up Characteristic at 240ohms		
Voltage (V)	MIN	MAX
0.1	-0.40	-0.49
0.2	-0.78	-0.97
0.3	-1.16	-1.44
0.4	-1.55	-1.90
0.5	-1.92	-2.34
0.6	-2.30	-2.77
0.7	-2.67	-3.18
0.8	-3.05	-3.60
0.9	-3.38	-4.02
1.0	-3.70	-4.43
1.1	-4.01	-4.83
1.2	-4.30	-5.23
1.3	-4.56	-5.60
1.4	-4.78	-5.97
1.5	-4.96	-6.31
1.6	-5.12	-6.65
1.7	-5.26	-7.00
1.8	-5.39	-7.34

## GDDR SGRAM Boundary Scan

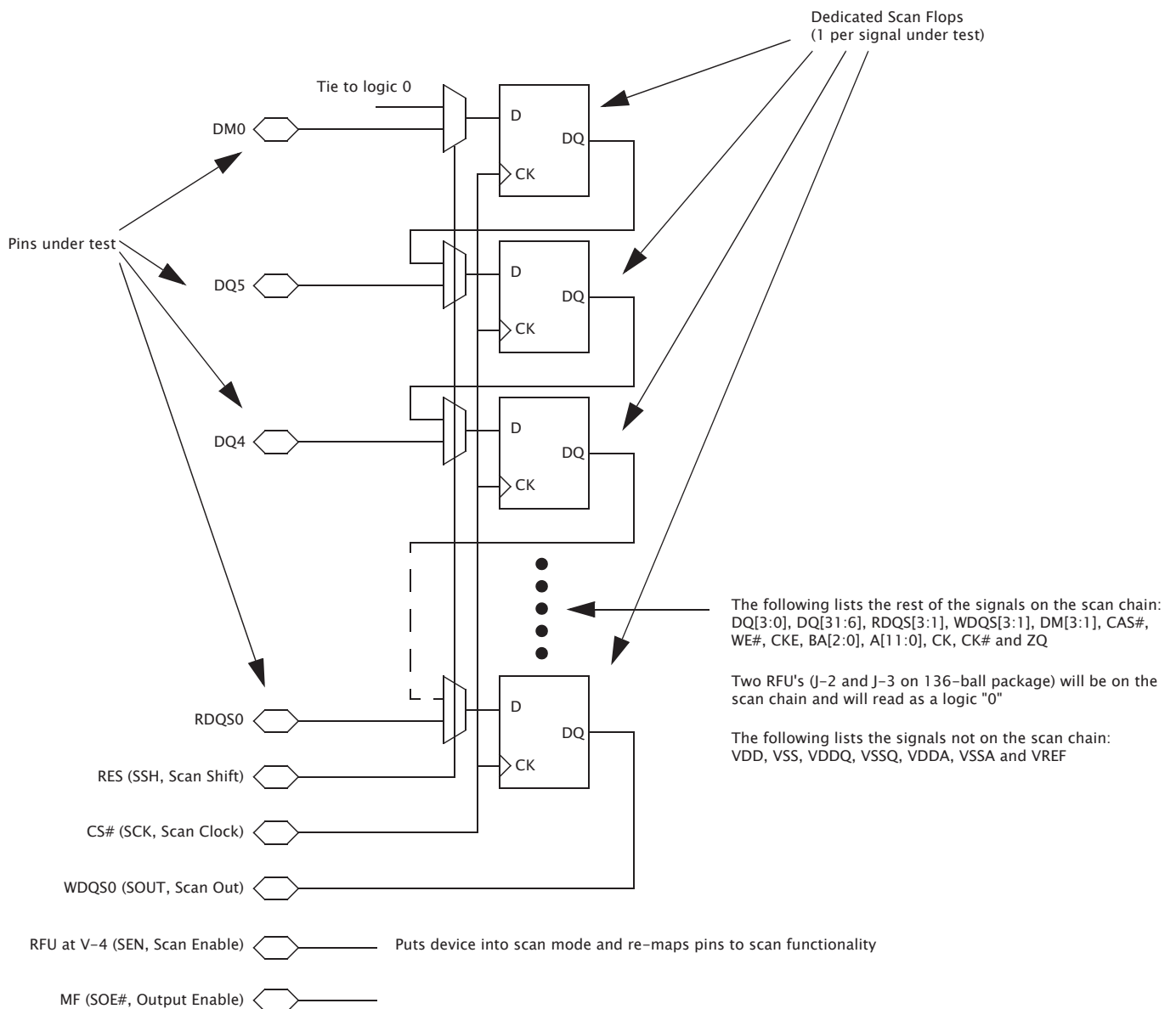
### GENERAL INFORMATION

The 512Mb GDDR3 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.1-1990. To save the current GDDR3 ball-out, this mode will scan the parallel data input and output the scanned data through WDQS0 pin controlled by an add-on pin, SEN which is located at V-4 of 136 ball package.

### DISABLING THE SCAN FEATURE

It is possible to operate the 512Mb GDDR3 without using the boundary scan feature. SEN(at V-4 of 136-ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RES, MF, WDQS0 and CS# will be operating at normal GDDR3 functionalities when SEN is deasserted.

**Figure 1 . Internal Block Diagram (Reference Only)**



**Table 1. Boundary Scan (Exit) Order**

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-11	37	R-10	49	L-3	61	G-4
2	C-2	14	F-10	26	K-10	38	T-11	50	M-2	62	F-4
3	C-3	15	E-11	27	K-9	39	T-10	51	M-4	63	F-2
4	B-2	16	G-10	28	M-9	40	T-3	52	K-4	64	G-3
5	B-3	17	F-11	29	M-11	41	T-2	53	K-3	65	E-2
6	A-4	18	G-9	30	L-10	42	R-3	54	K-2	66	F-3
7	B-10	19	H-9	31	N-11	43	R-2	55	L-4	67	E-3
8	B-11	20	H-10	32	M-10	44	P-3	56	J-3		
9	C-10	21	H-11	33	N-10	45	P-2	57	J-2		
10	C-11	22	J-11	34	P-11	46	N-3	58	H-2		
11	D-10	23	J-10	35	P-10	47	M-3	59	H-3		
12	D-11	24	L-9	36	R-11	48	N-2	60	H-4		

\* Note:

1. When the device is in scan mode, the mirror function will be disabled and none of the pins are remapped.
2. Since the other input of the MUX for DM0 tied to GND, the device will output the continuous zeros after scanning a bit #67, if the chip stays in scan shift mode.
3. Two RFU balls (#56 and #57) in the scan order, will read as a logic“0”.

**Table 2. Scan Pin Description**

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
V-9	SSH	RES	Input	Scan Shift. Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	CS#	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock.
D-2	SOUT	WDQS0	Output	Scan Output.
V-4	SEN	RFU	Input	Scan Enable. Logic HIGH would enable the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	SOE#	MF	Input	Scan Output Enable. Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1K $\Omega$ ) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

\* Note:

1. When SEN is asserted, no commands are to be executed by the GDDR3. This applies both to user commands and manufacturing commands which may exist while RES is deasserted.
2. All scan functionalities are valid only after the appropriate power-up and initialization sequence. (RES and CKE, to set the ODT of the C/A)
3. In a double-load clam-shell configuration, SEN will be asserted to both devices. Separate two SOE#’s should be provided to top and bottom devices to access the scanned output. When either of the devices is in scan mode, SOE# for the other device which is not in a scan will be disabled.

Table 3. Scan DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	-	V	1, 2
Input Low (Logic 0) Voltage	$V_{IL}(DC)$	-	$V_{REF}-0.15$	V	1, 2

\* Note: 1. The parameter applies only when SEN is asserted.  
 2. All voltages referenced to GND.

Figure 2 . Scan Capture Timing

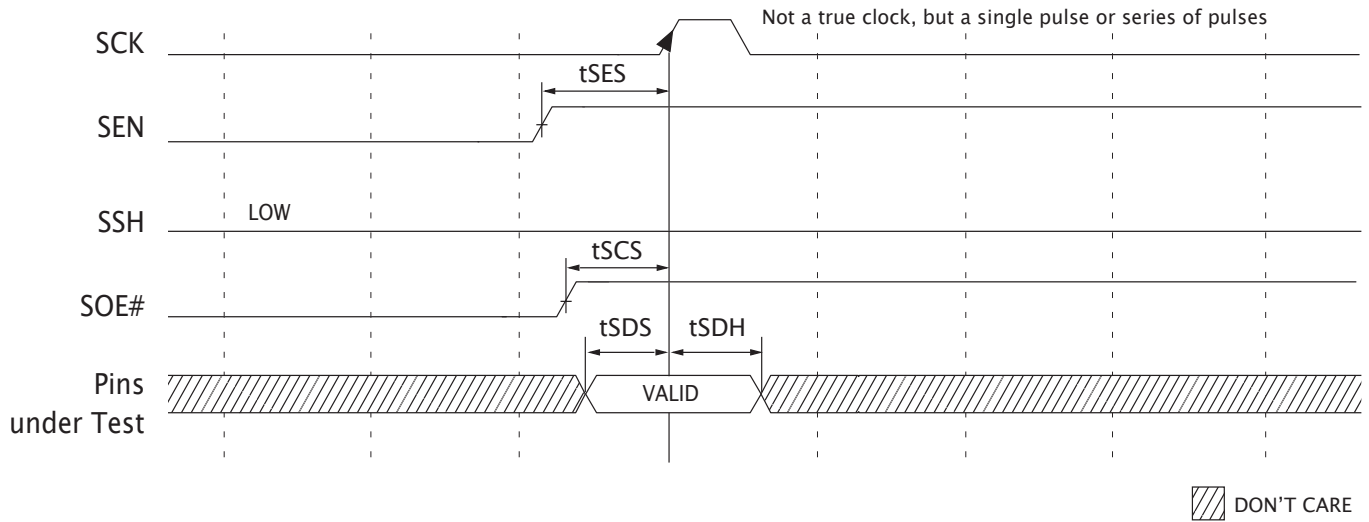


Figure 3 . Scan Shift Timing

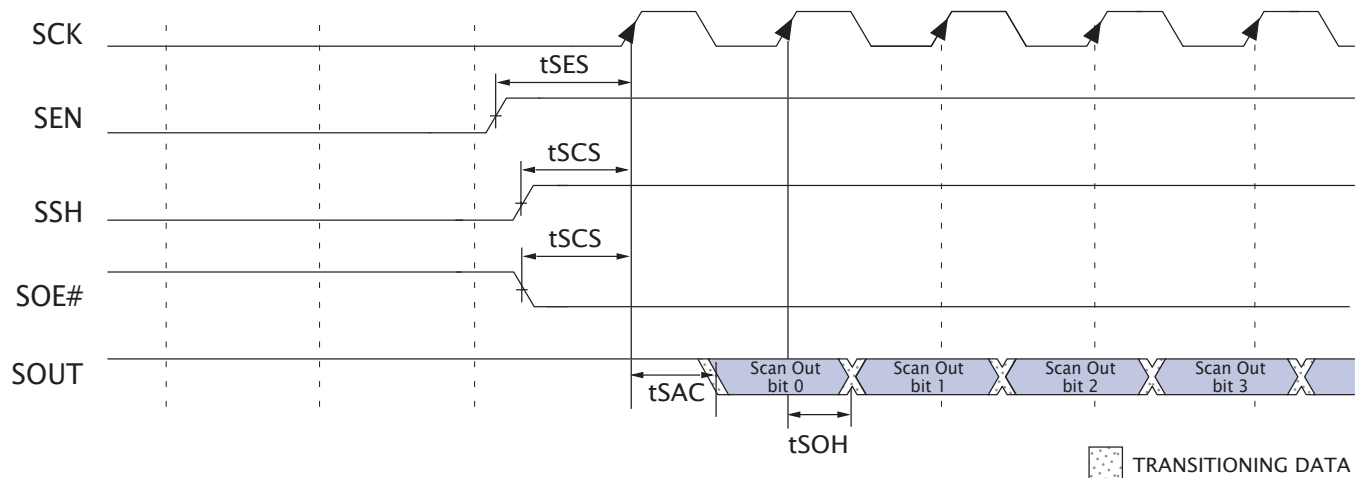
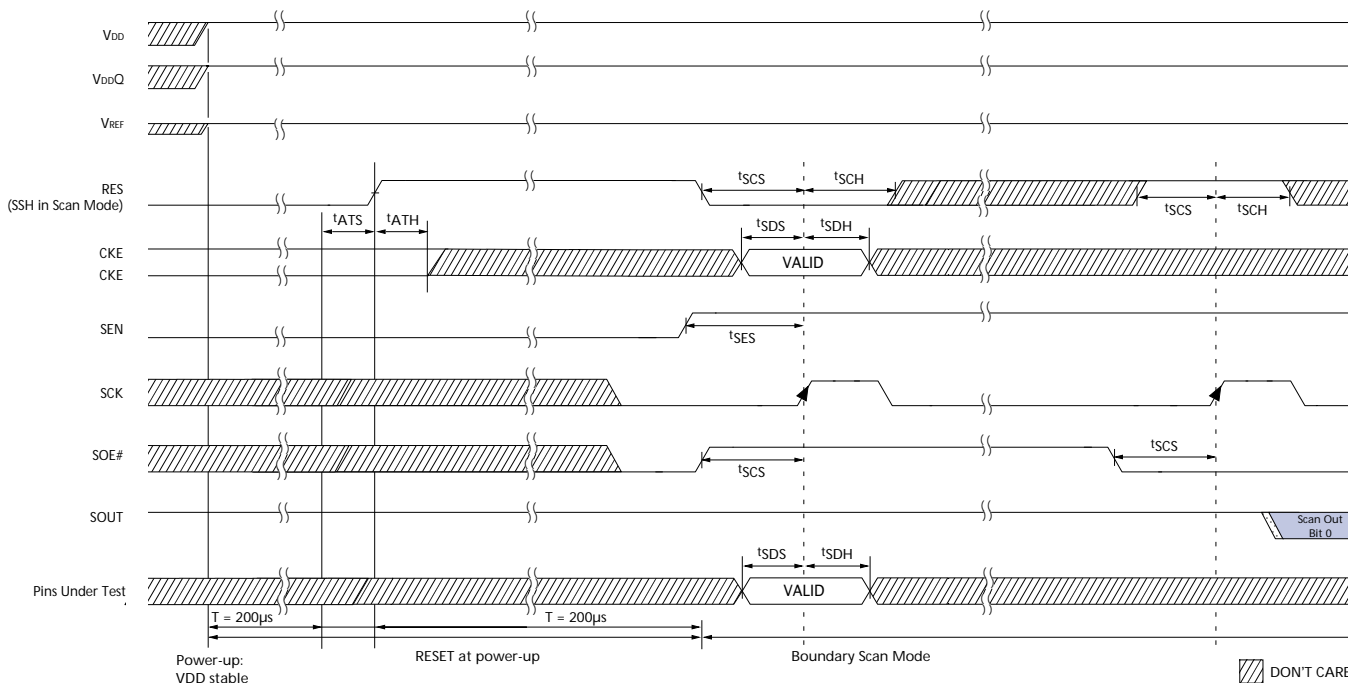


Table 4. Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
<b>Clock</b>					
Clock cycle time	tSCK	40	-	ns	1
<b>Scan Command Time</b>					
Scan enable setup time	tSES	20	-	ns	1, 2
Scan enable hold time	tSEH	20	-	ns	1
Scan command setup time for SSH, SOE# and SOUT	tSCS	14	-	ns	1
Scan command hold time for SSH, SOE# and SOUT	tSCH	14	-	ns	1
<b>Scan Capture Time</b>					
Scan capture setup time	tSDS	10	-	ns	1
Scan capture hold time	tSDH	20	-	ns	1
<b>Scan Shift Time</b>					
Scan clock to valid scan output	tSAC	-	10	ns	1
Scan clock to scan output hold	tSOH	1.5	-	ns	1

\* Note: 1. The parameter applies only when SEN is asserted.  
2. Scan Enable should be issued 10ns before any other Scan Commands.

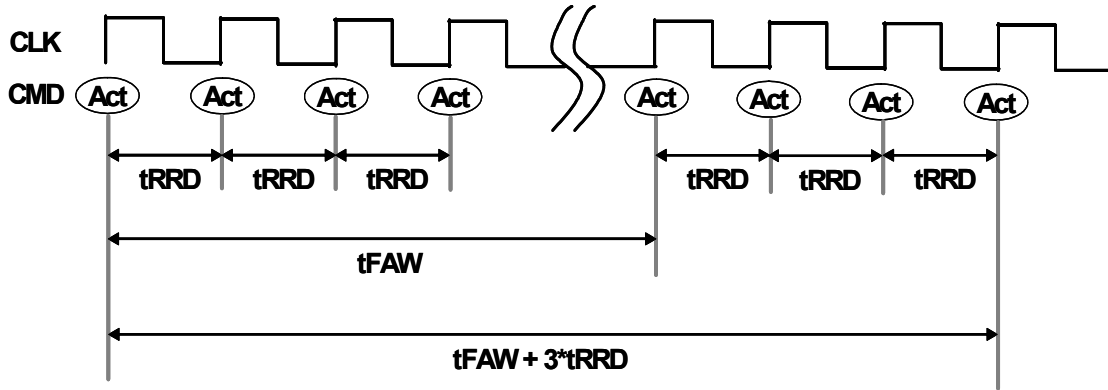
Figure 4 . Scan Initialization Sequence



Note : To set the pre-defined ODT for C/A, a boundary scan mode should be issued after an appropriate ODT initialization sequence with RES and CKE signals

### GDDR3 SGRAM tFAW Definition

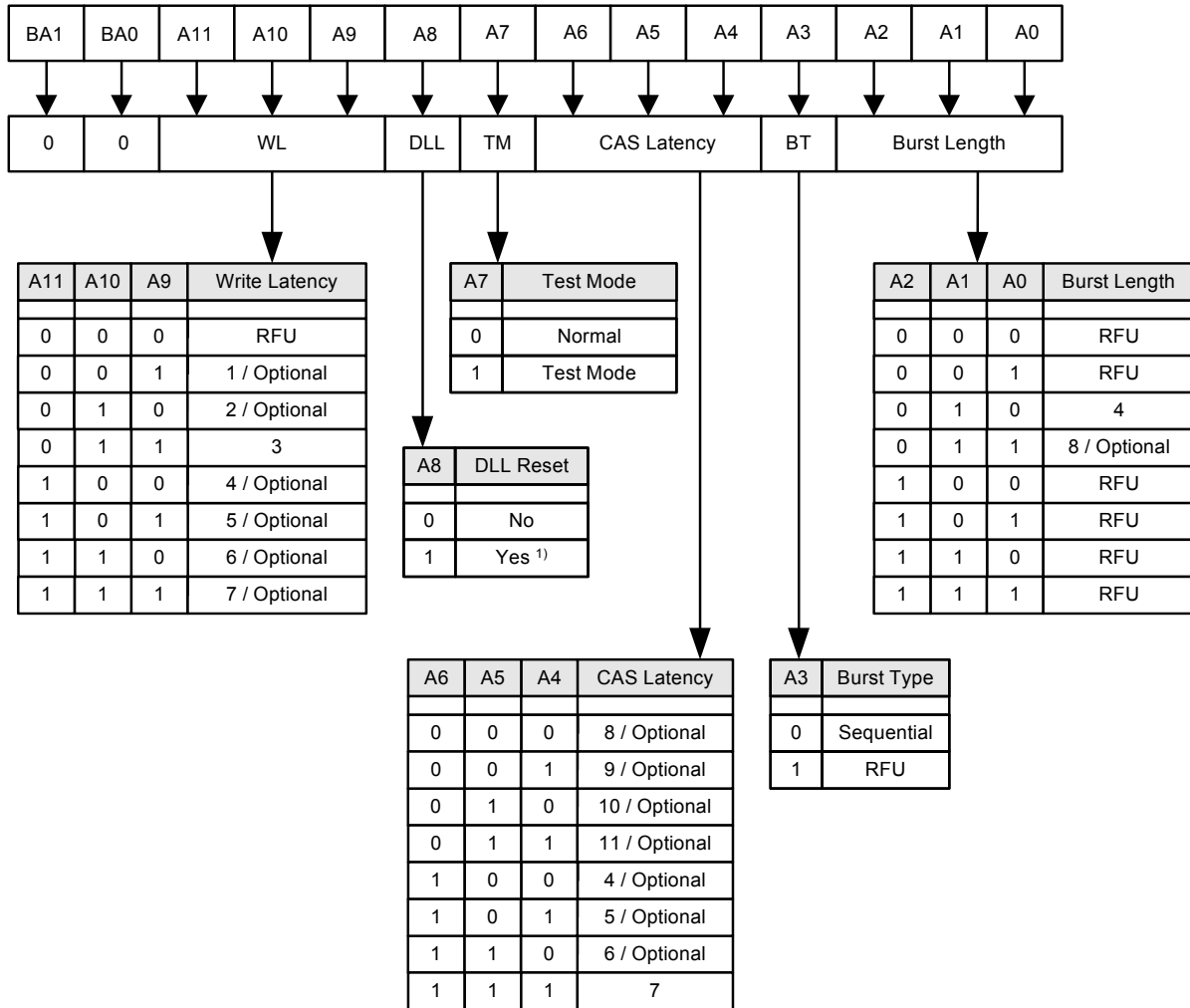
8 bank device Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW(ns) by tCK(ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clocks N+1 through N+9.



### AC Timing

tFAW = xx ns

# GDDR3 Graphics RAM Mode Register



Note: 1) The DLL reset command is self-clearing