

### 3.10.2 Byte Wide MPDRAM



### 3.10.2.1 – 128K AND 256K BY 8 MPDRAM IN DIP, SOJ, & TSOP2

CAPACITY—128K, & 256K WORDS OF 8 BITS

LOGIC FEATURES—Multiplexed Address

—SERIAL and RAM data ports

The 128K part has two versions: in DIP, and SOJ

PACKAGE—128K PART, 40 PIN DIP, 0.600" WIDE

PIN ASSIGNMENTS—FIG. 3.10.2-1

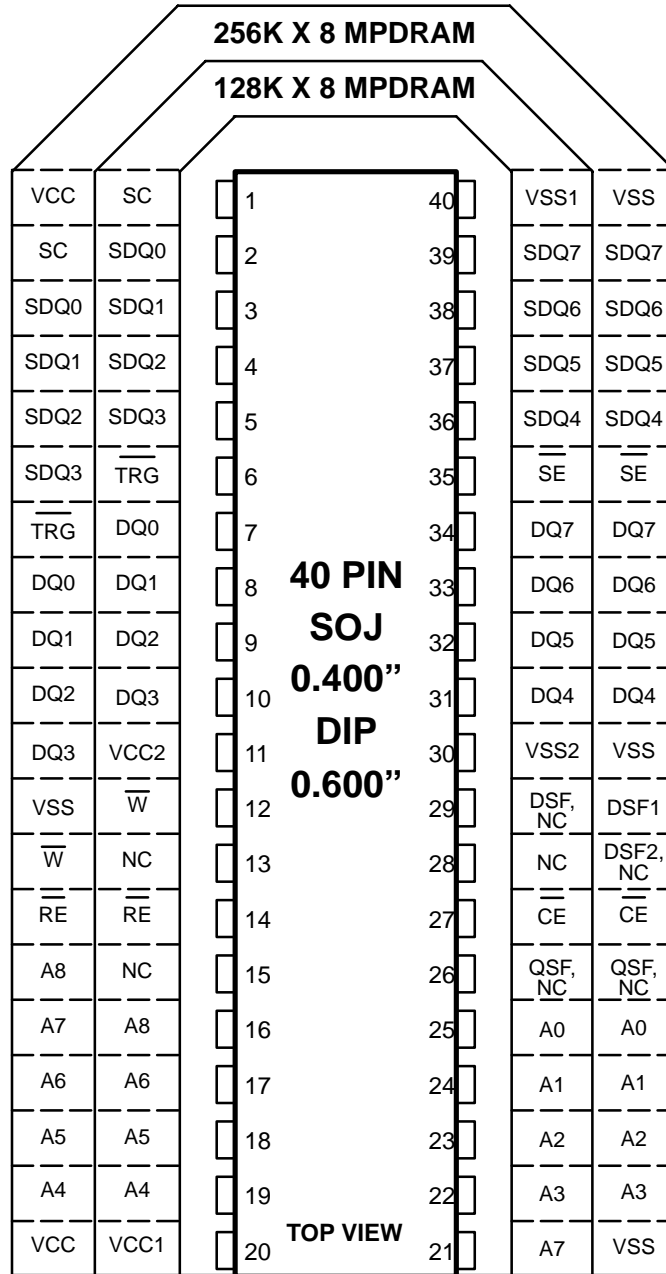
PACKAGE—128K & 256K PARTS, 40 PIN SOJ, 0.400" WIDE

PIN ASSIGNMENTS—FIG. 3.10.2-1

PACKAGE—128K PART, 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH

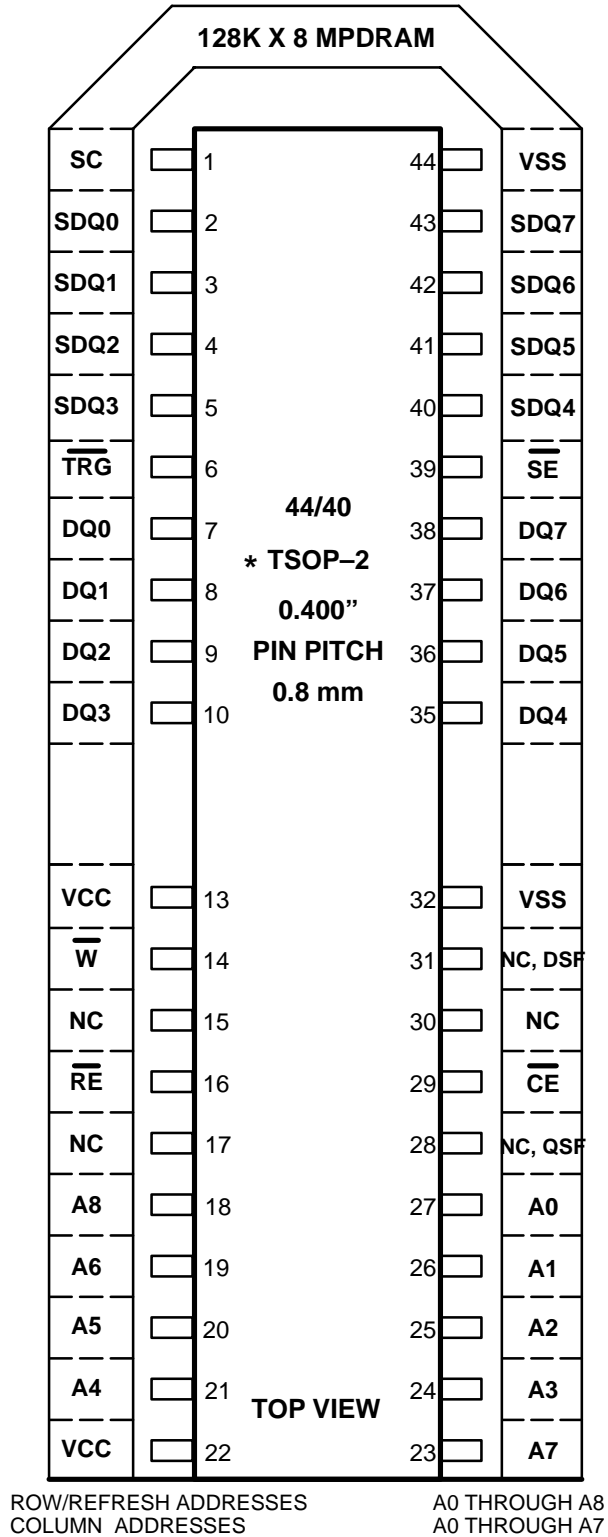
PIN ASSIGNMENTS—FIG. 3.10.2-2





REFRESH ADDRESS FIELD = A0 THROUGH A8

**FIGURE 3.10.2-1**  
**128K AND 256K BY 8 MPDRAM IN DIP & SOJ**



\* Note: The JEDEC Standard 30 term for the TSOP-2 package is PDSO-G

**FIGURE 3.10.2-2**  
**128K BY 8 MPDRAM IN TSOP2**