3.9.5 DRAM Optional Features

3.9.5.1 - OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM

The definitions for serial data access, bit write, and refresh control included in Release 1 of this standard have been replaced by the more general definitions of Optional Operational Modes and Cycles beginning on page 3.9.5-11

3.9.5.2 - 1M DRAM BUILT IN TEST FUNCTION

An approved option for 1M DRAM (1M X 1 or 256K X 4) is the inclusion of a built in manufacturer defined "Test Mode". This mode is enabled using a dedicated pin which is optional NC or TF. When the optional mode is implemented, the manufacturer should include notes on his data sheet as follows:

(A) Normal operation requires the "TF" pin be connected to a VSS or logic low level or left unconnected.

(B) When the "TF" pin is connected to the manufacturer defined positive voltage, the internal test mode will be actuated. Contact the manufacturer for specific operational details of the Test Mode.

3.9.5.3 - ON-CHIP REFRESH CONTROL FOR X8 DRAM

This standard describes an optional feature that is applicable to the non-address multiplexed byte wide dynamic RAMs described in this publication. The standard establishes the clock timing sequence needed to invoke an on-chip refresh feature.

3.9.5.4 - $\overline{G}$ BEFORE $\overline{E}$ REFRESH

If G is low when E falls, a refresh cycle is executed. During this type of refresh cycle, an internal counter/register provides the refresh address and the external address is ignored

3.9.5.5 - DRAM SPECIAL TEST AND OPERATIONAL MODES

This standard defines a scheme for controlling a series of special operational modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control and exit from the special modes. In addition, it defines a basic test mode plus a series of other special test and operational modes. The details of this standard are given on pages 3.9.5-7 through 3.9.5-10.

3.9.5.6 - NON-MULTIPLEXED DRAM OPERATION

This standard defines multiple aspects of the address and clock relationships for DRAMs that have a non-multiplexed address architecture. It also defines the relationships between the address bits of multiplexed and non-multiplexed devices. The details of the standard are given on page 3.9.5-13

3.9.5.7 - DRAM EXTENDED DATA OUT

This standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating "EDO" must satisfy all of the following criteria to conform to the Standard. The details of the EDO standard are given on P 3.9.5-14

3.9.5.8 - 256M DRAM TEST MODE DATA AND ADDRESS COMPRESSION

This standard defines the algorithms for data and address compression when 256M DRAMs are operated in the built in special test mode. The detaild of the Compression standard are given on P 3.9.5-15

3.9.5.9 - PIPELINED NIBBLE MODE DEFINITION

This standard defines the output characteristics of the Pipelined Nibble Mode feature for DRAMs. Any part encorporating Pipelined Nibble Mode must satisfy all of the following criteria to conform to the Standard. The details of the standard are given on P 3.9.5-16

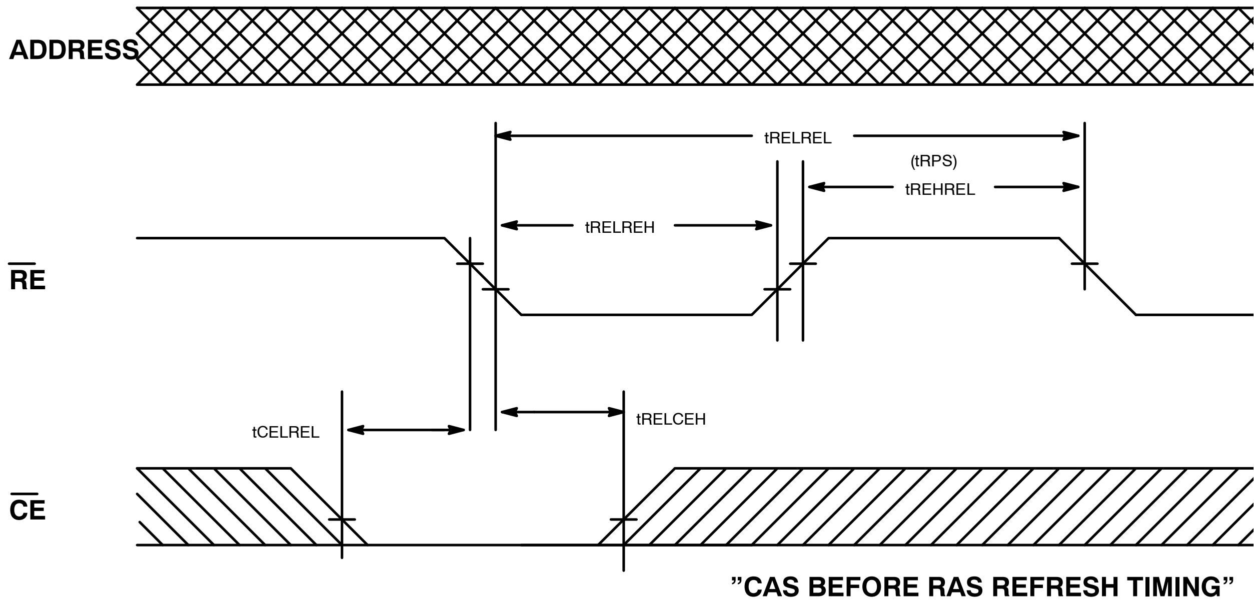
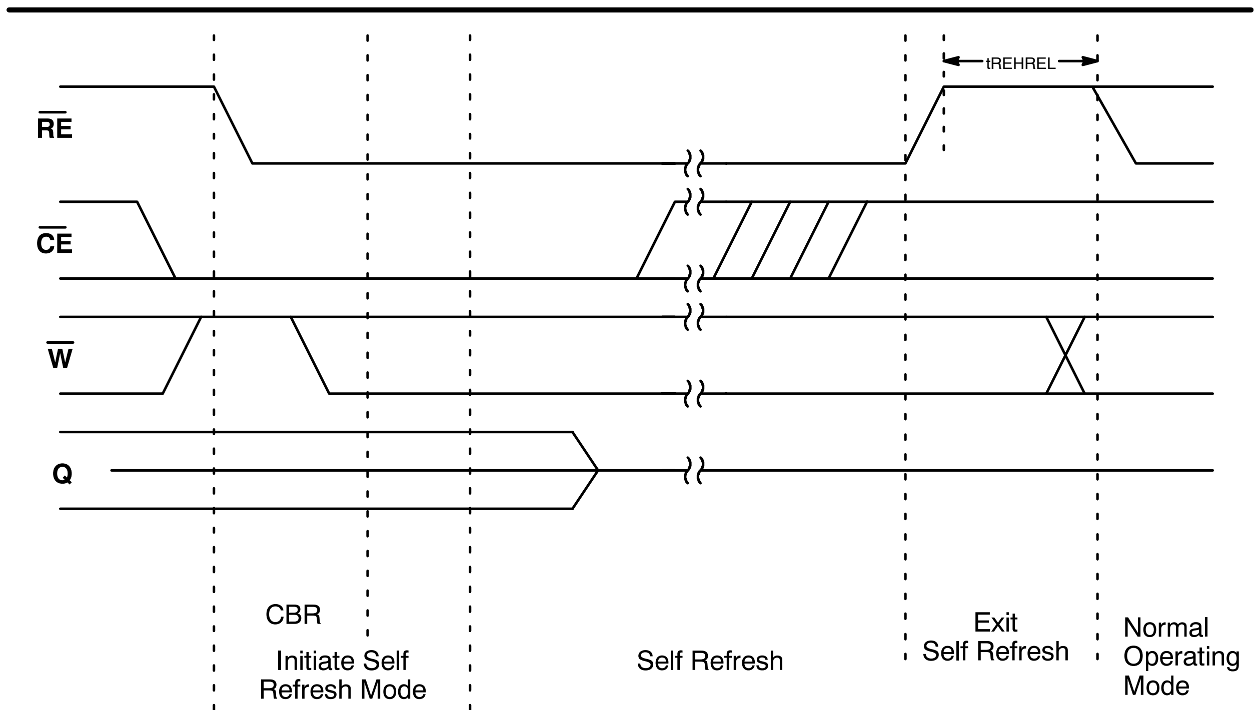


FIGURE 3.9.5-1A
DRAM ON CHIP REFRESH TIMING



Data Out may be either Tristate or Active depending on the state of CE\ when the cycle is entered.

FIGURE 3.9.5-1 B
DRAM SELF REFRESH MODE TIMING

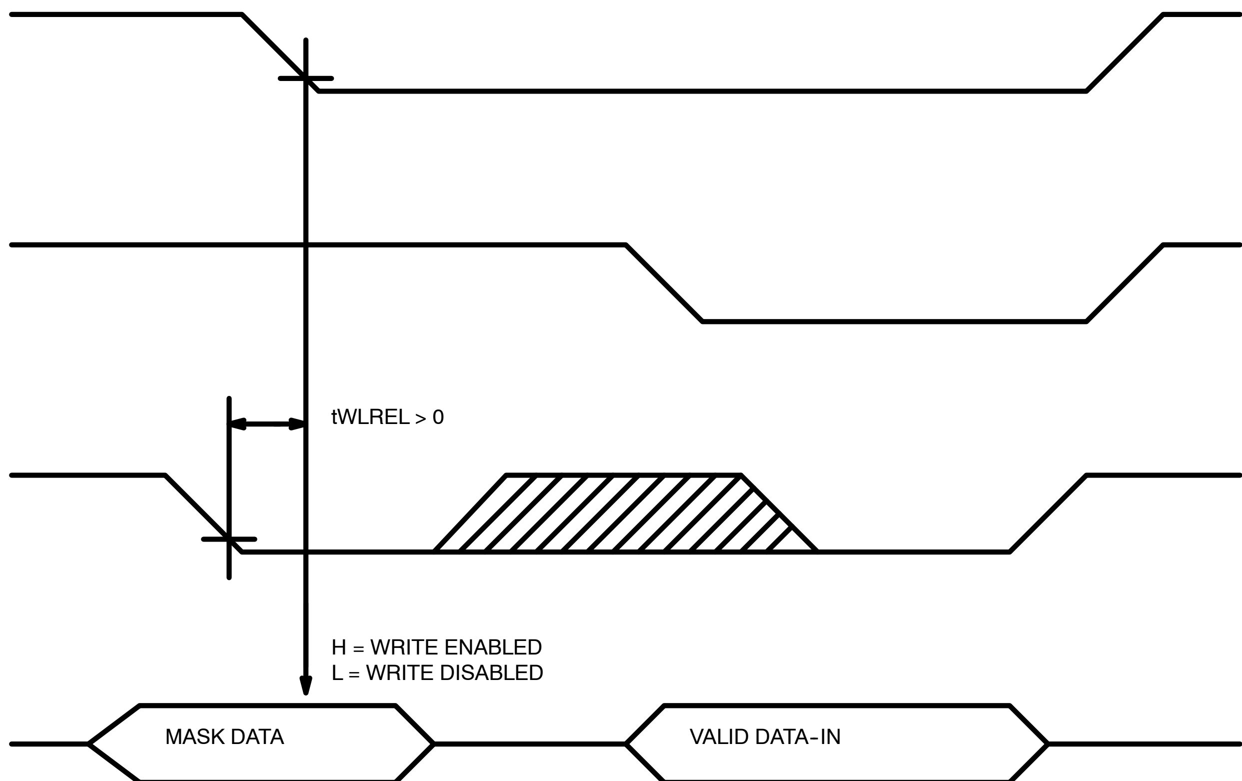


FIGURE 3.9.5-2
DRAM BIT WRITE TIMING

DRAM SPECIAL TEST AND OPERATIONAL MODES

1 PURPOSE

This standard defines a scheme for controlling a series of special modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control, and exit from the special modes. In addition, it defines a basic special test mode plus a series of other special test and operational modes.

2 SPECIAL MODE INITIATE

The special modes will be initiated by the W\ AND CE\ BEFORE RE\ clock sequence shown in Fig.A2-1. This sequence is called "Write Enable and CAS before RAS" or "WCBR". When this clock sequence is generated, the state of the 8 low order Row Address bits (address key) will define the mode to be selected (see Par. 4) if optional modes are implemented. This mode will be latched and remain in effect until a special release cycle is generated or a new initiate cycle defining some other special mode is generated.

Following the initiate cycle, all subsequent cycles except refresh cycles (see pars. 3 & 5), will be operating cycles as allowed by the special mode selected.

3 MODE EXIT

A special mode will be cleared and the memory device returned to its normal operational state by the application of any normal REFRESH cycle, "RAS only refresh", (ROR) or "CAS before RAS refresh" (CBRR).

4 MODE SELECTION

Devices meeting this standard must have an implementation of the BASIC TEST MODE (see par 6) but also may contain other modes as options. When optional special modes are implemented, they will be selected by the state of the 8 least significant ROW Address bits at the time that INITIATE clock sequence is provided. The address space for the mode selection is defined as follows.

The special modes as selected by the 8-bit Address Key will be partitioned into four (4) subsets as follows:

1 - JEDEC Registered Modes

2 - Reserved for future expansion

3 - Vendor Specific Modes

4 - Customer Specific Modes

4.1 MODE PARTITIONING

These modes and their partitioning will be as diagrammed in Table A2-2. Additional address bits above A7 can be used to select additional pages of MODE definition (see par.4.3). Mode subgroups 1 and 2 will be further subdivided into "Test" and "Operational" modes as follows:

TEST MODES are those that implement some special test or measurement function or algorithm designed to enhance the ability of the Vendor or User to determine the integrity of, or to characterize, the part.

OPERATIONAL MODES are those that alter the operational characteristics of the part but do not interfere with its function as a storage device and are intended to be used in system operation.

4.2 MODE CHANGES

The special mode can be changed at any time by the application of a mode initiate clock sequence with the appropriate address key to define the new mode.

4.3 ADDITIONAL MODES

The additional address bits above A7 can be used as needed to define additional pages of MODE definitions.

5 JEDEC REGISTERED SPECIAL MODE REFRESH

-Refresh can be performed while in a special mode by the following means.

(1) - An initiate cycle is generated (W\ and CE\ before RE\) with the address key used to select the mode currently in effect.
(2) - Any normal read or write cycle will perform REFRESH.

-The Initiate Special Mode clock sequence will always perform an on-chip refresh cycle even when the MODE is being changed.

-This refresh applies to JEDEC Special Registered Modes only

6 BASIC TEST MODE DATA ALGORITHM

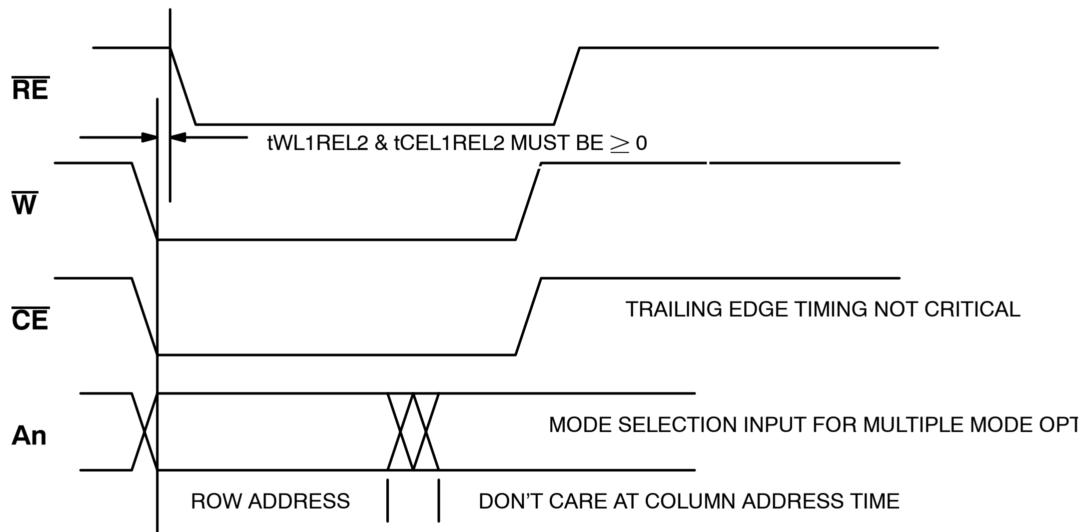
Any memory device that implements the JEDEC Registered modes must implement the “Basic Test Mode” as a minimum. Any other of the special modes which are registered and listed in Table A2-3, may be implemented at the option of the manufacturer. Additional MODES and test algorithms may be registered as needed.

When a memory device is operating in the Basic Test Mode, data that are presented to be written into the memory will be written into multiple locations depending upon the internal device organization and the number of parallel bits in the internal data bus (4, 8, 16, or other) (see par. 7). When a Read Operation is done, the data recovered will include the same set of data bits on the parallel data bus. The internal logic of the memory device will compare the states of all bits of the internal data bus. If all internal bits are equal, the “Q” pin will take the state equal to “1”. If any internal data bits are not equal , then “Q” will equal “0”. This is called the “1/0/=” test algorithm.

The BASIC TEST MODE is assigned the address keys, “All 1’s” and all subsets of this key from 2 low order 1’s to all 1’s (see Appendix 2). It is acceptable for a device which implements the BASIC TEST MODE and optional test modes to sense a low order subset of the key address field but it is recomended that at least 3 bits be used to minimize the chances of ambiguities in the mode selection.

7 ADDRESS SPACE COMPRESSION CONTROL

Any Standard or Registered test algorithm in which the address space of the device is compressed by test operations on multiple internal data bits will have the address bits which control the internal data bits as defined in Table A2-1. In any test operations, the state of these bits will be “don’t care”.



FIG

A2-1 SPECIAL OPERATIONAL MODE INITIATE CYCLE

NOTE: The timing parameters of the pulses are not specified in this standard but care must be taken in the device specification to define minimum and maximum pulse durations to insure that noise pulses will be rejected and that intentional control sequencies will be recognized.

Table A2-1-A, 1M TO 16M DRAM ADDRESS COMPRESSION CONTROL BITS

Data Bus Width (# bits)	Control Address Bits	
	X1 DATA INTERFACE	X4 DATA INTERFACE
2		CA0
4	RA(MSB), CA(MSB)	CA0, CA1
8	RA(MSB), CA(MSB), CA0	
16	RA(MSB), CA(MSB), CA0, CA1	(MSB = Most Significant Bit)

Table A2-1-B 64M DRAM ADDRESS COMPRESSION CONTROL BITS

Compression Address = CA(MSB), CA(MSB-1), ...,CA(MSB-n)
where 2n-1 = the number of internal parallel data test bits = Compression factor

PARALLEL TEST BITS	64M X 1	16M X 4	8M X 8	4M X 16
32(n=4)	CA12>CA8			
8(n=2)		CA10>CA8		
4(n=1)			CA10>CA9(4K)	
2(n=0)				CA9(4K)

TABLE A2-1-C 64M DRAM ADDRESS ASSIGNMENT TABLE

Test Bits	DEVICE	RFSH CYCLES	Address Assignments												
32	64M X 1	-													
32	64M X 1	8K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / (8)	9 / (9)	10 / (10)	11 / (11)	12 / (12)
8	16M X 4	-													
8	16M X 4	8K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / (8)	9 / (9)	10 / (10)	11	12
4	8M X 8	4K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / 8	9 / (9)	10 / (10)	11	12
4	8M X 8	8K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / (8)	9 / (9)	10	11	12
2	4M X 16	4K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / 8	9 / (9)	10	11	12
2	4M X 16	8K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8 / (8)	9	10	11	12
1	2M X 32	4K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7 / 7	8	9	10	11	12
1	2M X 32	8K	0 / 0	1 / 1	2 / 2	3 / 3	4 / 4	5 / 5	6 / 6	7	8	9	10	11	12

These addresses can be used as common addresses for 64M X 1, 16M X 4, 8M X 8, & 16M X 32 devices

(n) = compression address
n / n = RAn/CAn

TABLE A2-2 SPECIAL MODE ADDRESS KEY SPACE

The SPECIAL MODE Address Key space will be as shown in the following Karnaugh map with the exception of those codes reserved for the BASIC TEST MODE:

		$\overline{A7}$	A7	
$\overline{A6}$	$\overline{A5}$	JEDEC Registered Modes	Reserved for Expansion	TEST
	A5			OPERATION
A6	$\overline{A5}$	Vendor Specific Modes	Customer Specific Modes	
	A5			

A0 - A4 define individual modes within a block

JEDEC REGISTERED MODES - These are the modes that are defined in detail in registration documents. The function(s) shall be performed as defined with no variations (see Appendix 2 for list of registered modes).

VENDOR SPECIFIC MODES - These are those modes that are implemented by a Vendor for his own in-house use. The details will be revealed only at the discretion of the Vendor. The code assignments will have no standardization from vendor to vendor except at their discretion.

CUSTOMER SPECIFIC MODES - These modes are implemented by a vendor at the request of a specific customer. The information on these modes is not revealed except at their discretion.

TABLE A2-3

REGISTERED MODE ASSIGNMENT PAGE 0 TABLE

ROW ADDRESS BIT	FUNCTION
7, 6, 5, 4, 3, 2, 1, 0	
0, 0, 0, 0, 0, 0, 0, 0	NOT ASSIGNED
0, 0, 0, 0, 0, 0, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 0, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 0, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 0, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
0, 0, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 0, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=
* 1, 1, 1, 1, 1, 1, 1, 1	BASIC TEST MODE, 1/0/=

Additional address bits above A7 can be used to select additional pages of MODE definition.

* It should be noted that these pre-assigned address codes do not fall into the address space assigned to JEDEC Registered Modes.

NOTE:: A table of registered optional modes along with definitions will be compiled by the Committee and published periodically.

OPTIONAL DRAM OPERATIONAL MODES AND CYCLES

This standard defines a series of optional serial and random READ, WRITE, and REFRESH operational modes for address multiplexed DRAMs.

1 RANDOM ACCESS MODES

The following sections define the timing sequence required to operate a variety of optional random access data modes for address multiplexed DRAMs.

1.1 PAGE MODE

Page Mode is initiated with the row (word) address strobed by the falling edge of RE. While RE remains asserted any combination of successive read or write operations on randomly selected column (bit) addresses may be initiated by the falling edge of CE. During a read cycle, data out (Q) is terminated (high impedance) when CE goes inactive. A write cycle is initiated, and data-in sampled, at the concurrence of CE and W active. Page mode is terminated by RE going inactive.

1.2 STATIC COLUMN MODE

Static Column Mode features a static “ripple through” column address decoder. While RE remains asserted, successive reads or writes of randomly selected column addresses of the currently selected row are initiated by an address transition. A write operation is initiated, and data-in sampled, at the concurrence of W and CE active. Note that CE may function as an output enable rather than a column address strobe. Static Column operation is terminated by RE going inactive.

1.3 FAST PAGE MODE

Fast Page Mode is a latched Static Column operation. It is initiated with a row address strobed by the falling edge of RE. While RE remains asserted, successive read or write operations on randomly selected column addresses are controlled by CE. The mode is similar to that of Static Column with the addition of a “flow-through” address latch that is controlled by CE.

open with RE active and CE inactive

latched with RE active and CE active

During a read operation, CE going active will also enable data out and CE going inactive will also place the output terminals into a high impedance state. Note that read cycle access times in Fast Page mode are often measured from the point where CE is inactive with a valid address. Data-in for a write operation is sampled at the concurrence of CE and W active. Fast Page mode is terminated by RE going inactive.

1.4 EXTENDED DATA OUT FAST PAGE MODE

In this variation of Fast Page Mode, in a read operation, the low to high transition of CE with RE active will not place the data out terminals into a high impedance state. Data-out will remain valid. During sequential read operations the data out terminals will transition from old to new data. The data out terminals will not go to the high impedance state until both RE and CE are inactive.

2 SERIAL ACCESS MODES

The following sections define the timing sequence required to operate a variety of serial access data modes for address multiplexed DRAMs.

2.1 NIBBLE MODE

Nibble mode provides high speed serial access of 4 sequential address locations. A Nibble Mode cycle is initiated with the row address strobed by the falling edge of RE. An initial, randomly selected, column address is strobed by the falling edge of CE. While RE remains asserted, reads or writes of sequential column addresses (modulo 4) can be performed by cycling CE. The column address is internally incremented by +1 and wraps around. (4n+2, 4n+3, 4n, 4n+1, 4n+2, ...)

Nibble mode is terminated by the rising edge of RE.

2.2 BYTE MODE

Byte Mode is an extension of the Nibble Mode operation to modulo 8. As in Nibble Mode, the initial column address may be randomly selected, and is automatically incremented by +1 at each cycle of CE. The column address accessed is modulo 8 and wraps around (8n+6, 8n+7, 8n, 8n+1 ...).

2.3 BURST MODE

Burst Mode provides high speed serial access to all column addresses along a single row. Burst mode is initiated with a row address strobed at the falling edge of RE. An initial, randomly selected column address is strobed at the falling edge of CE. While RE remains asserted, read or write operations on sequential column addresses can be performed by cycling CE. Like Nibble and Byte Modes, the column address is incremented by +1 and wraps around. (N-3, N-2, N-1, 0, 1, ...) Burst mode operation is terminated by RE going inactive.

2.4 STREAMING MODE

Streaming Mode is an extension of Burst Mode. In addition to being modulo N in the column direction, the row address is also incremented by +1 when the column address wraps from N-1 to 0. At the maximum row and maximum column addresses, both will wrap around to row 0, column 0, at the next cycle of CE.

3 REFRESH MODES

The following sections define the timing sequence required to operate a variety of modes which refresh the data in address multlipexed DRAMs.

3.1 RAS ONLY REFRESH

A cycle with RE active and CE inactive is a RAS Only Refresh cycle. The address of the row to be refreshed is externally provided.

3.2 INTERNAL REFRESH (CAS BEFORE RAS REFRESH, CBRR)

A CBR refresh will occur if any CE is active and W is inactive when RE falls. External addresses are ignored; an internal refresh address counter supplies the address of the row to be refreshed. The refresh counter is incremented during each CBR cycle. Figure 3.9.5-2 shows the timing relationships which must be maintained to perform an internal refresh cycle

3.3 HIDDEN REFRESH

A Hidden Refresh occurs when RE is cycled while CE remains active. If data out (Q) was valid at the start of the refresh cycle, it will remain valid for the duration of CE active. For devices with CBR, the internal refresh address counter supplies the refresh address and is incremented during the cycle. Devices without CBR that support Hidden Refresh require the refresh address to be supplied externally.

3.4 SELF REFRESH

Self Refresh occurs when a CBR cycle is initiated following which RE and CE are kept active for an indefinite time that exceeds the DRAM active specification. The part then will internally cycle through all refresh addresses at a rate defined by the internal design of the part. The mode is exited by RE going inactive. The required timing relationships are shown in Figure 3.9.5-1B

4 WRITE MODES

The following sections describe the various WRITE modes which can be used with address multiplexed DRAMs

4.1 EARLY WRITE

W has transitioned to the active state, and data in is valid, prior to CE transitioning from high to low. Additional high to low transitions of W while CE remains active are not interpreted as write cycles. Data-out (Q) remains in a high impedance state for the duration of the cycle.

Note: Multiple Early Write cycles can be performed within a single RE cycle.

4.2 LATE WRITE

During a RE/CE cycle, W is inactive when CE transitions from high to low. W will be asserted after CE transitions from high to low. Data-in will be sampled and the write operation initiated by W going active.

Note: Multiple Late Write cycles can be performed at several column addresses during a single RE cycle.

Note: For devices with bidirectional (DQ) input/outputs, the output drivers should be disabled by G (and the data-in provided), prior to the the falling edge of W.

4.3 READ WRITE

This is a late write cycle at a single address for memory devices with independent data-in (D) and data-out (Q) terminals. During a RE/CE cycle W is inactive when CE transitions from high to low. W will be asserted prior to the data access time of the memory. The memory will start a write operation with new data-in in parallel with the access of the previously stored information.

4.4 READ MODIFY WRITE

This is a late write cycle at a single address where the state of W remains inactive until after the access time of the memory and then goes active. (As data has been read out of the memory prior to writing, the data to be written could be the modified data out.)

4.5 BIT WRITE

A write cycle for a n bit wide memory in which the data bits that are to be written are controlled by a write mask. Write per Bit is selected by W active and CE inactive as RE transitions to the active state. The mask is supplied at the beginning of the write cycle on the data-in terminals. A high mask bit enables the write function for that bit. A low mask bit leaves the previously stored data unaltered. Figure 3.9.5-1 shows the riming relationships which must be maintained for a bit write cycle.

4.6 FLASH WRITE

This is a write cycle in which the contents of an entire row of the memory array can be selectively set to a stated value. For an n bit wide memory, the write per bit register determines which bits of the word are to be altered.

4.7 BLOCK WRITE

A write cycle in which n sequential column addresses, modulo n, are written in a single operation. The n locations are controlled by the LSB of the column address.

NON-ADDRESS MULTIPLEXED DRAM OPERATIONAL REQUIREMENTS

All DRAMs that do not utilize address multiplexing must have internal architecture that allows them to operate with the following characteristics:

NON-ADDRESS MULTIPLEXED DRAM with PAGING

Non-Multiplexed DRAMs require that all addresses be valid at $\overline{RE}$ time; however $\overline{CE}$ is still needed for control of other standard DRAM modes & features. A Non-Muxed DRAM is the same as a multiplexed DRAM except for the four items listed below:

1 ALL Refresh modes are supported, but ”RAS-Only” is not recommended;

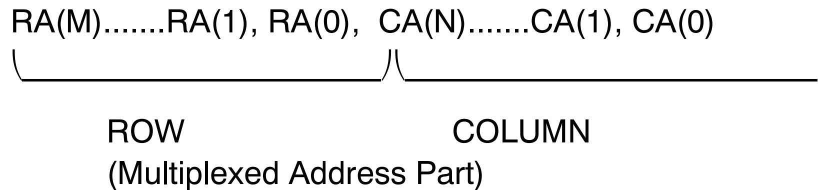
2 All addresses are provided valid at $\overline{RE}$ ($\overline{RAS}$) time;

3. 1st $\overline{CE}$ is Non-Critical; it is used only to enable the output(s);

4. Subsequent $\overline{CE}$s (with Low-Order Addresses) or only the Low-Order Addresses provide the various DRAM column operations such as Page Mode, Static Column Mode, and Page Mode. The length of a column is limited by the number of Low-Order Addresses, which is manufacturer defined.

Non-Muxed to Muxed address equivalents

ADDRESSES: Non-Multiplexed Part (High to Low Order)
High Low



Extended Data Out Standard

This Standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part encorporating ”EDO” must satisfy all of the following criteria to conform to the Standard.

1. Data out remains valid when $\overline{RAS}$ is active, $\overline{CAS}$ is inactive, and $\overline{WE}$ is inactive, and $\overline{OE}$ is active. In this case, either $\overline{WE}$ going active, or $\overline{OE}$ going inactive will cause the output to go high Z
2. Data output becomes high Z when both $\overline{CAS}$ and $\overline{RAS}$ are inactive.
3. When $\overline{RAS}$ and $\overline{CAS}$ are active and $\overline{WE}$ is inactive, output is controlled (turned on or turned off) as a static function of $\overline{OE}$. In an active Read cycle with $\overline{RAS}$ and $\overline{CAS}$ low, a change in state of $\overline{WE}$ to active low. is illegal.
4. If the output is high z when $\overline{CAS}$ goes inactive, the output will remain in high Z with G either active or inactive.
5. When $\overline{RAS}$ is active and the output from a read cycle is turned off by $\overline{WE}$ going active, the output will remain in a high Z state until a subsequent read is executed.
6. If output transitions from low Z (output turned on) to high Z (output turned off) while $\overline{CAS}$ is inactive, the output will remain high Z until a subsequent read cycle is executed.
7. Data from a read cycle will remain valid when $\overline{RAS}$ goes inactive as long as both $\overline{CAS}$ and $\overline{OE}$ will remain active. After $\overline{RAS}$ goes inactive, $\overline{WE}$ becomes a ”don’t care” and has no influence on the output.
8. When the output is high Z and $\overline{RAS}$ is inactive, the output will remain high Z, independent of the levels on $\overline{CAS}$ or $\overline{OE}$, until a $\overline{RAS}$ active read cycle is executed.

Definitions of terms used in EDO description:

High Z: An output logic state that presents a high impedence (neither sourcing or sinking) to any driving device.

Low Z: An output logic state that presents a low inpedence (either sourcing or sinking current) to any driving device.

Active Low: (low true) A logic description where a low signal represents a logical “active” condition. Note: All input signals included in this specification of EDO are “low true”.

Read Cycle: A memory cycle for which the control signals are applied in the appropriate sequence to have data read from the device and presented on the output terminals.

256M DRAM Address Compression for Test-Mode

Devices		16K Refresh cycles (RA0-RA13)			8K Refresh cycles (RA0-RA12)		
		Normal Mode Input Addr.	Test Mode		Normal Mode Input Addr.	Test Mode	
			Input Address	Compress. Address		Input Address	Compress. Address
256M	64M X 4	RA0-RA13 CA0-CA11	RA0-RA13 CA0-CA7	CA8-11	RA0-RA12 CA0-CA12	RA0-RA12 CA0-CA8	CA9-12
	32M X 8	RA0-RA13 CA0-CA11	RA0-RA13 CA0-CA7	CA8-10	RA0-RA12 CA0-CA11	RA0-RA12 CA0-CA8	CA9-11
	16M X 16	RA0-RA13 CA0-CA9	RA0-RA13 CA0-CA7	CA8-9	RA0-RA12 CA0-CA10	RA0-RA12 CA0-CA8	CA9-10
	8M X 32	RA0-RA13 CA0-CA8	RA0-RA13 CA0-CA7	CA8	RA0-RA12 CA0-CA9	RA0-RA12 CA0-CA8	CA9

256M DRAM Data Space Compression for Test-Mode

When the memory device is operating in the compression mode, the data space is compressed with four DQn circuits supplying test data and receiving test results as defined in the following table.

Devices		Normal Mode Data Interface	Test Mode Data Interface	
			Active Data Bits	Data Bits Served
256M	64M X 4	DQ0-DQ3	DQ0	DQ0
			DQ1	DQ1
			DQ2	DQ2
			DQ3	DQ3
	32M X 8	DQ0-DQ7	DQ0	DQ0, DQ1
			DQ3	DQ2, DQ3
			DQ5	DQ4, DQ5
			DQ6	DQ6, DQ7
	16M X 16	DQ0-DQ15	DQ0	DQ0⇒DQ3
			DQ7	DQ4⇒DQ7
			DQ11	DQ8⇒DQ11
			DQ12	DQ12⇒DQ15
	8M X 32	DQ0-DQ31	DQ0	DQ0⇒DQ7
			DQ15	DQ8⇒DQ15
			DQ23	DQ16⇒DQ23
			DQ24	DQ24⇒DQ31

256M DRAM ADDRESS AND DATA SPACE COMPRESSION FOR TEST MODE

Pipelined Nibble Mode Definition

Devices that operate in the Pipelined Nibble Mode are required to meet the following criteria to conform to this Standard.

1. Burst Length shall be 4
2. Read Latency shall be 2 (refer to attached timing diagram for clarification)
3. Write Latency shall be 0
4. A WCBR, with the address keys shown below, is used to program the burst sequence. It is persistant until it is reprogrammed.

   Address

Sequence	A0	A1	A2	A3	A4	A5	A6	A7
Linear	0	0	0	0	0	1	0	0
Interleaved	1	0	0	0	0	1	0	0

5. $\overline{\text{WE}}$ transition during $\overline{\text{CAS}}$ precharge time causes burst to terminate
6. $\overline{\text{WE}}$ transition during $\overline{\text{CAS}}$ low, which remains through the $\overline{\text{CAS}}$ rising edge, causes burst to terminate.
7. $\overline{\text{WE}}$ pulse which is fully enclosed by a $\overline{\text{CAS}}$ low will be ignored and not cause a burst terminate.
8. Same output enable function as in EDO definition.
9. Read-modify-write cycle within $\overline{\text{CAS}}$ active cycle is not supported.
10. A Pipelined Nibble Mode device may not be reconfigured by the user to operate in the standard EDO (non-burst) mode.