

3.9.4 Word Wide DRAM

3.9.4.1 – 64K BY 16 DRAM WITH 2 \bar{W} IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\bar{C}\bar{E}$ OR 2 \bar{W} DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
The standard for the 2 \bar{W} versions of the 1M part has been rescinded and removed from Figs. 3.9.4–4 & 3.9.4–5 in Release 5.

LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 \bar{W} and the other with 2 $\bar{C}\bar{E}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP2

CAPACITY—2M & 4M WORDS OF 16 or 4M WORDS OF 18 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts utilizes 4K or 8K refresh cycles
PACKAGE—50 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH, X16 parts only
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

3.9.4.5 – 128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, OR ZIP

CAPACITY—128K OR 256K WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts have BURST data out capability
PACKAGE—40 PIN SOJ, 10.16 mm WIDE, 1.27 mm PIN PITCH
PACKAGE—44/40 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH
PACKAGE—40 PIN ZIP, 1.27 mm PIN PITCH (256K only)
PIN ASSIGNMENT—SOJ, Fig. 3.9.4–9
PIN ASSIGNMENT—TSOP2, Fig. 3.9.4–10
PIN ASSIGNMENT—ZIP, Fig. 3.9.4–11, (256K ONLY)

3.9.4.6 – 16M X 16 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 16M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT—Fig. 3.9.4-12

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.7 – 128K, 256K, & 512K X 32 DRAM WITH 4 \overline{CE} IN SSOP

CAPACITY—128K, 256K, OR 512K WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address

—The part, has 4 \overline{CE} , one controlling each group of 8 data bits.

PACKAGE— 64 PIN SSOP, 0.525" WIDE, PP = 0.8 mm

PIN ASSIGNMENT—Fig. 3.9.4-13

3.9.4.8 – 512K & 2M BY 32 & 36 DRAM WITH 4 \overline{CE} IN SOJ & TSOP2

CAPACITY—512K, 2M WORDS OF 32 & 36 BITS,

LOGIC FEATURES—MULTIPLEXED ADDRESS

—The part, has 4 \overline{CE} , one controlling each group of 8 or 9 data bits.

—The standard allows the option of the manufacturer to utilize either 1K or 4K refresh cycles

PACKAGE—70 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PP

—70 PIN TSOP2, 10.16 mm WIDE, 0.65 mm PP, 512K only.

—70 PIN SOJ, 10.16 mm WIDE, 0.8 mm PP

PIN ASSIGNMENT—Fig. 3.9.4-14

3.9.4.9 – 8M X 32 DRAM IN TSOP2 PIN ROTATION (OBSOLETE, DO NOT USE)

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT—Fig. 3.9.4-15

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time. (THIS STANDARD WAS DECLARED OBSOLETE IN 1998)

3.9.4.10 – 2M X 32 DRAM IN TSOP2

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—86 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP

PIN ASSIGNMENT—Fig. 3.9.4-16

3.9.4.11 – 2M X 32 DRAM WITH EDO IN QFP

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

—The Data Out conforms to the EDO feature defined in Par. 3.9.5.7.

PACKAGE—100 PIN QFP OR TQFP, 10 mm BU 14 mm, 0.65 mm PP

PIN ASSIGNMENT—Fig. 3.9.4-17

3.9.4.12 – 1M BY 16 DRAM IN USON

CAPACITY—1M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—46 PAD USON, 7 mm WIDE, 0.5 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.4-18

3.9.4.13 – 4M BY 16 DRAM IN USON

CAPACITY—4M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—58 PAD USON, 10 mm WIDE, 0.5 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.4-19

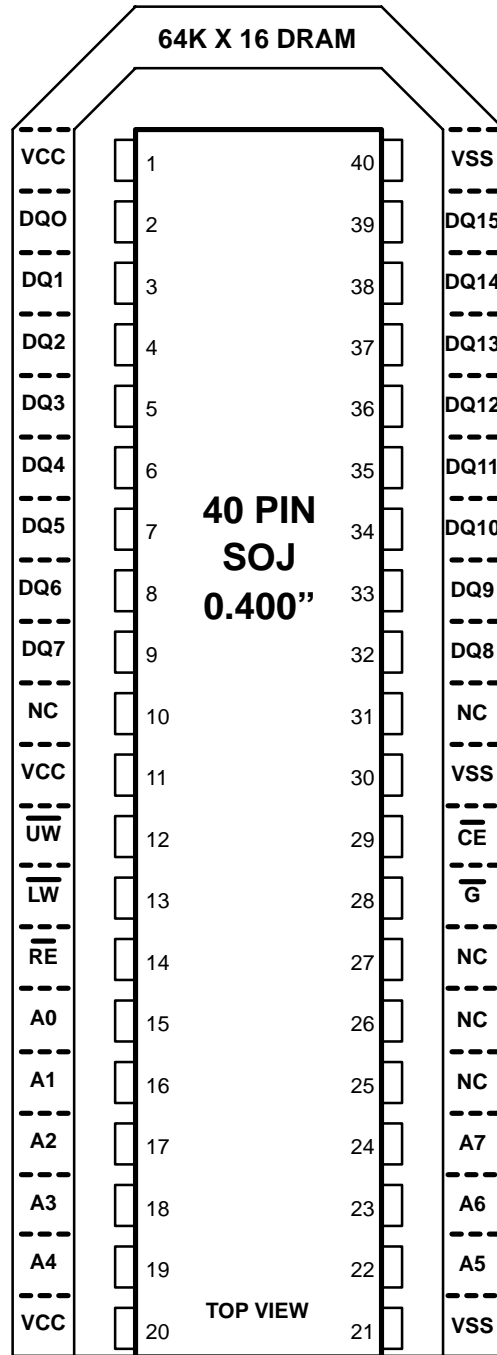


FIGURE 3.9.4-1
64K BY 16 DRAM IN SOJ

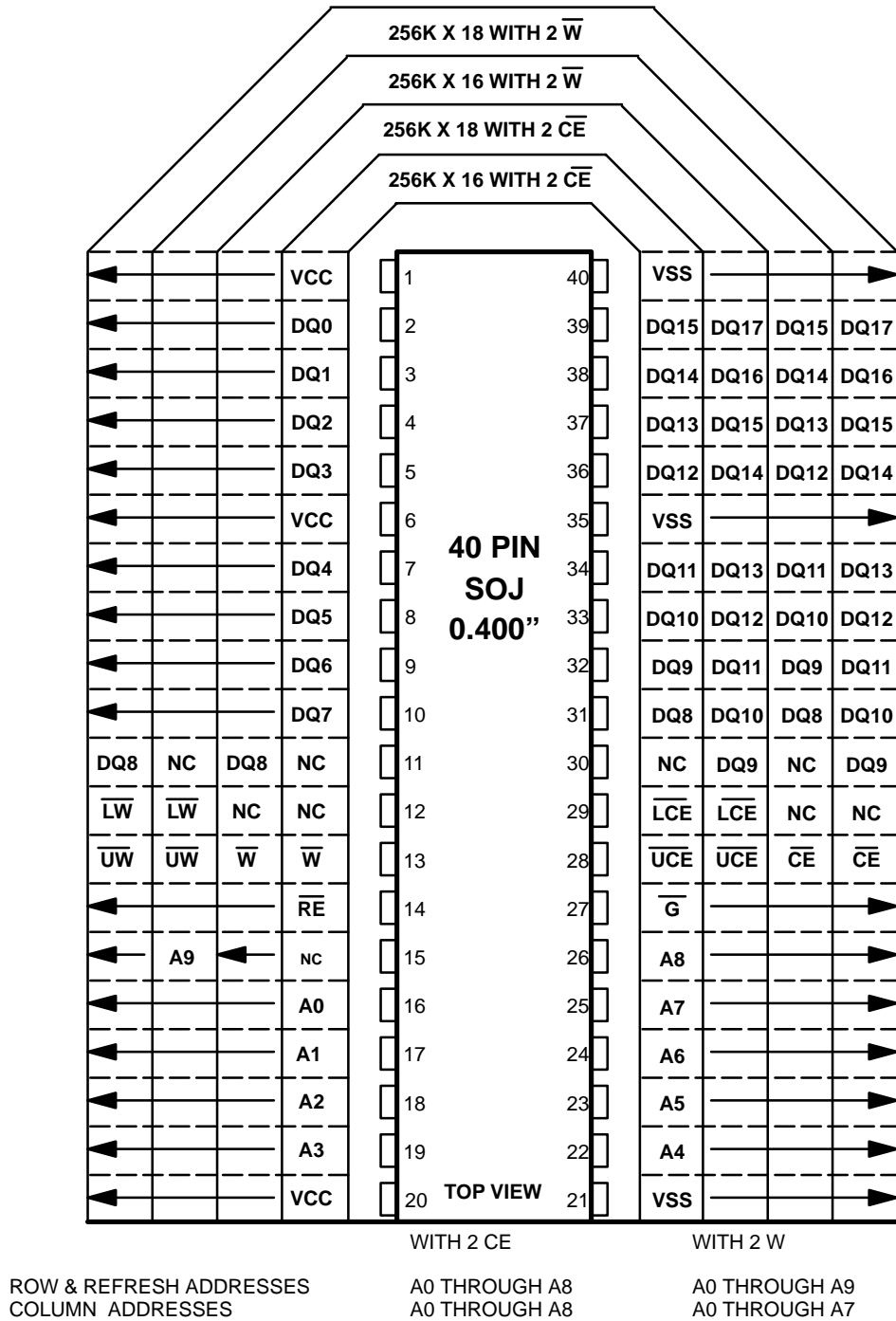
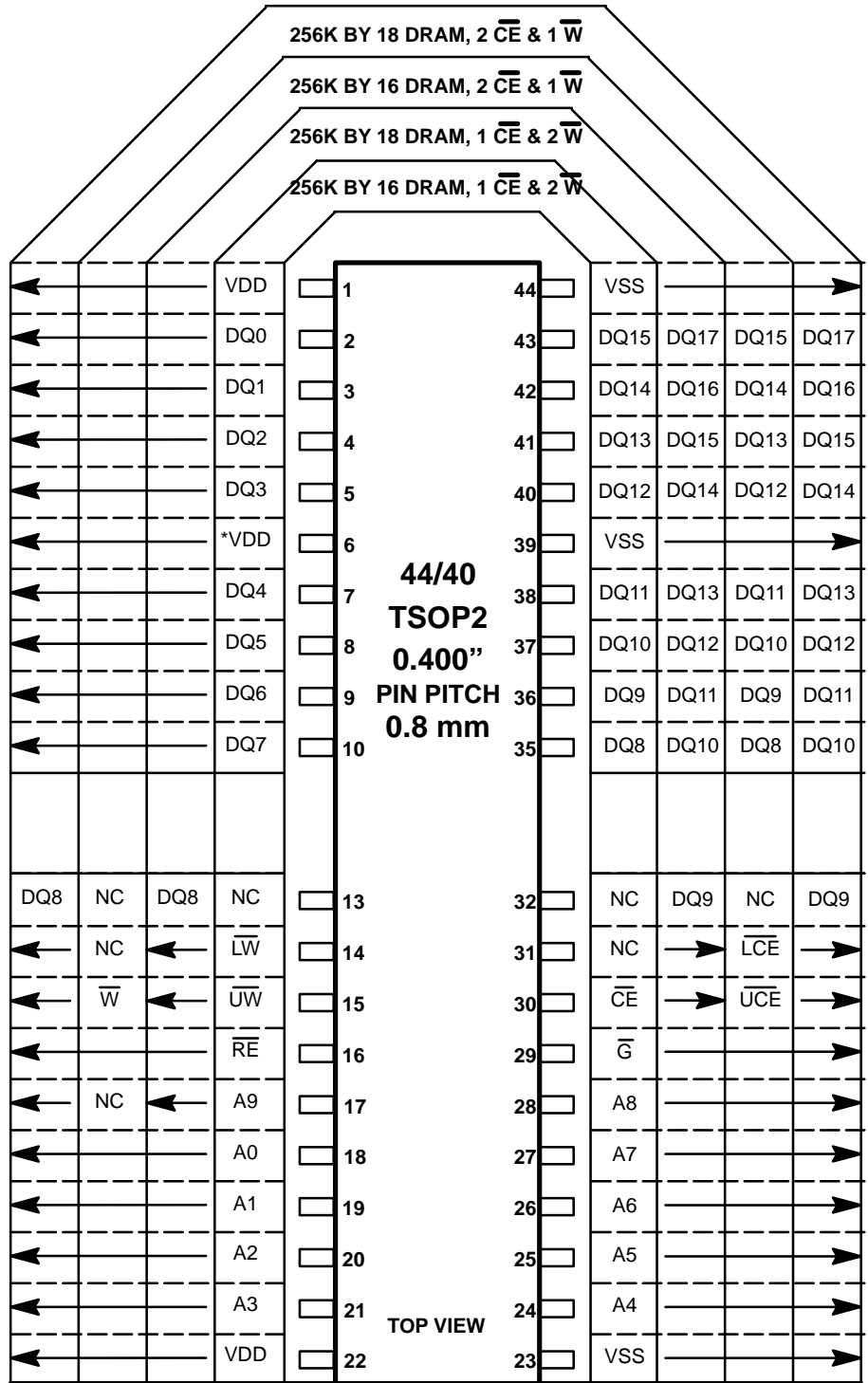


FIGURE 3.9.4-2
256K BY 16 & 18 DRAM WITH 2 W OR 2 CE IN SOJ



CONFIGURATION	1 \overline{CE} , 2 \overline{W}	2 \overline{CE} , 1 \overline{W}	The JEDEC Std. No 30 designator for the TSOP2 package is PDSO-G
REFRESH COUNT	1024 Cycles	512 Cycles	
REFRESH ADDRESS	A0 TO A9	A0 TO A8	
ROW ADDRESS	A0 TO A9	A0 TO A8	* NOTE: In the first release of this standard, Pin 6 was a VSS connection. This was in error and this release changes Pin 6 to VDD.
COLUMN ADDRESS	A0 TO A7	A0 TO A8	

FIGURE 3.9.4-3
256K BY 16 & 18 DRAM WITH 2 \overline{W} OR 2 \overline{CE} IN TSOP2

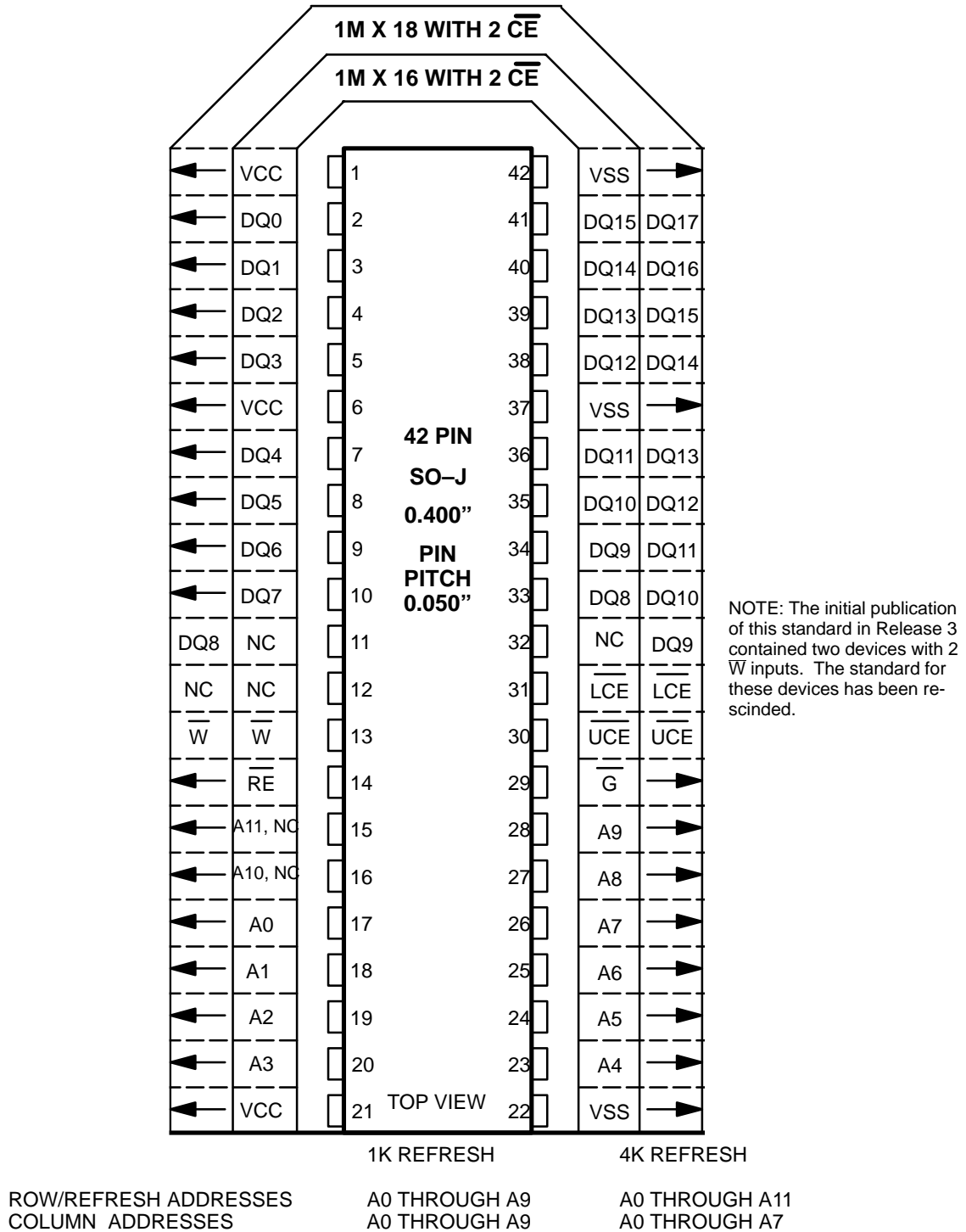


FIGURE 3.9.4-4
1M BY 16 & 18 DRAM WITH 2 \overline{CE} IN SOJ

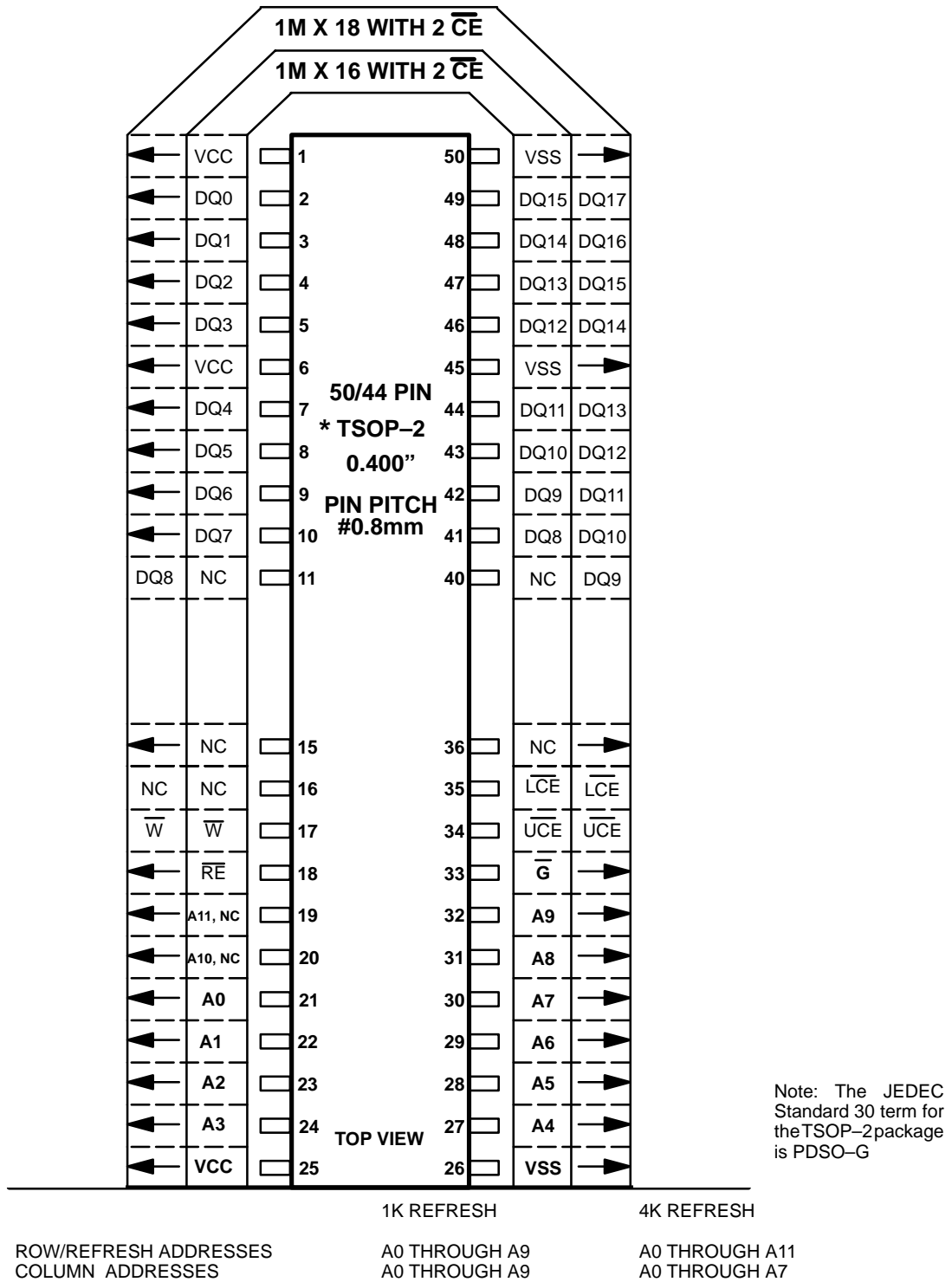
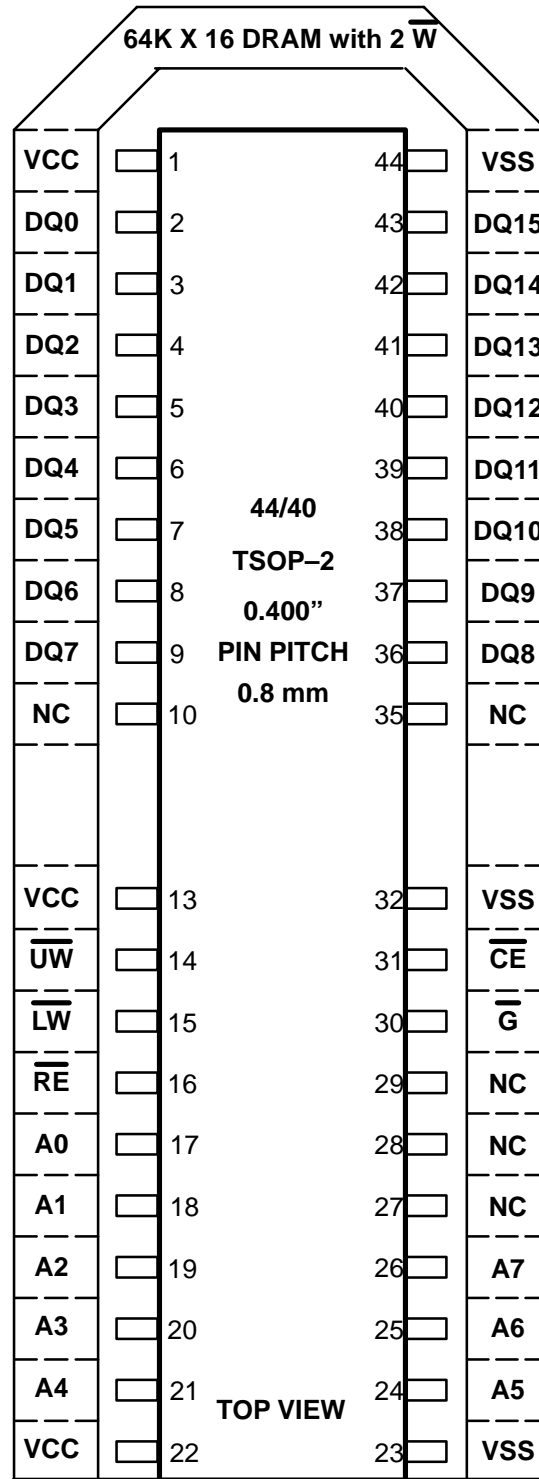


FIGURE 3.9.4-5

1M BY 16 & 18 DRAM WITH 2 \overline{CE} IN TSOP2



* Note: The JEDEC Standard 30 term for the TSOP-2 package is PDSO-G

ROW/REFRESH ADDRESSES A0 THROUGH A7
COLUMN ADDRESSES A0 THROUGH A7

FIGURE 3.9.4-6
64K BY 16 DRAM WITH 2 \overline{W} IN TSOP-2

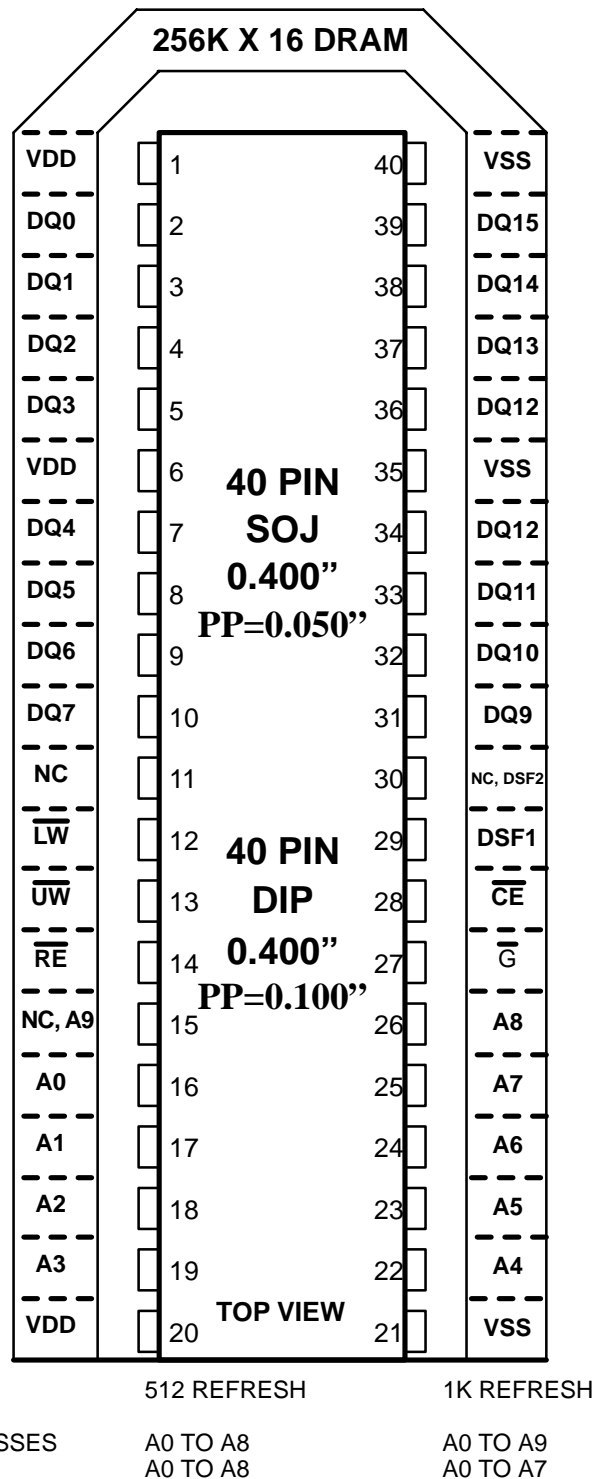


FIGURE 3.9.4-7 A

256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

MANDATORY TRUTH TABLE FOR 256K BY 16 DRAM with EXTENDED FUNCTIONS

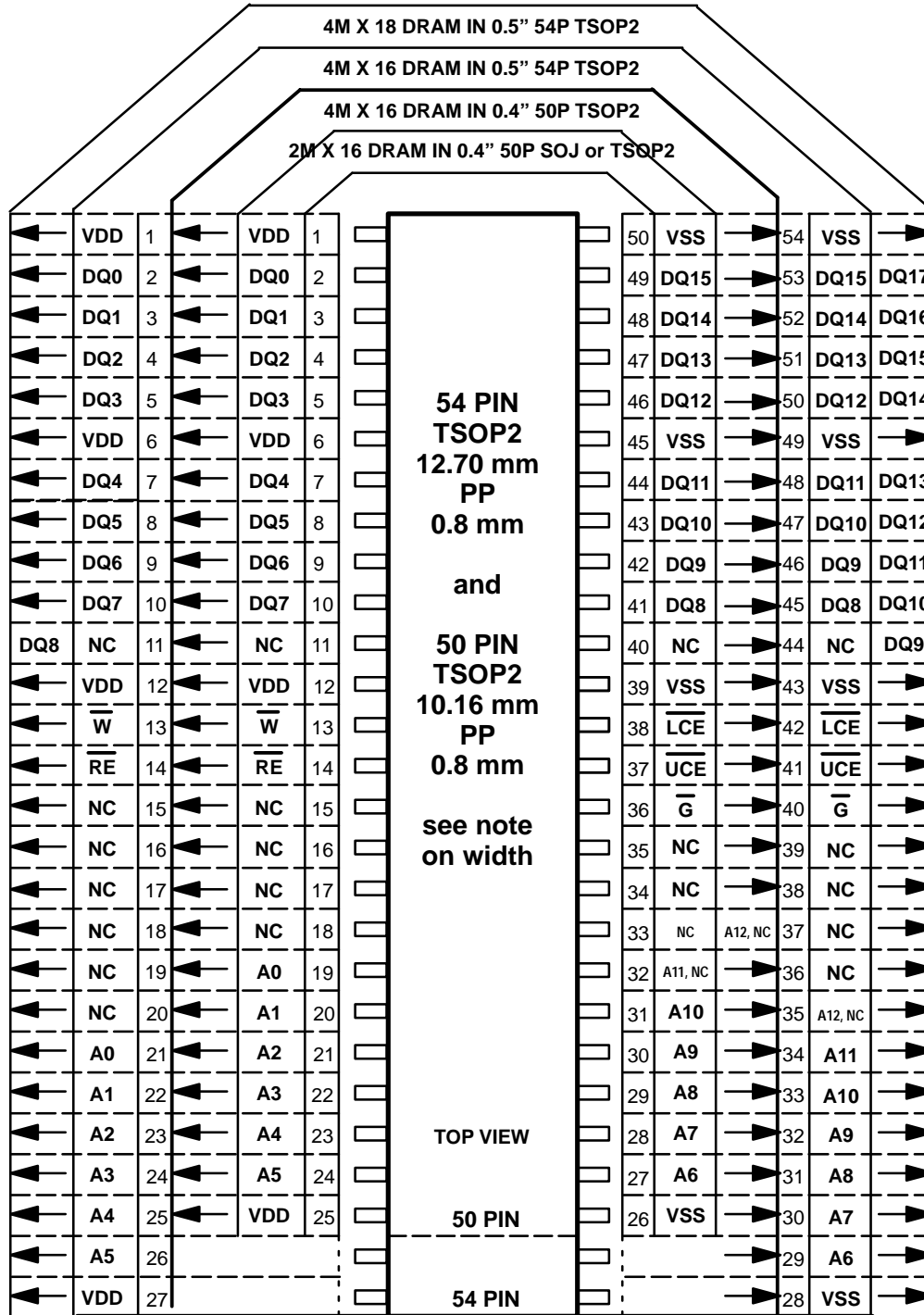
Mnem.	Function	Valid at RE					Valid at CE
		CE	G	W	DSF(1)	*DSF2	DSF(1)
RW	READ/WRITE	1	1	1	0	0	0
BW	BLOCK WRITE	1	1	1	0	0	1
LMR	LOAD MASK REGISTER	1	1	1	1	0	0
LCR	LOAD COLOR REGISTER	1	1	1	1	0	1
RWM	WRITE, MASKED	1	1	0	0	0	0
BWM	BLOCK WRITE, MASKED	1	1	0	0	0	1
CBR	CBR REFRESH (1)	0	X	1	0	0	X
CBRN	CBR REFRESH (2)	0	X	1	1	0	X
FWT	FLASH WRITE	1	1	0	1	0	X

* IF DSF2 IS PRESENT

CBR(1) – All optional modes reset

CBR(2) – Any optional modes remain active

FIGURE 3.9.4-7 B
256K BY 16 DRAM MANDATORY EXTENDED FUNCTION TRUTH TABLE



* NOTES:
For 54P parts,
Pin 35 is A12 for
8K rows and NC
for 4K rows.

For 50P 4M
parts, Pin 33 is
A12 for 8K rows
and NC for 4K
rows. Pin 32 is
NC for devices
with 11 row & 11
columns and
A11 for other
Refresh/Address
options..

For 50P 2M
parts, Pin 32 is
A11 for devices
with 4K rows
and NC for de-
vices with 2K
rows.

The use of CBR
for Refresh is
strongly recom-
mended for
these devices.

* NOTE: The
JEDEC Std. 30
term for the
TSOP-2 package
is PDSO-G.

This standard rec-
ognizes that some
early deliveries of
the 54P parts may
have to be in a
0.6" wide package

54 P ADDRESS CONFIGURATION
4M X 16/18
ROW ADDRESSES A0 → A11
COLUMN ADDRESSES A0 → A9

8K ROWS
A0 → A12
A0 → A8

50 P ADDRESS CONFIGURATION
2M X 16
ROW ADDRESS A0 → A10
COLUMN ADDRESS A0 → A9
4M X 16
ROW ADDRESS A0 → A10
COLUMN ADDRESS A0 → A10

2K ROWS
A0 → A10
A0 → A9
4K ROWS
A0 → A11
A0 → A9
8K ROWS
A0 → A12
A0 → A8

FIGURE 3.9.4-8

2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP-2

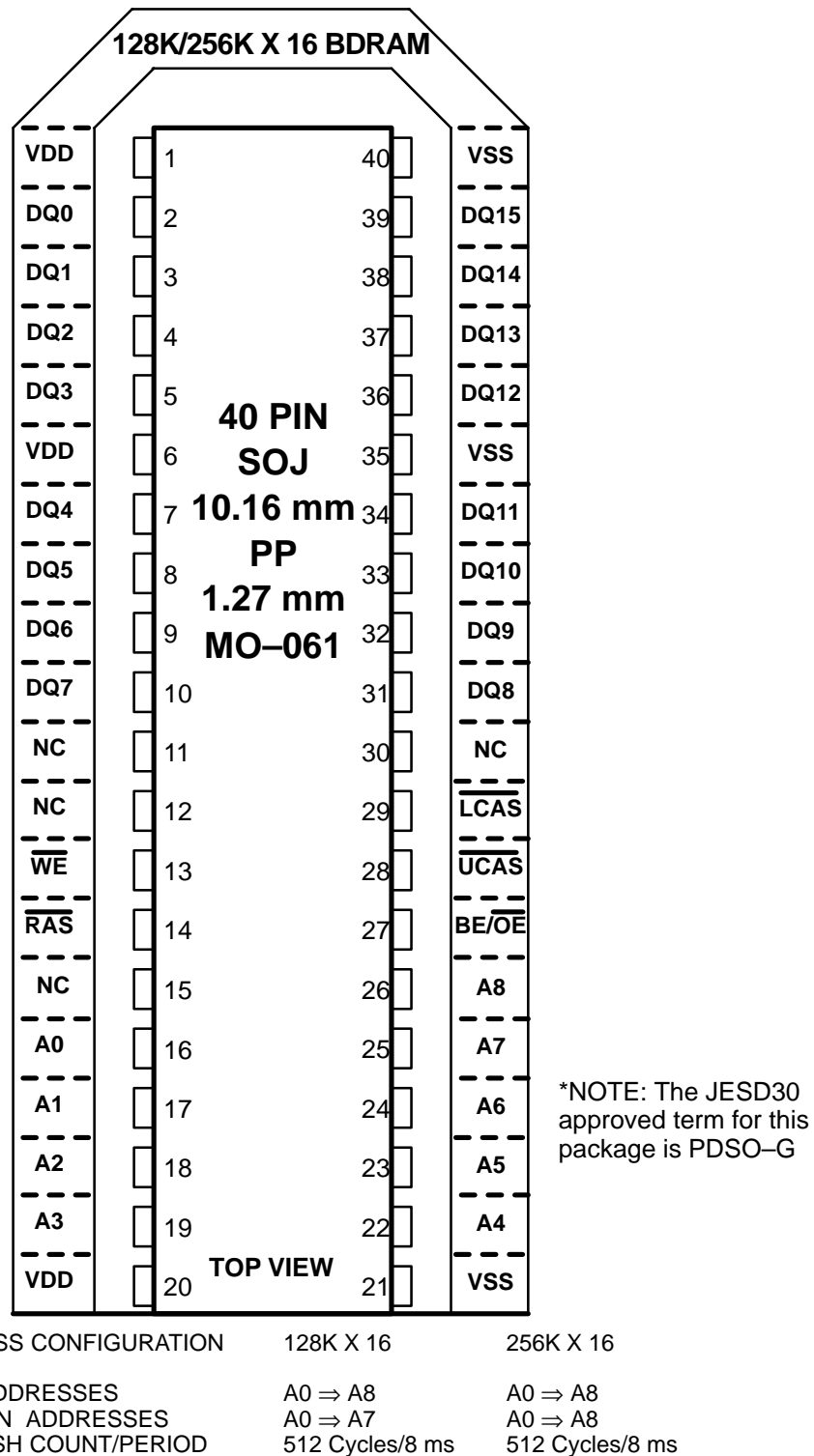
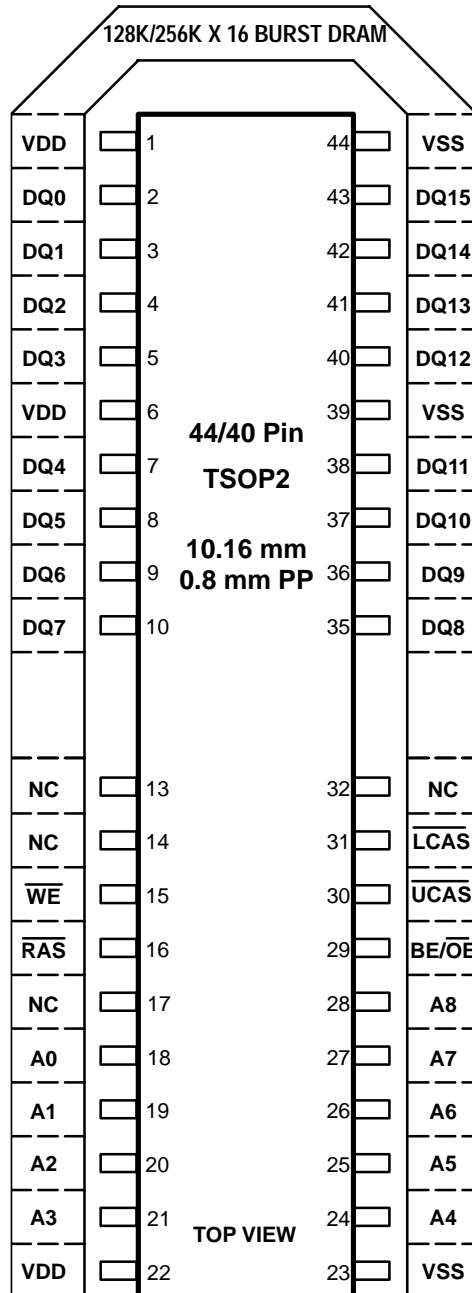


FIGURE 3.9.4-9
128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ



*NOTE: The JESD30 approved term for this package is PDSO-G

CONFIGURATION	128K X 16	256K X 16
ROW ADDRESSES	A0 ⇒ A8	A0 ⇒ A8
COLUMN ADDRESS	A0 ⇒ A7	A0 ⇒ A8
REFRESH COUNT/PERIOD	512/8 ms	512/8 ms

FIGURE 3.9.4-10

128K & 256K BY 16 BURST DRAM WITH 2 CAS IN TSOP2

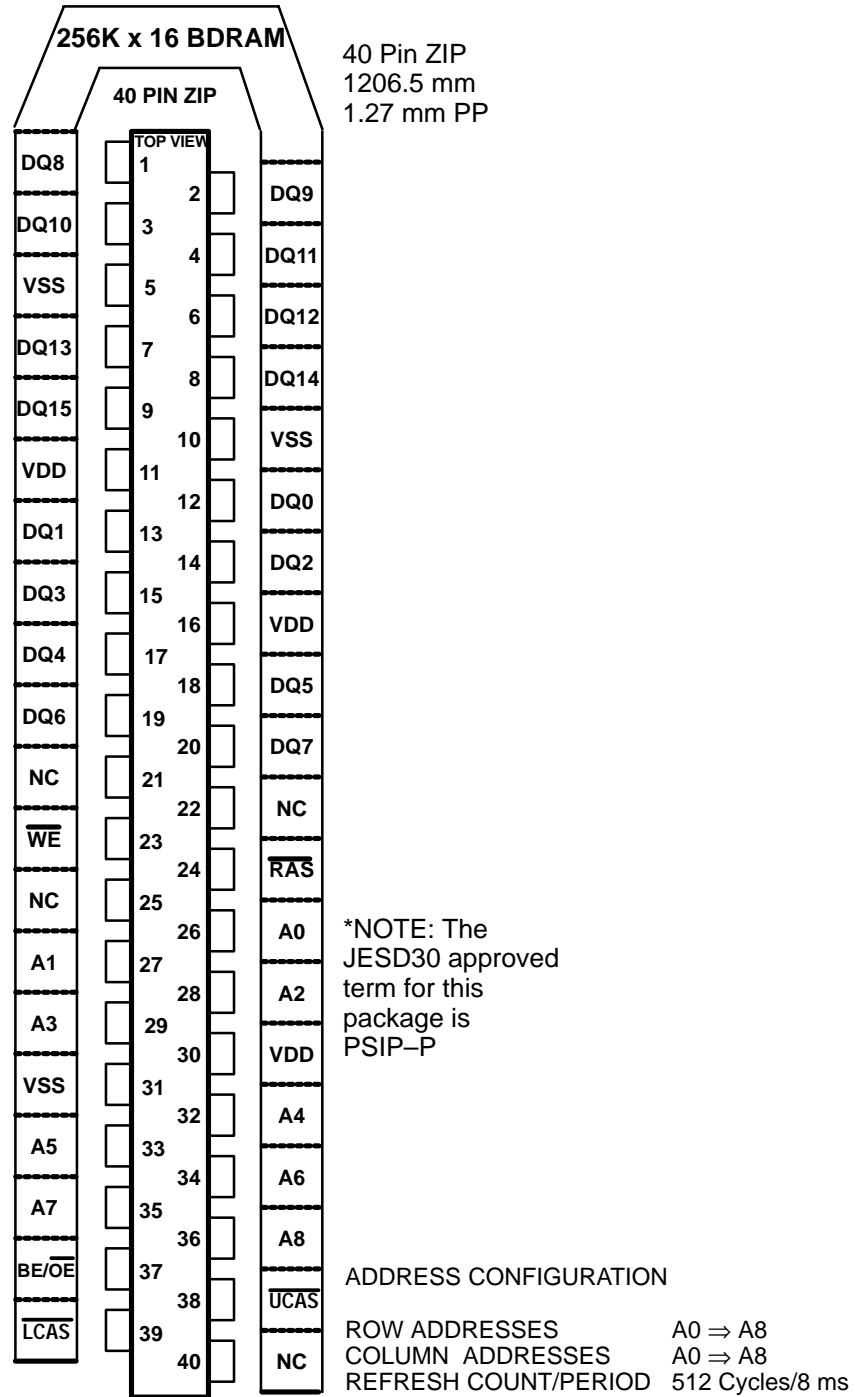
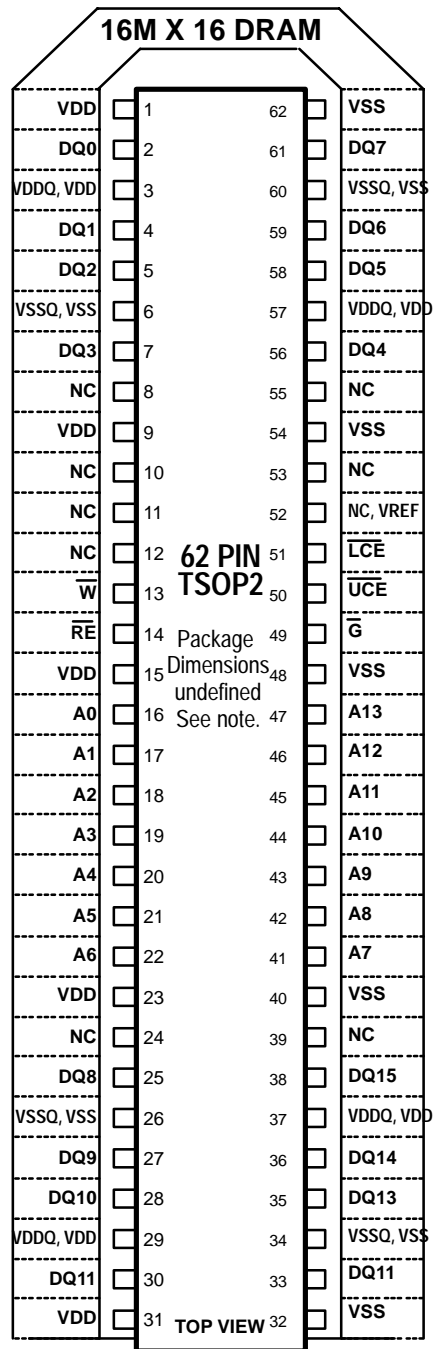


FIGURE 3.9.4-11
256K BY 16 BURST DRAM WITH 2 CAS IN ZIP



Configuration 16M X 16
ROW ADDRESS A0-A13
COLUMN ADDRESS A0-A9

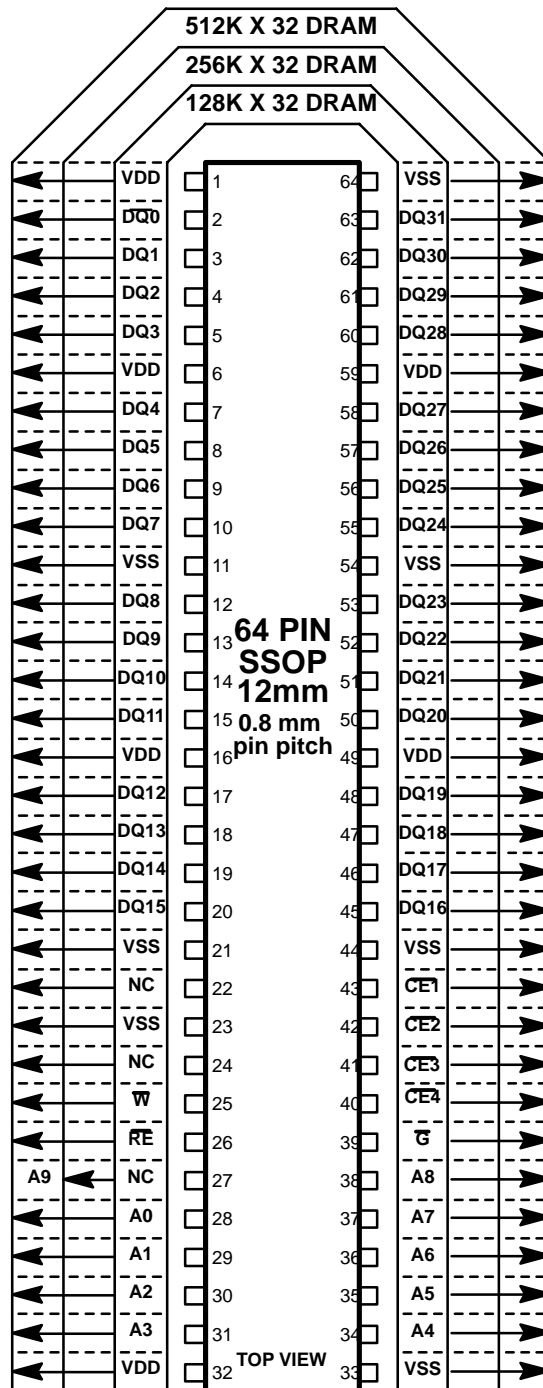
NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
2. CBR refresh is the only standardized method of refreshing non-synchronous DRAMs with densities of 256Mb and higher.
3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 μ s per row with 8K rows, 3.9 μ s with 16K rows.
4. (NC, VREF) is VREF on devices that require an external voltage reference.
5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.
6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

* NOTE: The JEDEC Std. 0 term for the TSOP-2 package is PDSO-G.

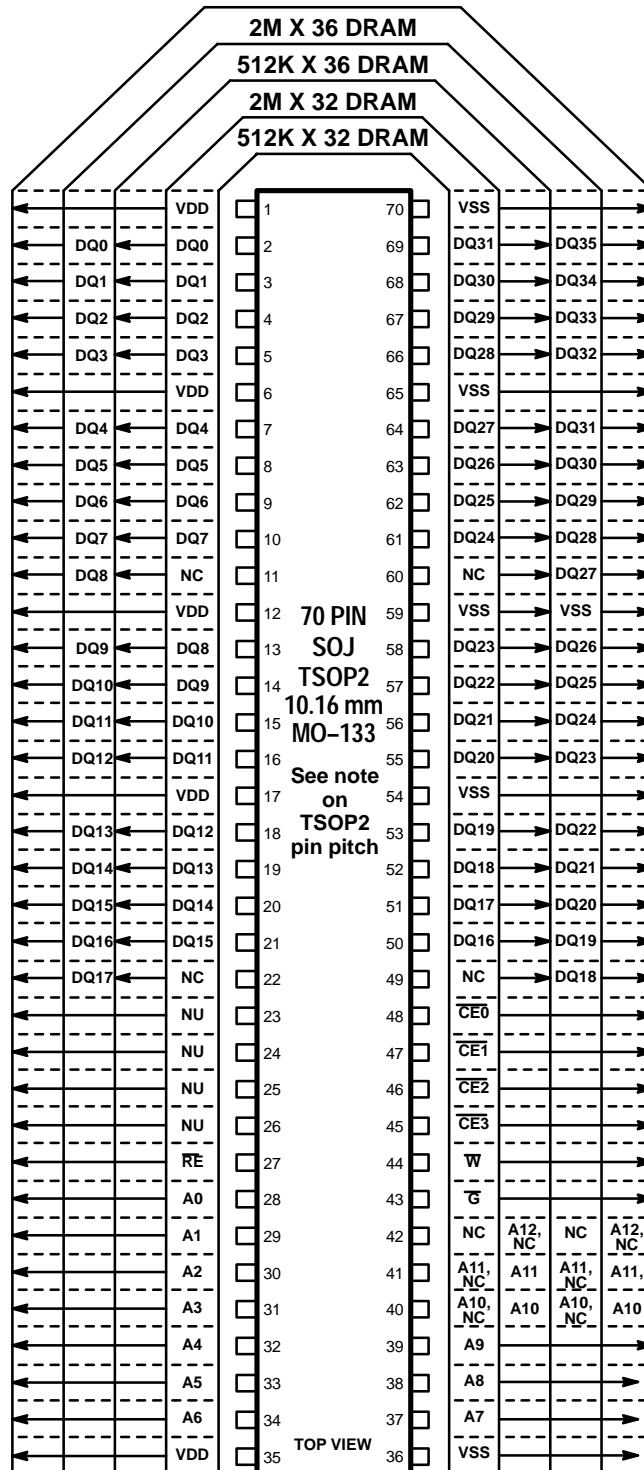
Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

FIGURE 3.9.4-12
16M BY 16 DRAM PIN ROTATION IN TSOP2



ADDRESS STRUCTURE	128K X 32	256K X 32	512K X 32
ROW Address	A0 ⇒ A8	A0 ⇒ A8	A0 ⇒ A9
Column Address	A0 ⇒ A7	A0 ⇒ A8	A0 ⇒ A8
Refresh Cycles/Period	512 Cycles/8 mS	512 Cycles/8 mS	1024 Cycles/16 mS

FIGURE 3.9.4-13
128K, 256K & 512K BY 32 DRAM WITH 4 CAS IN SSOP



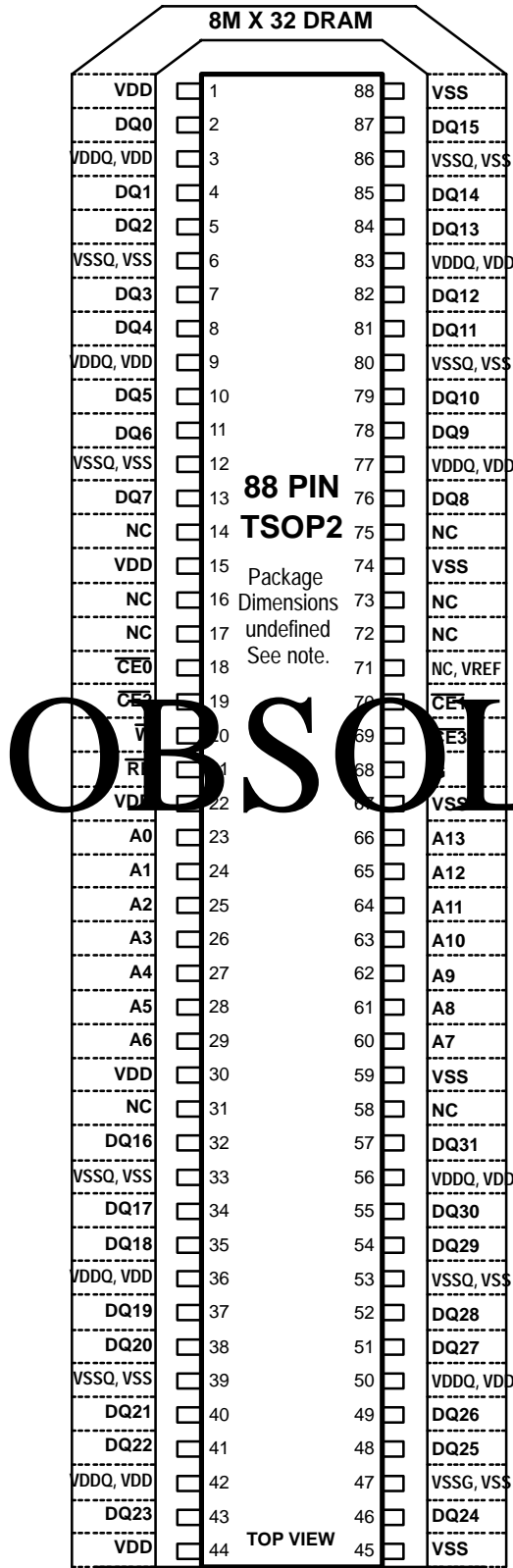
NOTE:
In addition to this pinout for a 2M X 32 SDRAM, there is another one that has the DQ pins at the outer ends of the package and the control pins in the center and supersedes this one. The other device should be used for all new designs. It is found in figure 3.9.4-16.

The 512K parts are approved with a TSOP2 package that has a pin pitch of either 0.8 mm or 0.65 mm. The 2M parts are approved with 0.8 mm only.

* NOTE: The JEDEC Std. 30 term for the TSOP-2 package is PDSO-G.

CAPACITY	512K		2M	
ADDRESS FIELD	1K REFRESH	4K REFRESH	4K REFRESH	8K REFRESH
ROW ADDRESS	A0-A9	A0-A11	A0-A11	A0-A12
COLUMN ADDRESS	A0-A8	A0-A6	A0-A8	A0-A7

FIGURE 3.9.4-14
512K & 2M BY 32 & 36 DRAM IN SOJ & TSOP2



NOTES

1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
2. CBR refresh is the only standardized method of refreshing non-synchronous DRAMs with densities of 256Mb and higher.
3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 μ s per row with 8K rows, 3.9 μ s with 16K rows.
4. (NC, VREF) is VREF on devices that require an external voltage reference.
5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.
6. The VSSQ designator is used when the column reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

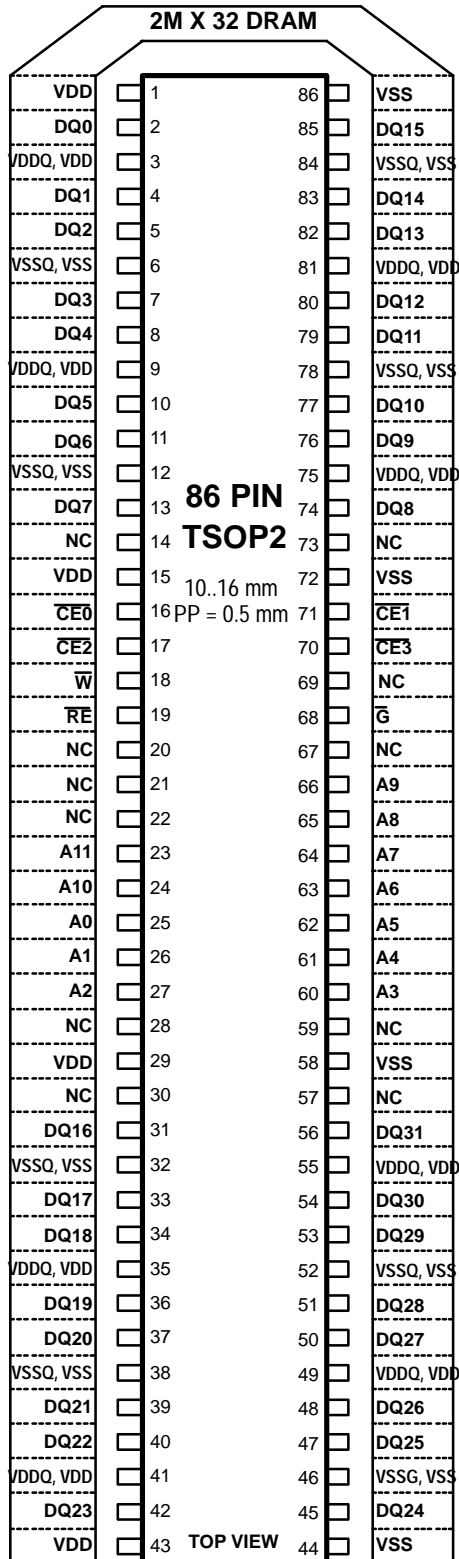
The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

Configuration	16M X 16
ROW ADDRESS	A0-A12
COLUMN ADDRESS	A0-A8

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

Note: This pin rotation is obsolete and will not be assigned to a package

FIGURE 3.9.4-15
8M BY 32 DRAM PIN ROTATION IN TSOP2



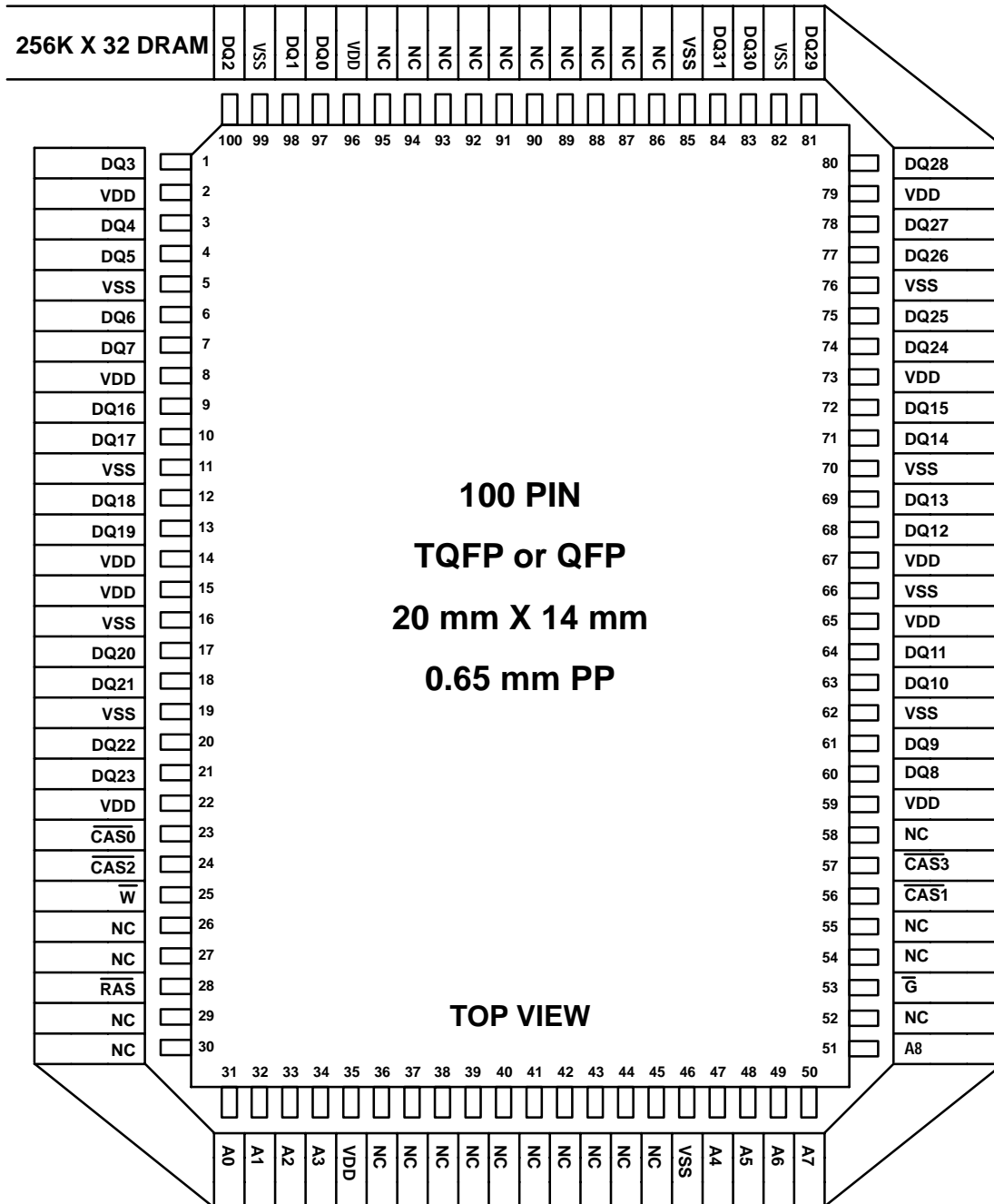
NOTES

1. The standard refresh period is 64 ms.
2. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally DC isolated from the VDD power supply pins.
3. The VSSQ designator is used when the ground reference pins

The JEDEC Std. No. 30 designator for the TSOP2 package is PDSO-G

Configuration	2M X 32
ROW COUNT	4K Rows
ROW ADDRESS	A0 ⇒ A11
COLUMN ADDRESS	A0 ⇒ A8

FIGURE 3.9.4-16
2M BY 32 DRAM IN TSOP2



Note: This device conforms to the EDO data out characteristic defined in Par. 3.9.5.7, and follows the same basic pin sequence as the SDRAM shown in Fig. 3.11.4-4 and the SGRAM shown in Fig. 3.10.3-4

Configuration
ROW ADDRESS
COLUMN ADDRESS
REFRESH PERIOD
ROWS REFRESH

256K X 32
A0⇒A8
A0⇒A8
8 mS
512

**FIGURE 3.9.4-17
256K BY 32, EDO DRAM IN QFP**

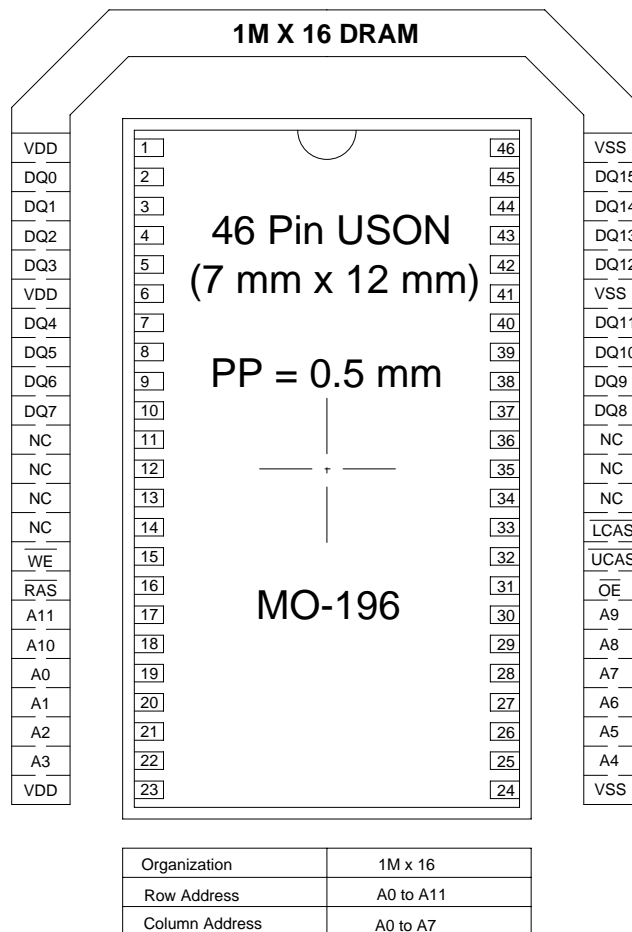
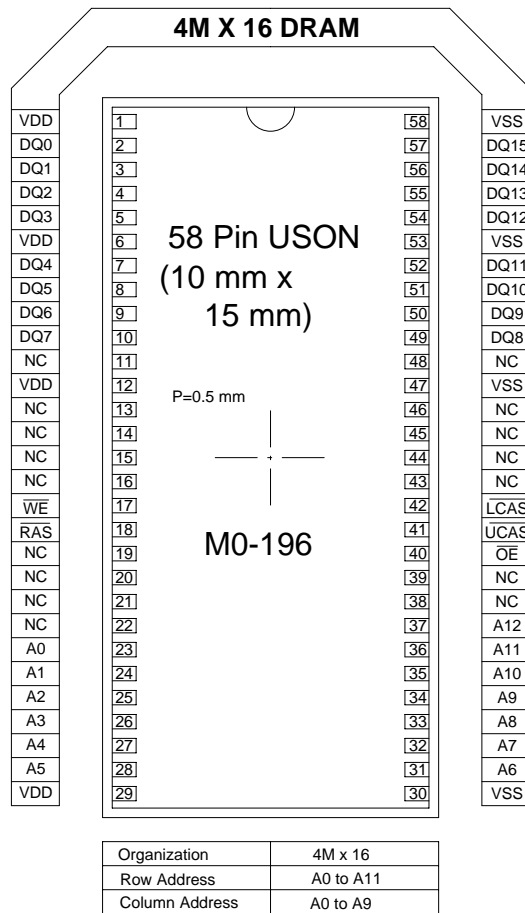


FIGURE 3.9.4-18
1M BY 16 DRAM IN USON



**FIGURE 3.9.4-19
 4M BY 16 DRAM IN USON**