

3.9.3 Byte Wide DRAM

3.9.3.1 – 32K BY 8 DRAM IN DIP

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–1

3.9.3.2 – 32K BY 8 DRAM IN RCC

CAPACITY—32K WORDS OF 8 BITS,
PACKAGE—32 PAD (PIN) RCC, 0.450" X 0.550"
PIN ASSIGNMENT—Fig. 3.9.3–2

3.9.3.3 – 512K BY 8 & BY 9 DRAM IN SOJ, TSOP2, & ZIP

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—28 PIN SOJ, 0.400" WIDE
—28 PIN TSOP2, 0.400" WIDE
—28 PIN ZIP, 0.475" WIDE
PIN ASSIGNMENT—SOJ & TSOP2, Fig. 3.9.3–3
—ZIP, Fig. 3.9.3–4

3.9.3.4 – 512K BY 8 & BY 9 NON-MUX DRAM IN SOJ

CAPACITY—512K WORDS OF 8 & 9 BITS,
LOGIC FEATURES—NON-MULTIPLEXED ADDRESS
PACKAGE—36 PIN SOJ, 0.400" WIDE
PIN ASSIGNMENT—Fig. 3.9.3–5

3.9.3.5 – 2M BY 8 & 9 DRAM IN SOJ & TSOP2

CAPACITY—2M WORDS OF 8 & 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 2K or 4K refresh cycles
PACKAGE—28 PIN SOJ or TSOP2, 0.300" or 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 Part
—32 PIN SOJ or TSOP2, 0.400" WIDE, 0.050" PIN PITCH for 2M BY 8 or 9 Part
PIN ASSIGNMENT—Fig. 3.9.3–6

3.9.3.6 – 8M BY 8 & 9 DRAM IN SOJ & TSOP2

CAPACITY—8M WORDS OF 8 or 9 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
—At the option of the manufacturer, these parts may utilize either 4K or 8K refresh cycles

The X8 part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.

PACKAGE—34 PIN SOJ, 0.500" WIDE
—34 PIN TSOP2, 0.500" WIDE, 0.025" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.3–7
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1–12

3.9.3.7 – 32M X 8 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 32M WORDS OF 8 BITS
LOGIC FEATURES—Multiplexed Address, Common DATA I/O
PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED
PIN ASSIGNMENT—Fig. 3.9.3–9

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.3.8 – 4M & 8M X 8 DRAM IN SOP

CAPACITY— 4M & 8M WORDS OF 8 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—32 PIN SOP, 11.18 mm WIDE

PIN ASSIGNMENT—Fig. 3.9.3-10

3.9.3.9 – 2M BY 8 DRAM IN USON

CAPACITY—2M WORDS OF 8 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—28 PAD USON, 7 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.3-11

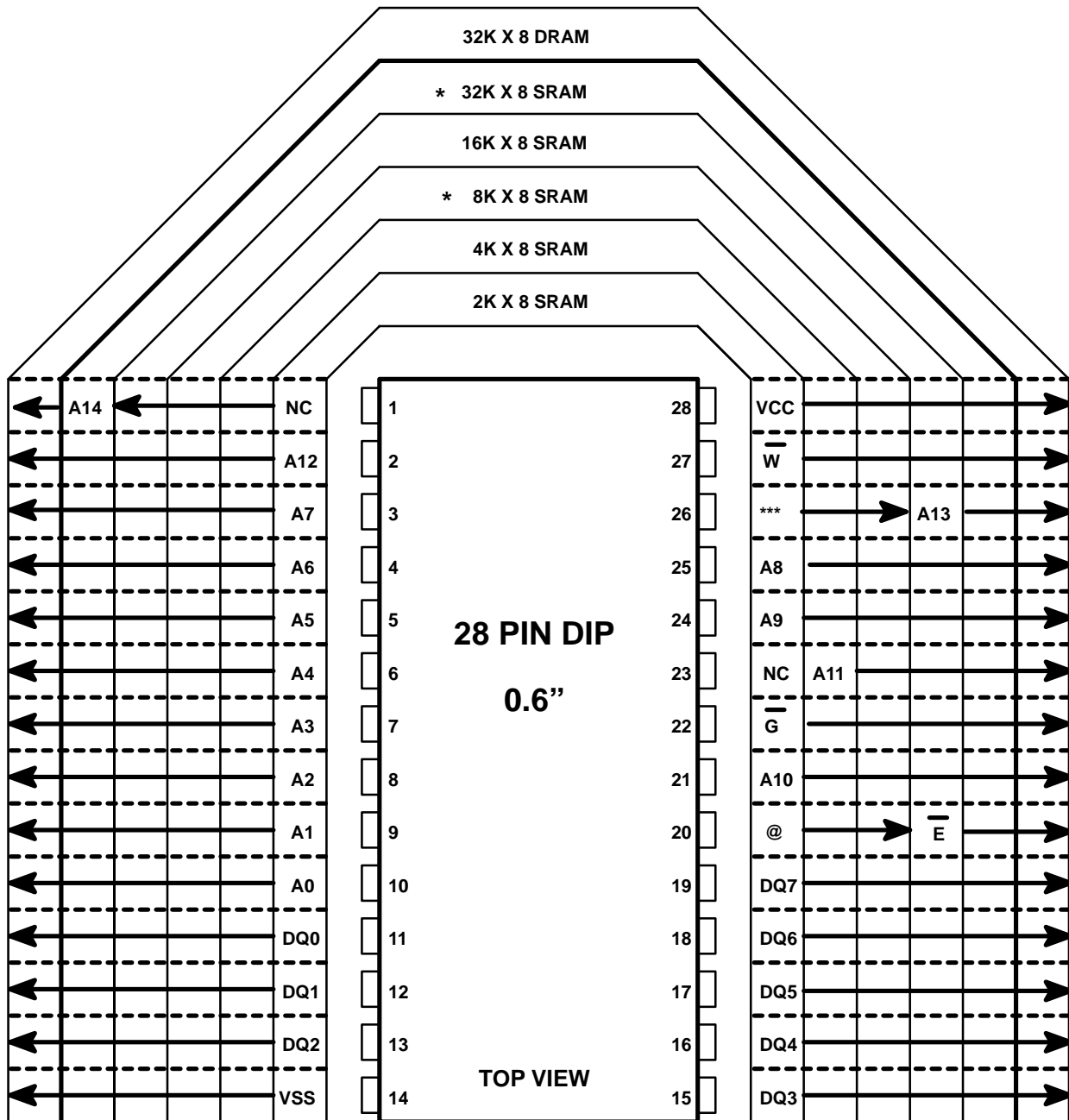
3.9.3.10 – 8M BY 8 DRAM IN USON

CAPACITY—8M WORDS OF 8 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—36 PAD USON, 10 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.3-12



***S or Opt.

@ E or S

* These parts Are also approved in a 0.3" DIP and 0.3" SOJ

FIGURE 3.9.3-1
32K BY 8 DRAM IN DIP

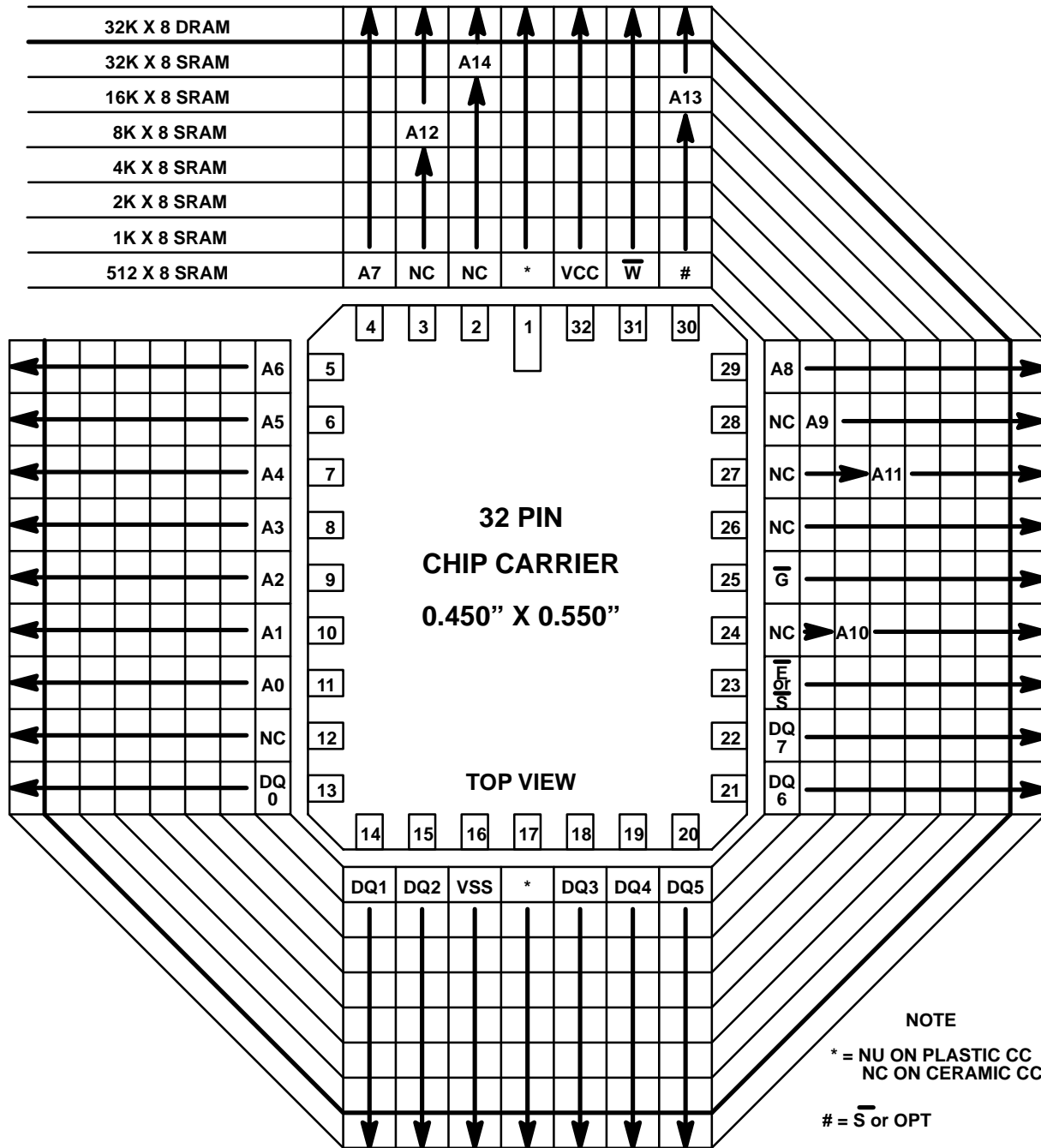


FIGURE 3.9.3-2
32K BY 8 DRAM IN RCC

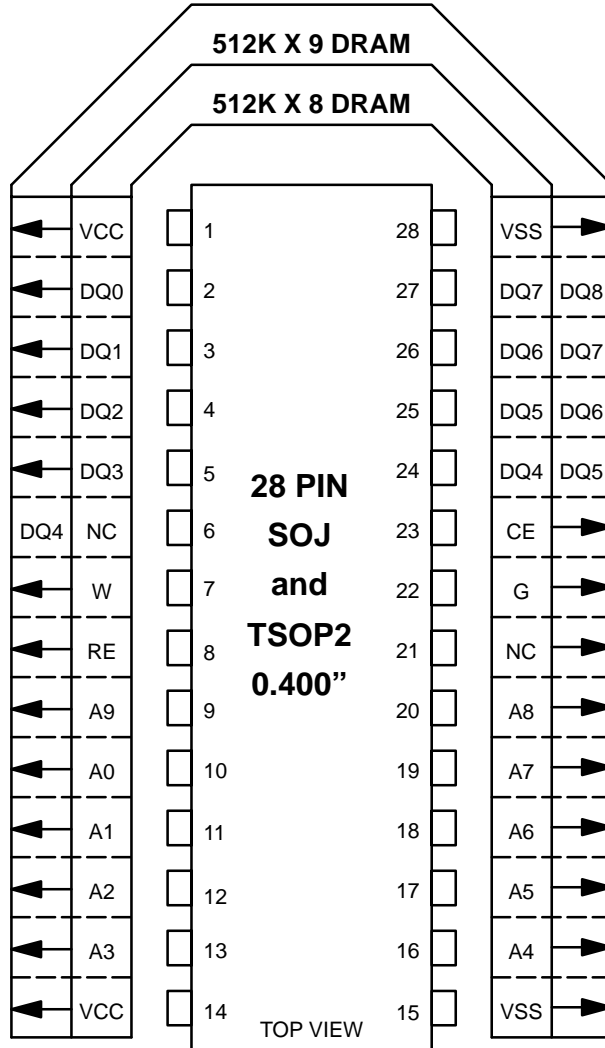


FIGURE 3.9.3-3
512K BY 8 & 9 DRAM IN SOJ

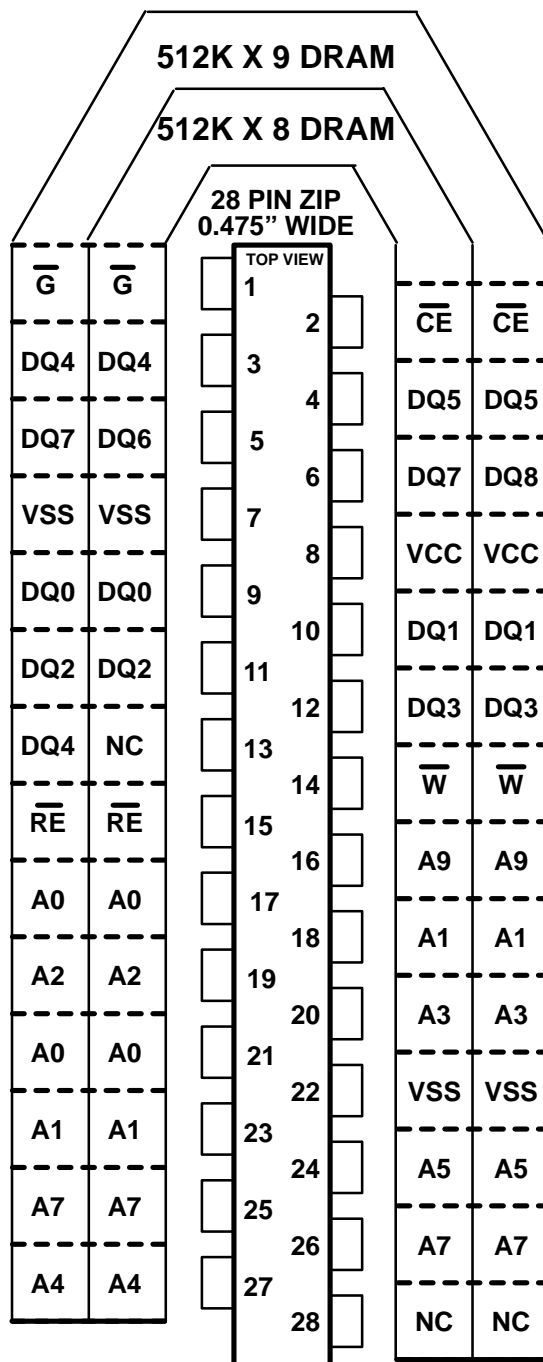
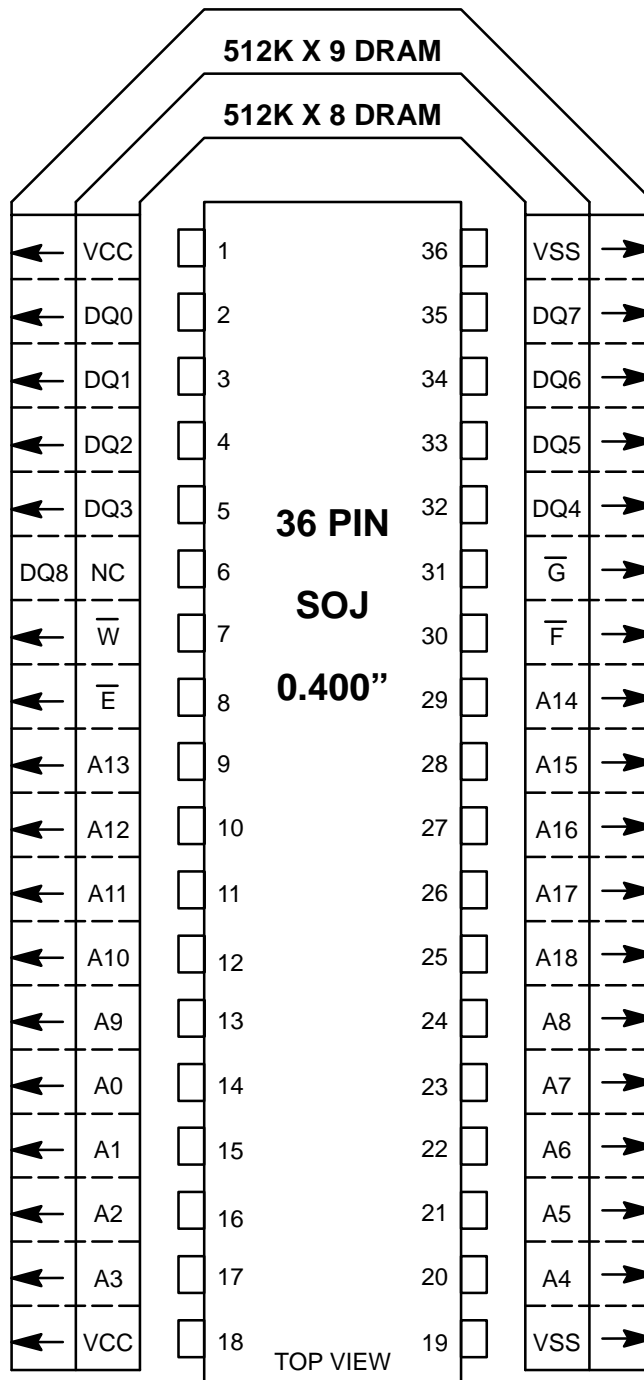


FIGURE 3.9.3-4
 512K BY 8 & 9 DRAM IN ZIP



Refresh address field = A0 THROUGH A9

FIGURE 3.9.3-5
512K BY 8 & 9 NON-MUX DRAM IN SOJ

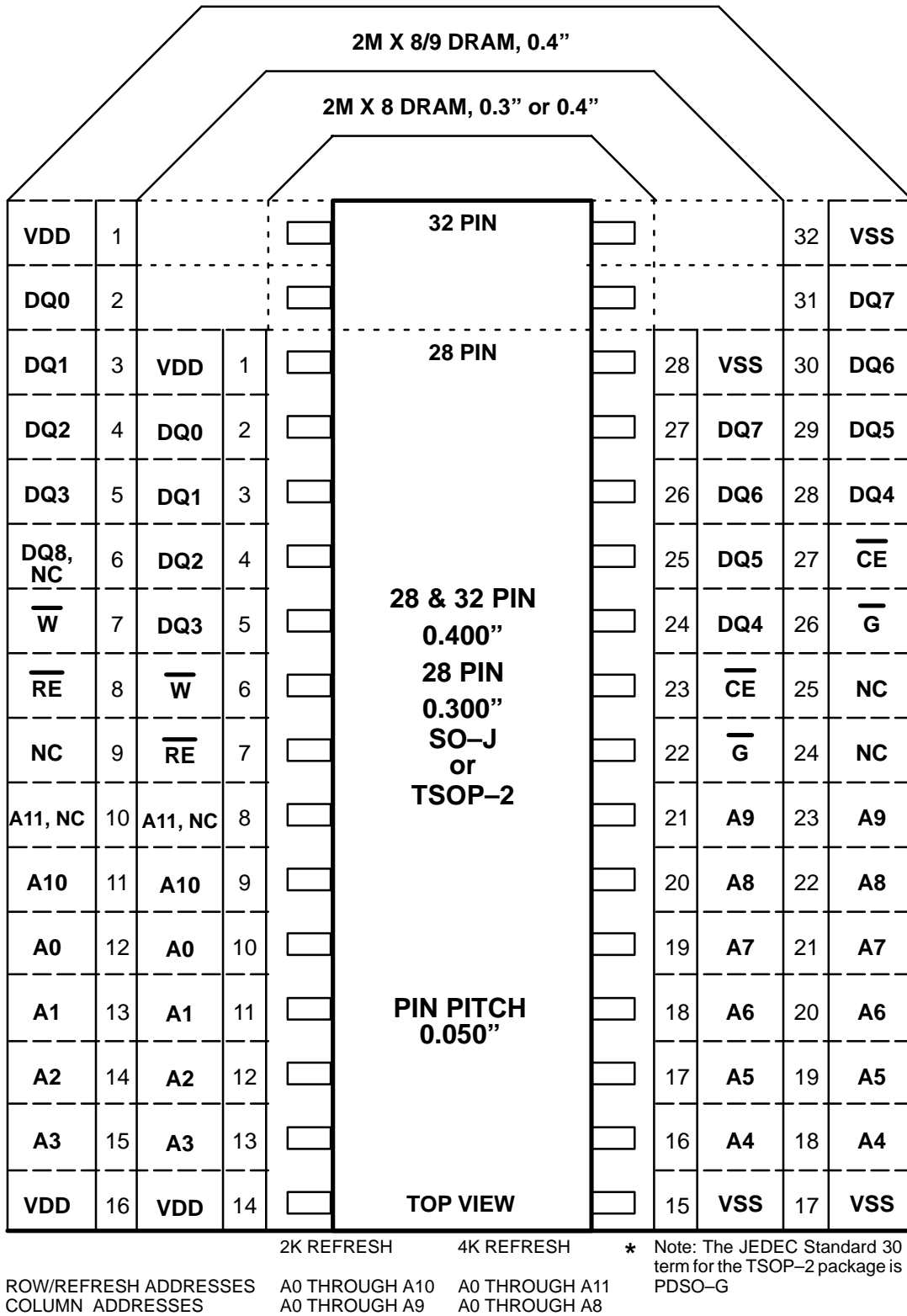
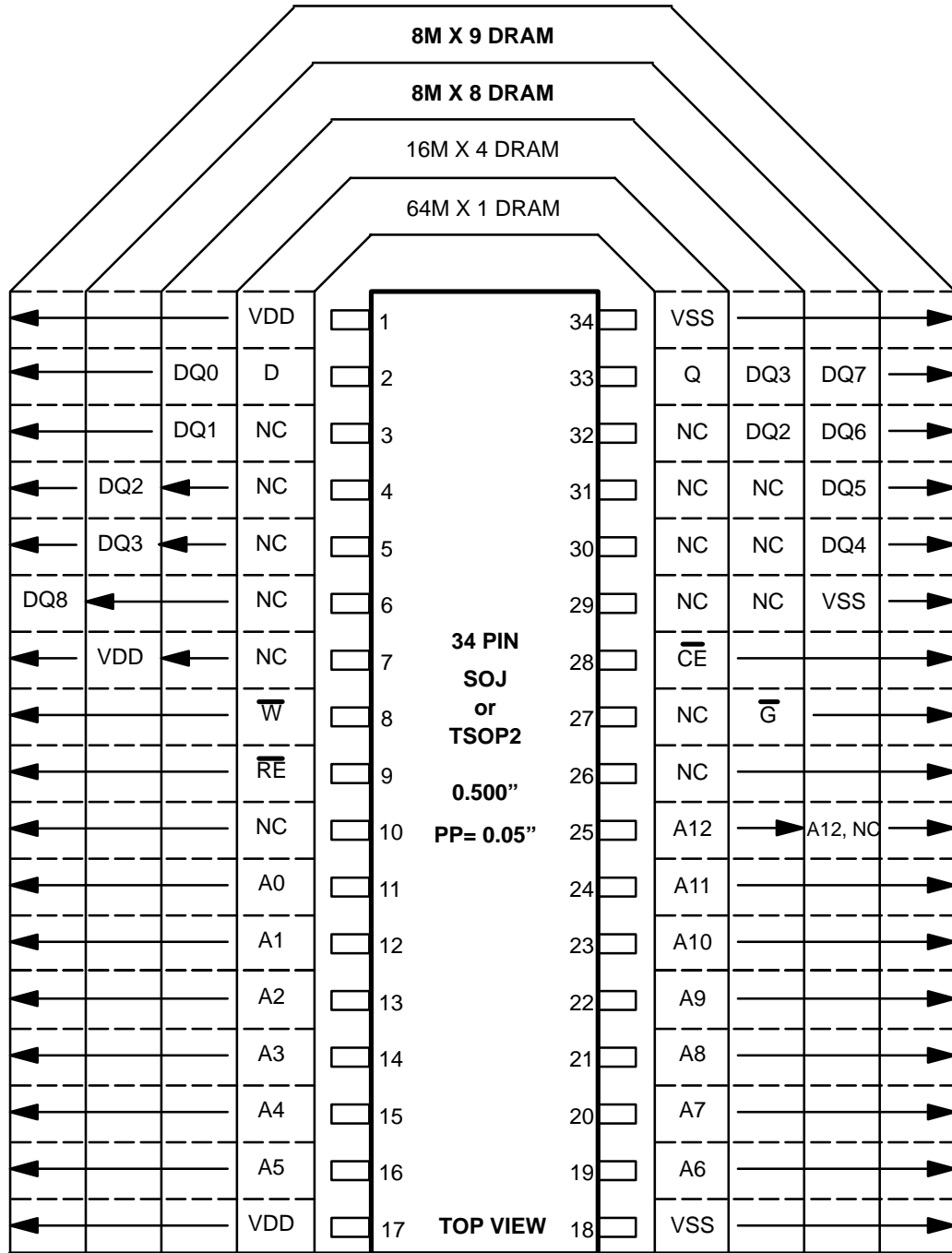


FIGURE 3.9.3-6
2M BY 8 & 9 DRAM IN SOJ & TSOP2

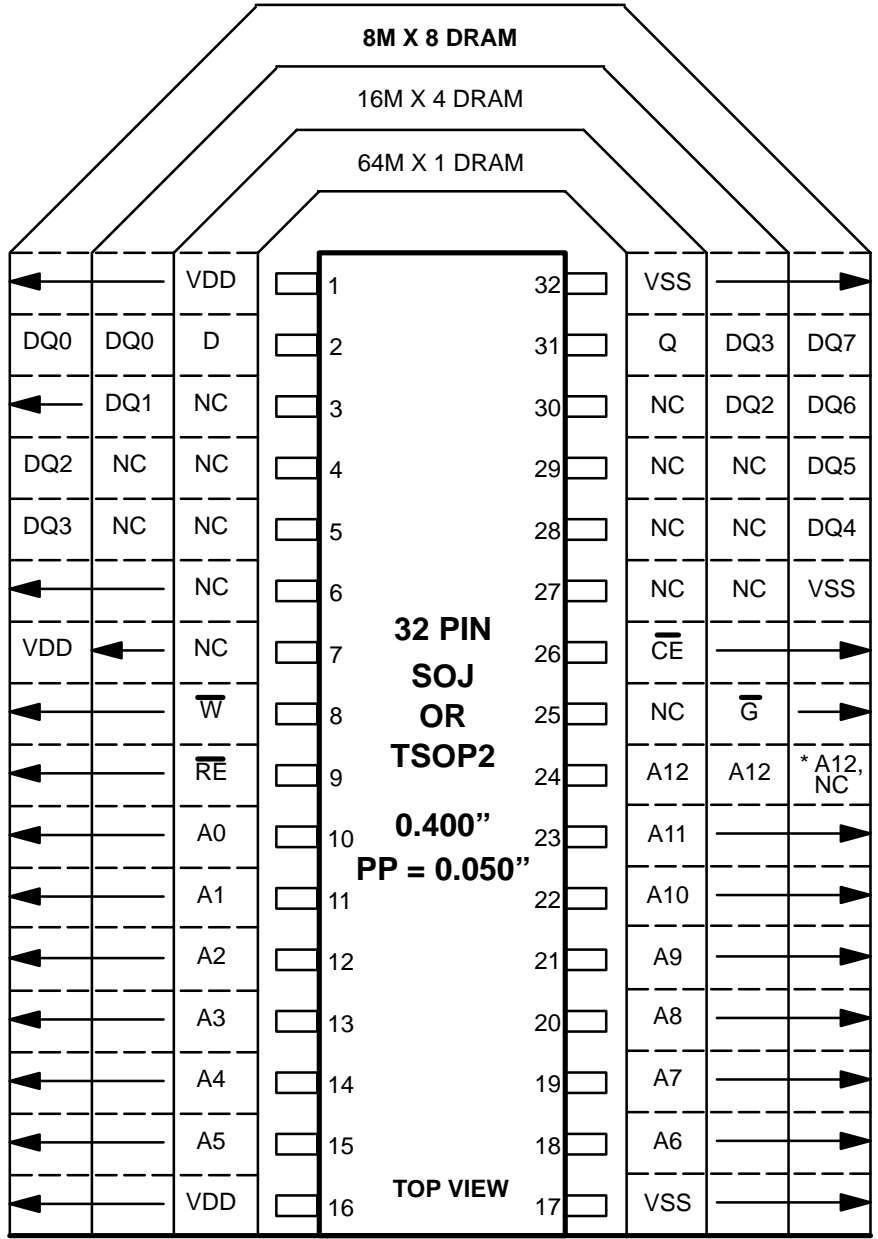


ROW, COLUMN, & REFRESH ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION REFRESH COUNT	64M X 1	16M X 4	8M X 8(9) 4K Refresh	8M X 8(9) 8K Refresh
ROW/REFRESH ADDRESSES	A0 Through A12	A0 Through A12	A0 Through A11	A0 Through A12
COLUMN ADDRESSES	A0 Through A12	A0 Through A10	A0 Through A10	A0 Through A9

This standard recognizes that some early deliveries of these parts may have to be in a 0.6" wide package

FIGURE 3.9.3-7
8M BY 8 & 9 DRAM IN SOJ & TSOP2

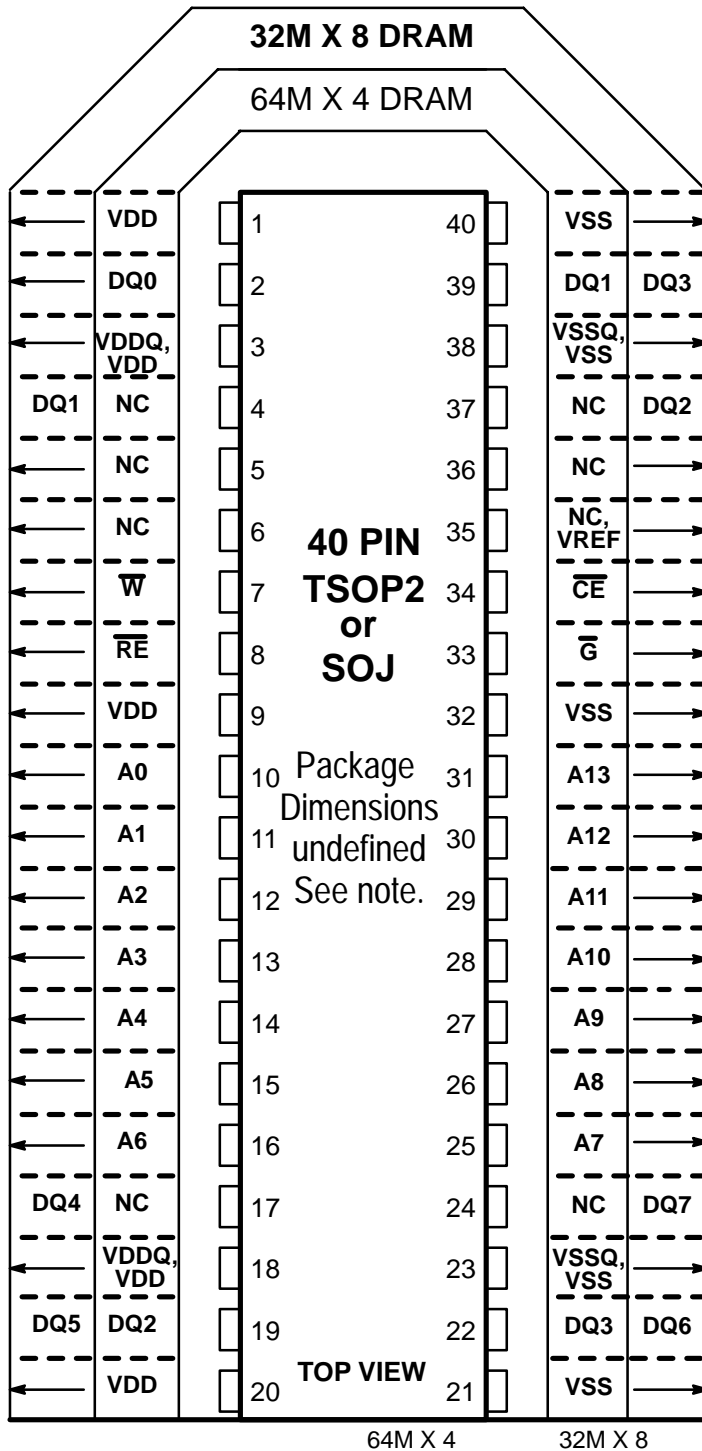


* Pin 24 is NC for the 16M X 4 & 8K X 8 parts with a 4K Refresh.

ROW & COLUMN, ADDRESS CONFIGURATIONS

DEVICE CONFIGURATION	64M X 1	16M X 4	16M X 4	8M X 8	8M X 8
ROW COUNT		4K Rows	8K Rows	4K Rows	8K Rows
ROW ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A12
COLUMN ADDRESSES	A0 ⇒ A12	A0 ⇒ A11	A0 ⇒ A10	A0 ⇒ A10	A0 ⇒ A9

FIGURE 3.9.3-8
8M BY 8 DRAM IN SOJ & TSOP2



NOTES

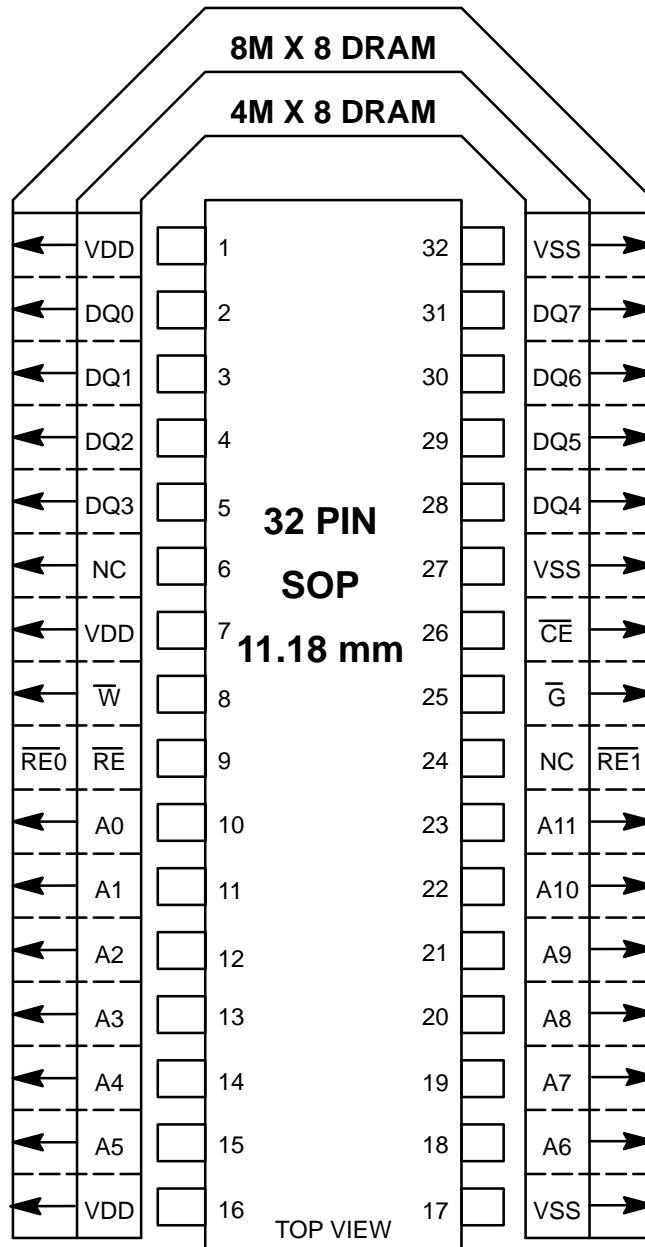
1. Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.
2. CBR refresh is the only standardized method of refreshing non-synchronous DRAMs with densities of 256Mb and higher.
3. The standard refresh interval (tREF) for 256Mb DRAMs is 64ms. (7.8 μs per row with 8K rows, 3.9 μs with 16K rows).
4. (NC, VREF) is VREF on devices that require an external voltage reference.
5. The VDDQ designator is used when the power supply pins for the DQ I/O drivers are internally dc isolated from the other VDD power supply pins.
6. The VSSQ designator is used when the ground reference pins for the DQ I/O drivers are internally isolated from the primary ground references (VSS)

ROW ADDRESSES
COLUMN ADDRESSES

A0 TO A13
A0 TO A11 A0 TO A13
A0 TO A10

Pin numbers and pin count are for reference only. This is a pin rotation only. Package dimensions are not specified at this stage.

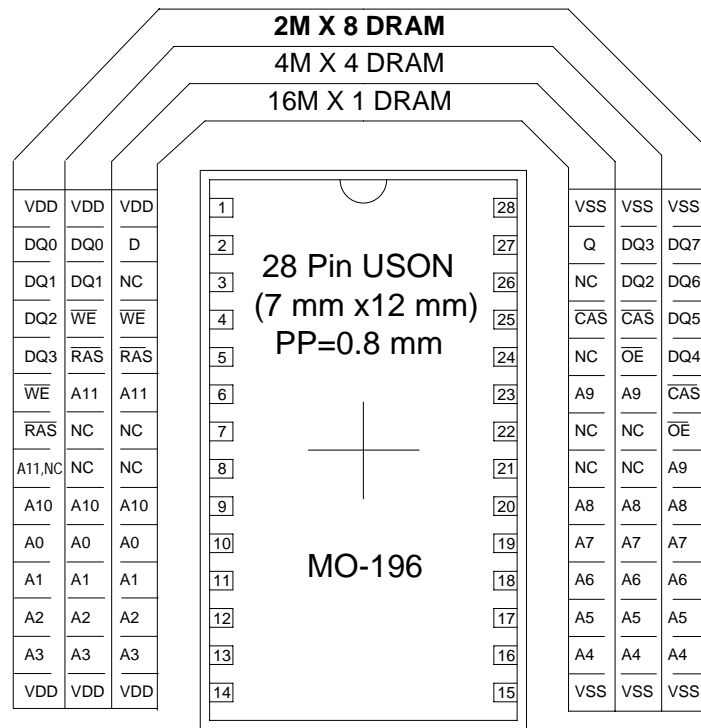
FIGURE 3.9.3-9
32M BY 8 DRAM PIN ROTATION IN TSOP2



Row, Column, & Address Configuration

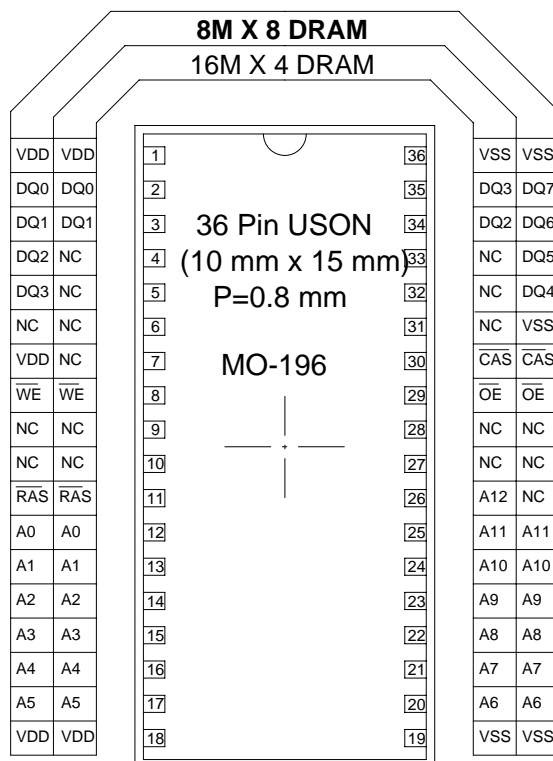
Device Configuration	4M X 8	8M X 8
Refresh Count	4K	4K
Row/Refresh Addresses	A0⇒A11	A0⇒A11
Column Addresses	A0⇒A9	A0⇒A9

FIGURE 3.9.3-10
4M & 8M BY 8 DRAM IN SOP



Organization	16M x 1	4M x 4	2M x 8 (2K Refresh)	2M x 8 (4K Refresh)
Row Address	A0 to A11	A0 to A11	A0 to A10	A0 to A11
Column Address	A0 to A11	A0 to A9	A0 to A9	A0 to A8

FIGURE 3.9.3-11
2M BY 8 DRAM IN USON



Organization	16M x 4	8M x 8
Row Address	A0 to A12	A0 to A11
Column Address	A0 to A10	A0 to A10

FIGURE 3.9.3-12
8M BY 8 DRAM IN USON