

3.7.6 Byte Wide ECL SRAM

All of the following standards are for devices which operate with ECL interface levels and power voltages.

3.7.6.1 – 32K and 128K BY 8 ECL SSRAM IN SOJ, SSOP, AND FP

CAPACITY—32K, & 128K WORDS OF 8 BIT

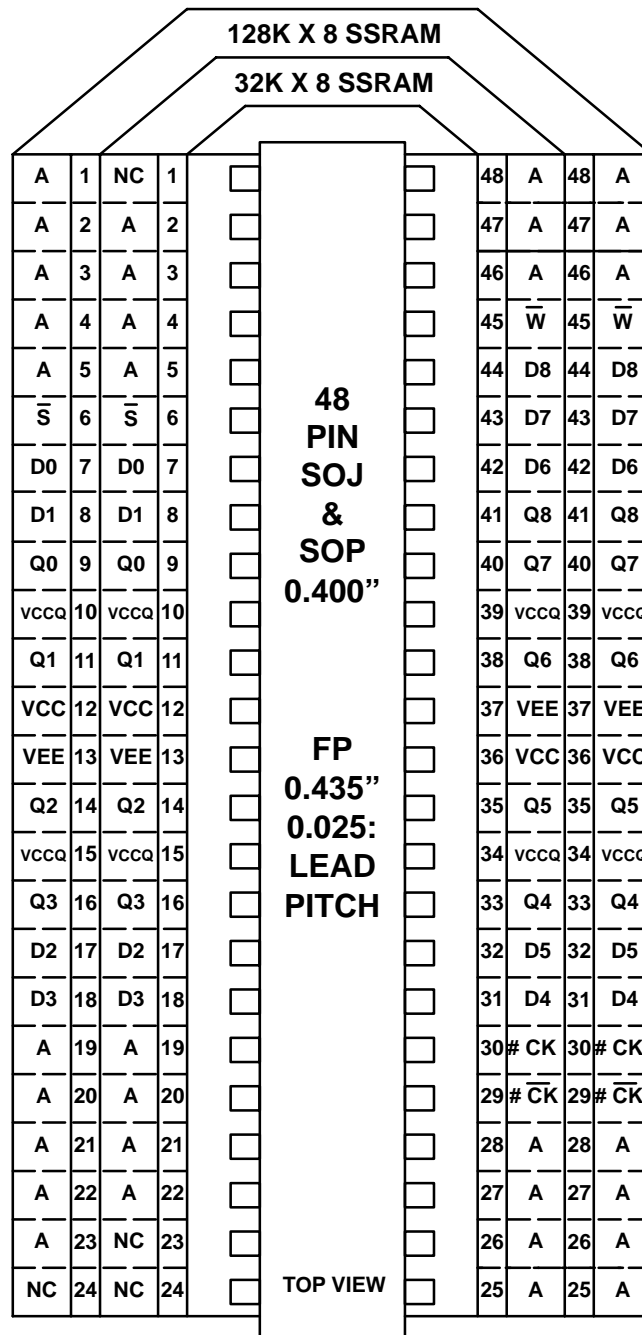
LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS

PACKAGE—48 PIN SOJ & SSOP, 0.4" wide

—48 PIN FP, 0.435 WIDE, 0.025" LEAD PITCH

SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS AND EXTRA GROUNDS

PIN ASSIGNMENT—Fig. 3.7.6-1



The Clock pins may be either C, K, CK or L as a manufacturer option.
These parts are approved for use with 10K, 100K, or 101K interface.

FIGURE 3.7.6-1
32K AND 256K BY 9 ECL SSRAM IN SOJ, SOP, AND FP