

3.7.5 Byte Wide TTL and MOS SRAM

All of the following standards are for devices which operate with TTL or MOS interface levels and power voltages.

3.7.5.1 - 64 BY 9 TTL SRAM IN SCC

CAPACITY--64 WORDS OF 9 BITS
PACKAGE--28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS--Fig. 3.7.5-1
This standard was developed by Committee 42.1.

3.7.5.2 - 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY--1K, 2K WORDS OF 8 BITS
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.7.5-2

3.7.5.3 - 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY--2K, 4K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.5-3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 - 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY--2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE--28 PIN DIP, 0.6" WIDE
--28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT--Fig. 3.7.5-4

3.7.5.5 - .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY--.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.5-5

3.7.5.6 - 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP-2,

CAPACITY--32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
--32 PIN TSOP-2 (see Fig. 3.7.5-6 for package approvals)
PIN ASSIGNMENT--Fig. 3.7.5-6

3.7.5.7 - 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY--64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.7.5-7

3.7.5.8 - 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY--32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
--OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT--Fig. 3.7.5-8

3.7.5.9 - 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP-2

CAPACITY--32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
--OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE--32, 36, or 40 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
--32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES--MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT--Fig. 3.7.5-9

3.7.5.10 - 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY--32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
--OUTPUT ENABLE
PACKAGE--40 PIN DIP, 0.6" wide
--40 PIN SOJ, UNDEFINED
SPECIAL FEATURES--MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT--Fig. 3.7.5-10

3.7.5.11 - 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY--2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES--Two identical access ports
PACKAGE--68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT--Fig. 3.7.5-11

This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 - 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY--32K WORDS OF 9 BITS,
LOGIC FEATURES--Internal CACHE data compare logic
PACKAGE--44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT--Fig. 3.7.5-12

This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 - 128K BY 8 SRAM IN TSOP1

CAPACITY--128K WORDS OF 8 BITS
PACKAGE--32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS--Fig. 3.7.5-13

3.7.5.14 - 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY--128K WORDS OF 8 BITS
PACKAGE--32 PIN SOJ, 0.400"
PIN ASSIGNMENTS--Fig. 3.7.5-14

3.7.5.15 - 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY--1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES--Two identical access ports
PACKAGE--48 PIN DIP, 0.600"
PIN ASSIGNMENT--Fig. 3.7.5-15

This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 - 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO-N

CAPACITY--128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT--Fig. 3.7.5-16

This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 - 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY--128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES--Both Synchronous and Asynchronous versions of the 128K part
PACKAGE--36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
-- See Fig. 3.7.5-17 for specific package approvals and dimensions.
PIN ASSIGNMENT--Fig. 3.7.5-17

3.7.5.18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY--128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.5-18
These parts contain BURST addressing capability.

3.7.5.19 - 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY--128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,
PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.5-19
Included with this standard is a table of the BOUNDARY SCAN ORDER to be used in testing the parts.
BOUNDARY SCAN ORDER TABLE--Fig. 3.7.5-20

3.7.5.20 - 32K BY 8 SRAM IN TSOP1

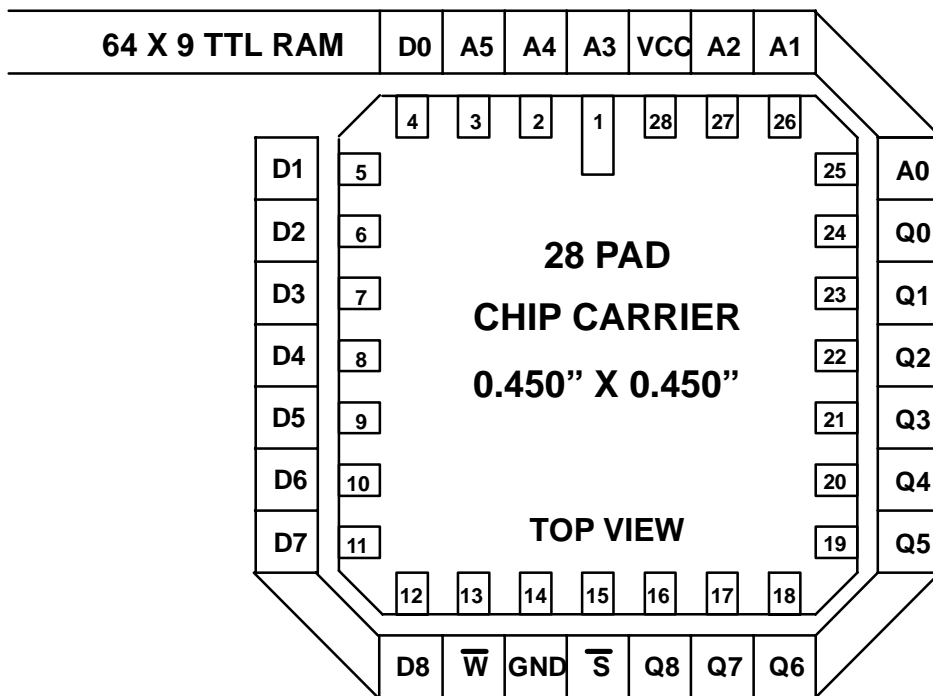
CAPACITY--32K WORDS OF 8 BITS
PACKAGE--32 PIN TSOP1, 8 mm X 11.8 mm, 0.55 mm PP
PIN ASSIGNMENTS--Fig. 3.7.5-21

3.7.5.21 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 209 BGA

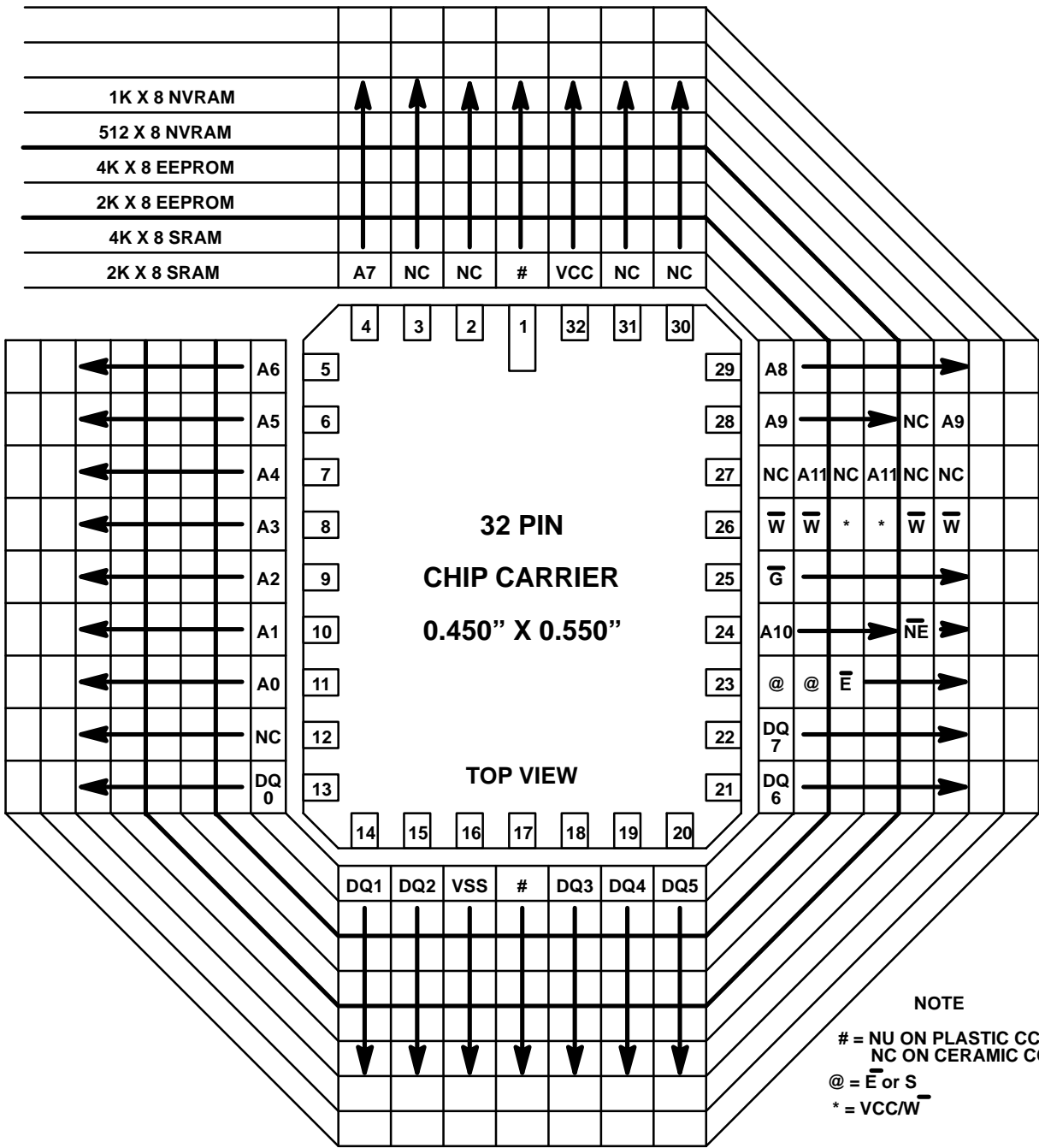
CAPACITY--128K, 256k, 512k, 1M, 2M, 4M, 8M, 16M WORDS OF 9 BITS
PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm, 1 mm Bump Pitch
PIN ASSIGNMENTS--Fig. 3.7.5-22

3.7.5.22 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 221 BGA

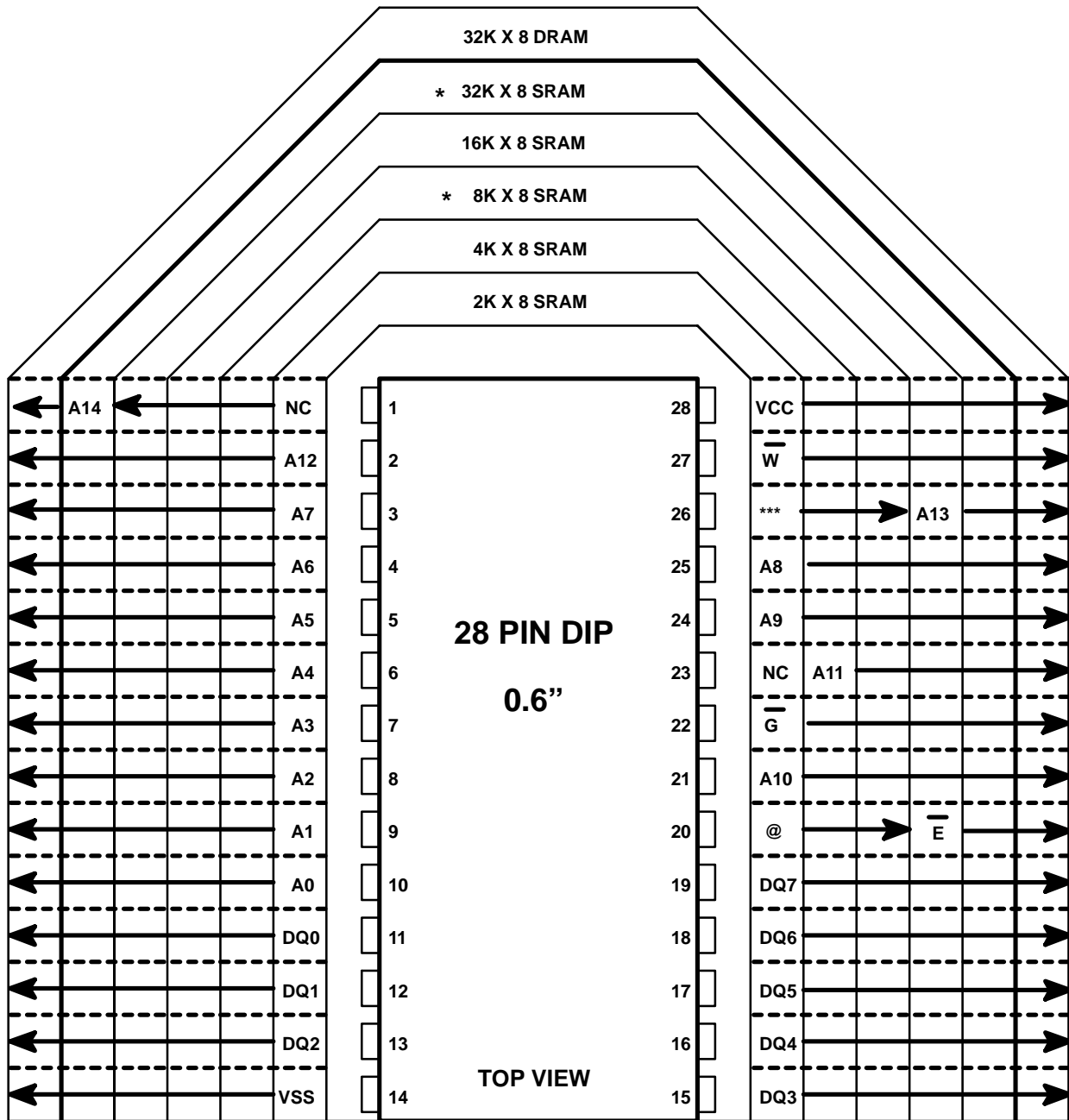
CAPACITY--128K, 256k, 512k, 1M, 2M, 4M, 8M, 16M WORDS OF 9 BITS
PACKAGE--13 X 17 BALL BGA 13 mm X 15 mm, 0.8 mm Bump Pitch
PIN ASSIGNMENTS--Fig. 3.7.5-23



**FIGURE 3.7.5-1
64 BY 9 SRAM IN SCC**



**FIGURE 3.7.5-3
2K & 4K BY 8 TTL SRAM IN RCC**



***S or Opt.

@ E or S

* These parts Are also approved in a 0.3" DIP and 0.3" SOJ

FIGURE 3.7.5-4
2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ

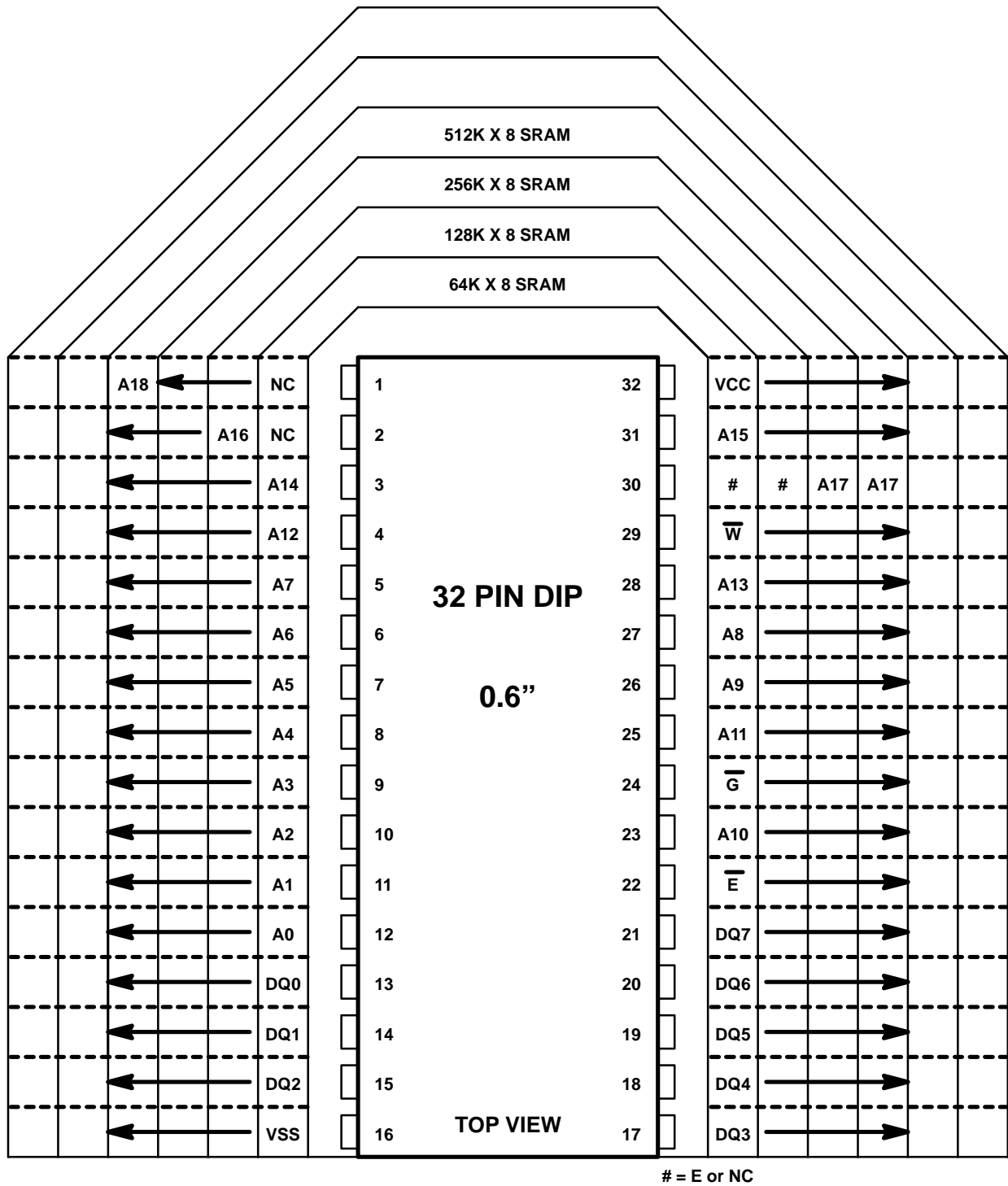
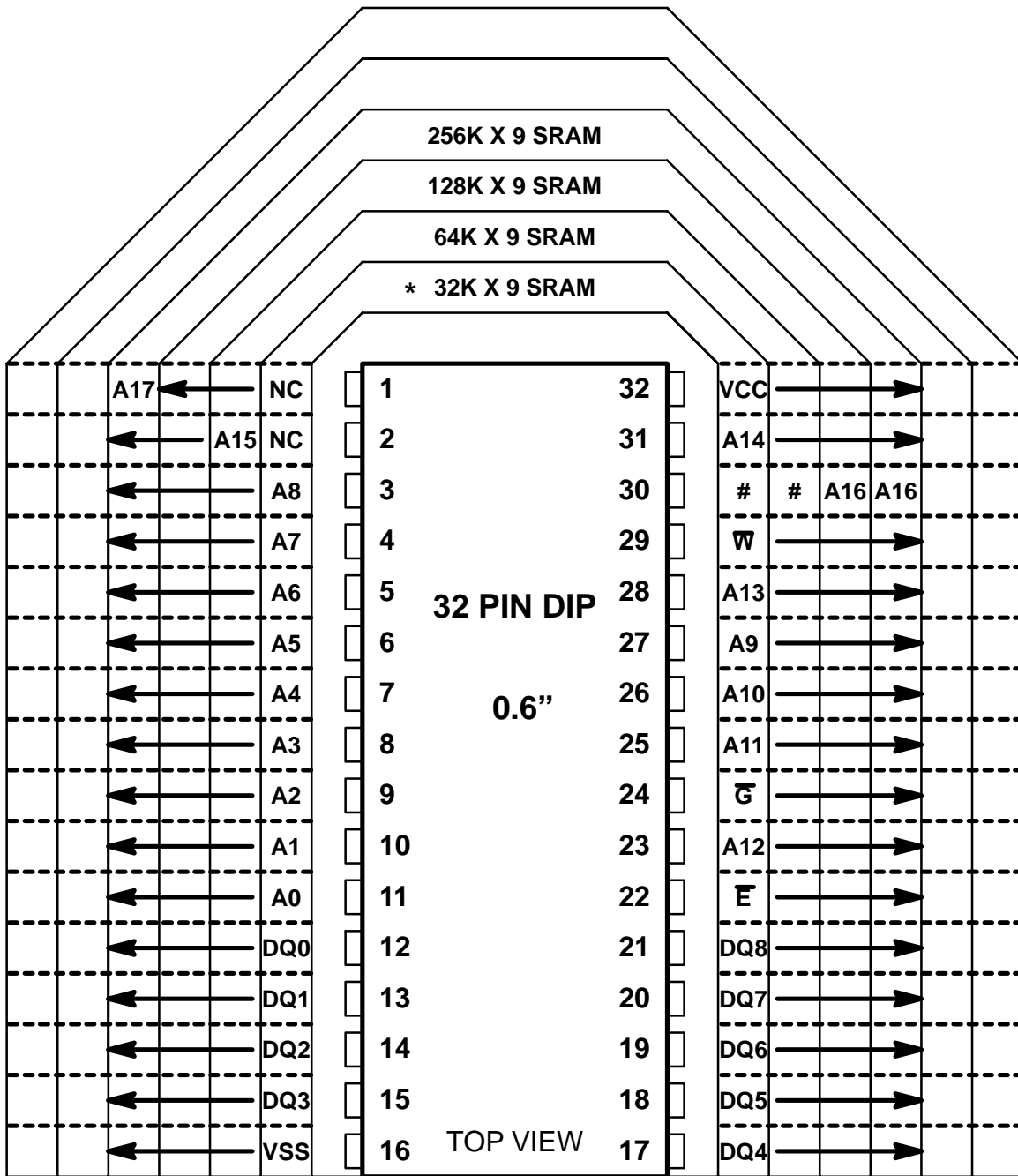


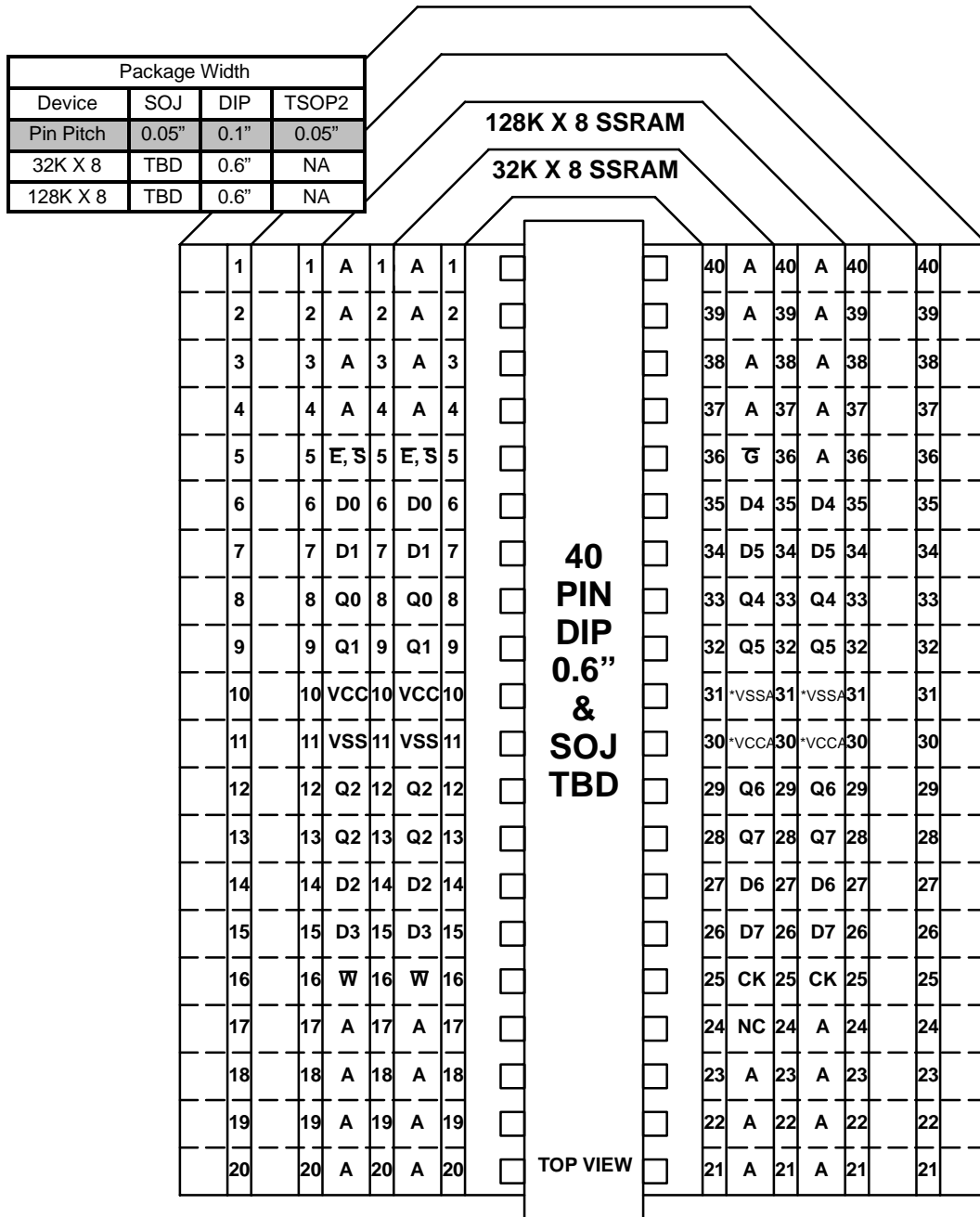
FIGURE 3.7.5-7
64K TO 512K BY 8 TTL SRAM FAMILY IN DIP



= E or NC

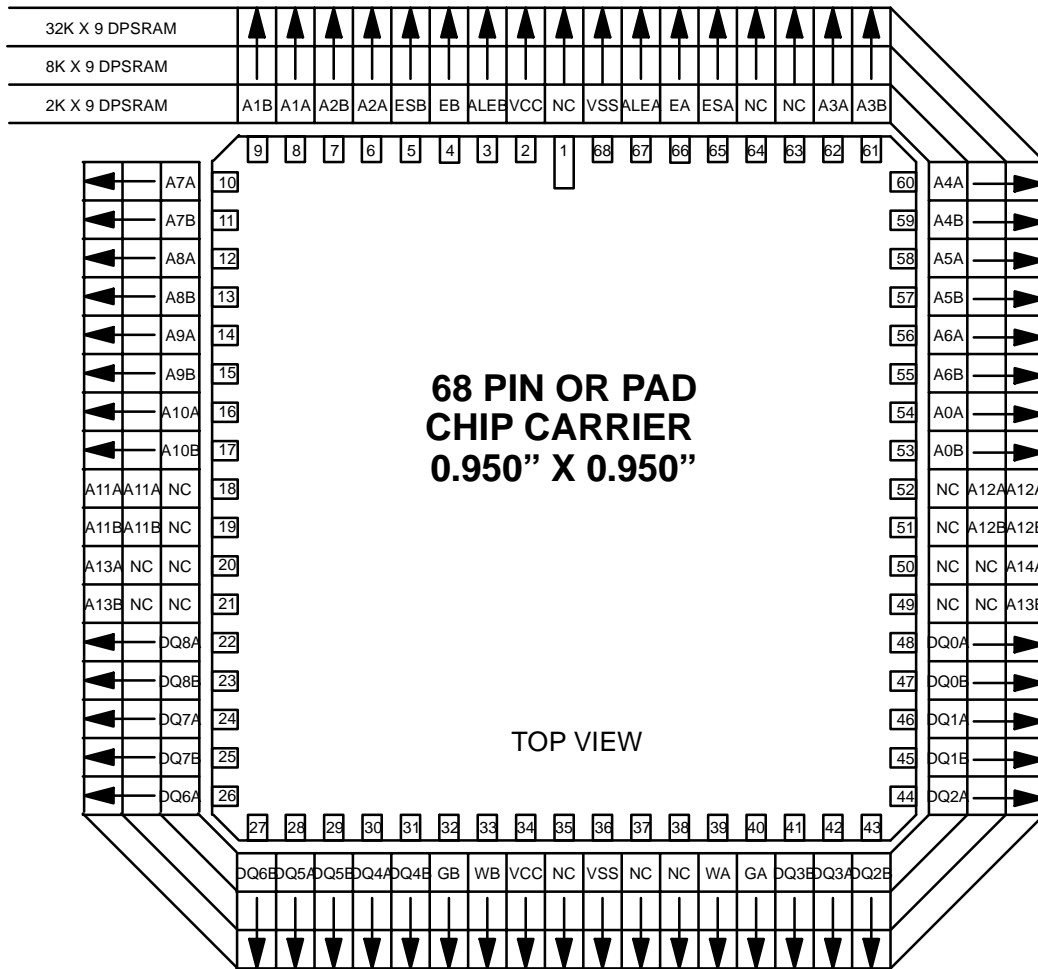
* This part is approved also with 0.3" DIP and 0.3" SOJ

FIGURE 3.7.5-8
32K TO 256K BY 9 TTL SRAM FAMILY IN DIP

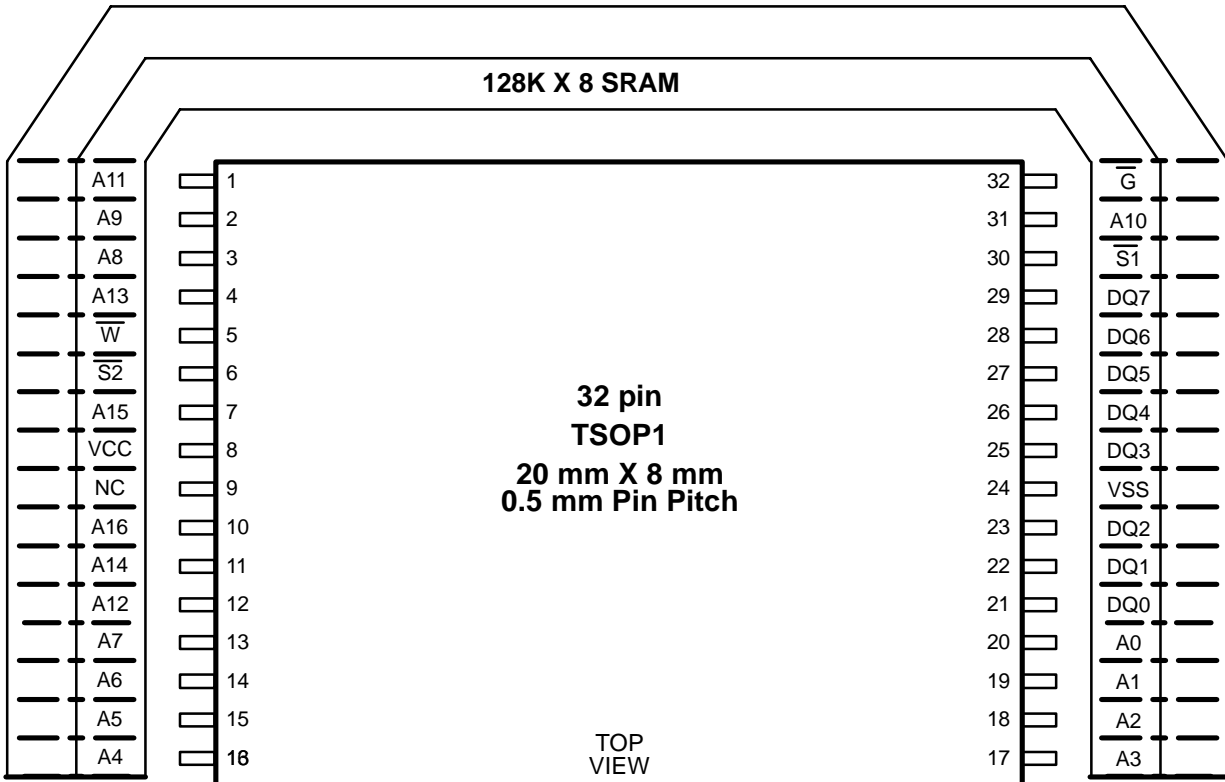


* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.5-10
32K AND 128K BY 8 TTL SSRAM IN DIP, TSOP2, AND SOJ



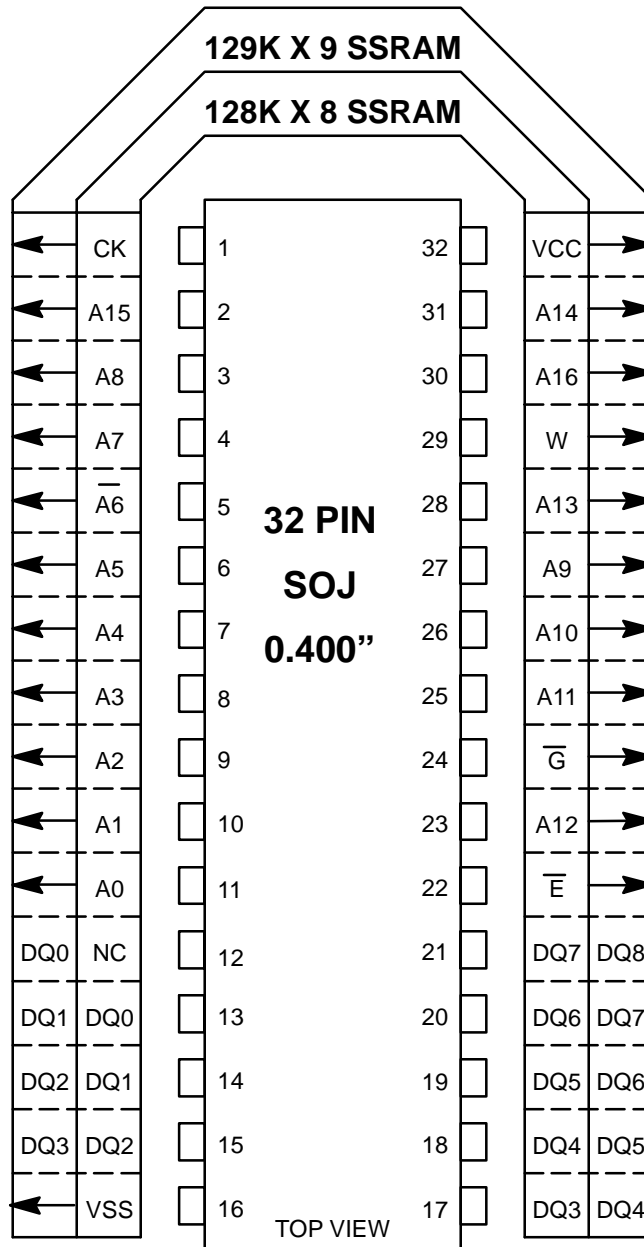
**FIGURE 3.7.5-11
2K TO 32K BY 9 DPSRAM FAMILY IN SCC**



The JEDEC Std. No 30 designator for the TSOP1 package is PDSO-G

Correct pp 14 & 15.

**FIGURE 3.7.5-13
128K BY 8 SRAM IN TSOP1**



All INPUTS and OUTPUTS can be either registered or latched

FIGURE 3.7.5-14
128K BY 8 & 9 TTL SSRAM IN SOJ

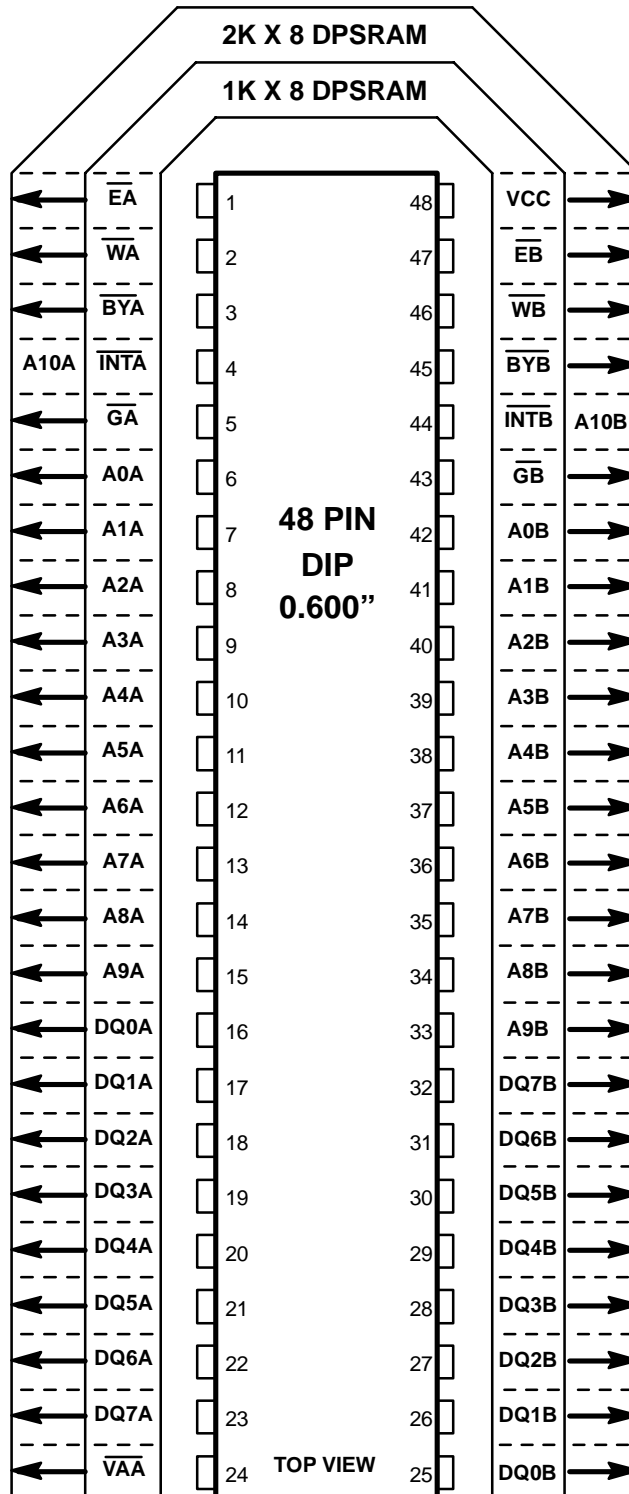


FIGURE 3.7.5-15A
1K AND 2K BY 9 DPSRAM IN DIP

1K & 2K BY 8 DPSRAM TRUTH TABLE

INPUTS			BYA	BYB	FUNCTION
EA	EB	A0A-A9A A0B-A9B	When used as an output	When used as an output	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	h	MATCH	H	H	Normal
L	L	MATCH	L if EA and A0A-A9A Are stable prior to EB and A0B-A9B ⁽²⁾	L if EB and A0B-A9B are stable prior to EA and A0A-A9A ⁽²⁾	Write inhibit ⁽³⁾

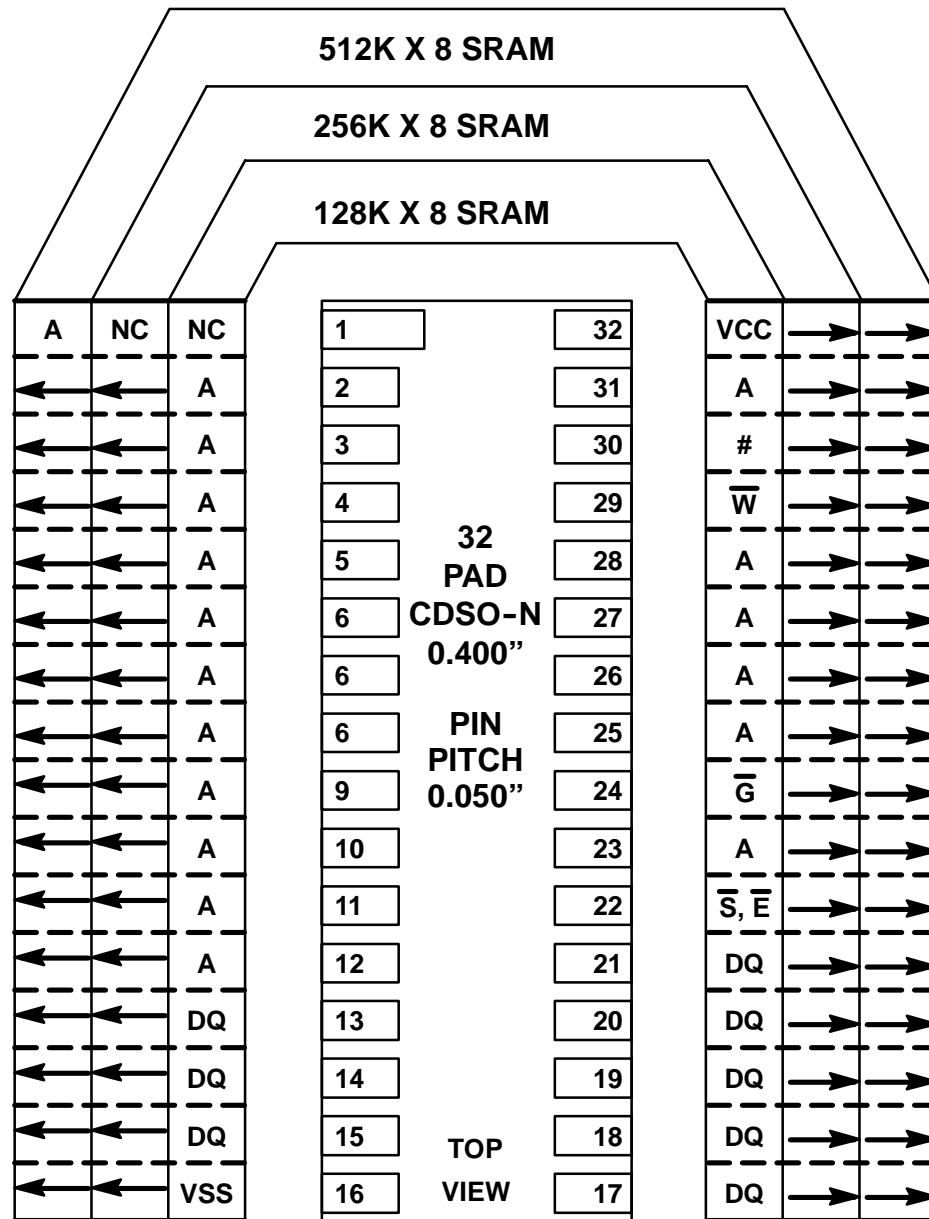
1. Pins BYA and BYB are wither both inputs or both outputs depending on the part type. When used as inputs, BYx gates Wx. Wx internal - Wx OR NOT BYx. BYx outputs are open drain outputs.
2. If the primacy of stable inputs cannot be resolved, either BYA = low or BYB = low, will result. BYA and BYB outputs cannot be low simultaneously.
3. Writes to port A are internally ignored when BYA outputs are driving low regardless of actual logic level on the pin. Writes to port B are internally ignored when BYB outputs are driving low regardless of actual logic level on the pin.

1K BY 8 DPSRAM FUNCTION TABLE

PORT A INPUTS				PORT B INPUTS						FUNCTION
WA	EA	GA	A0A-A9A	WB	EB	GB	A0B-A9B	INTA	INTB	
L	L	X	3FF	X	X	X	X	X	L(1)	SET INTB F-F
X	X	X	X	X	L	L	3FF	X	H	RESET INTB F-F
X	X	X	X	L	L	X	3FF	L(1)	X	SET INTA F-F
X	L	L	3FE	X	X	X	X	H	X	RESET INTA F-F

1. Interrupt B will not be set if BYA is low when WA is low. Interrupt A will not be set if BYB is low when WB is low. Interrupt outputs are open drain.

FIGURE 3.7.5-15B
1K AND 2K BY 9 DPSRAM TRUTH TABLE



NOTE: CDSO-N is the JEDEC Standard 30 term for a LEADLESS CERAMIC SO Package

FIGURE 3.7.5-16
128K TO 512K BY 8 SRAM IN CDSO-N

Package Width			
Device	SOJ	DIP	TSOP2
Pin Pitch	0.05"	0.1"	0.05"
128K X 8/9	0.4"	0.4"	NA
Pin Pitch	0.05"	0.07"	0.05"
512K X 8/9	0.4"	0.6"	0.4"

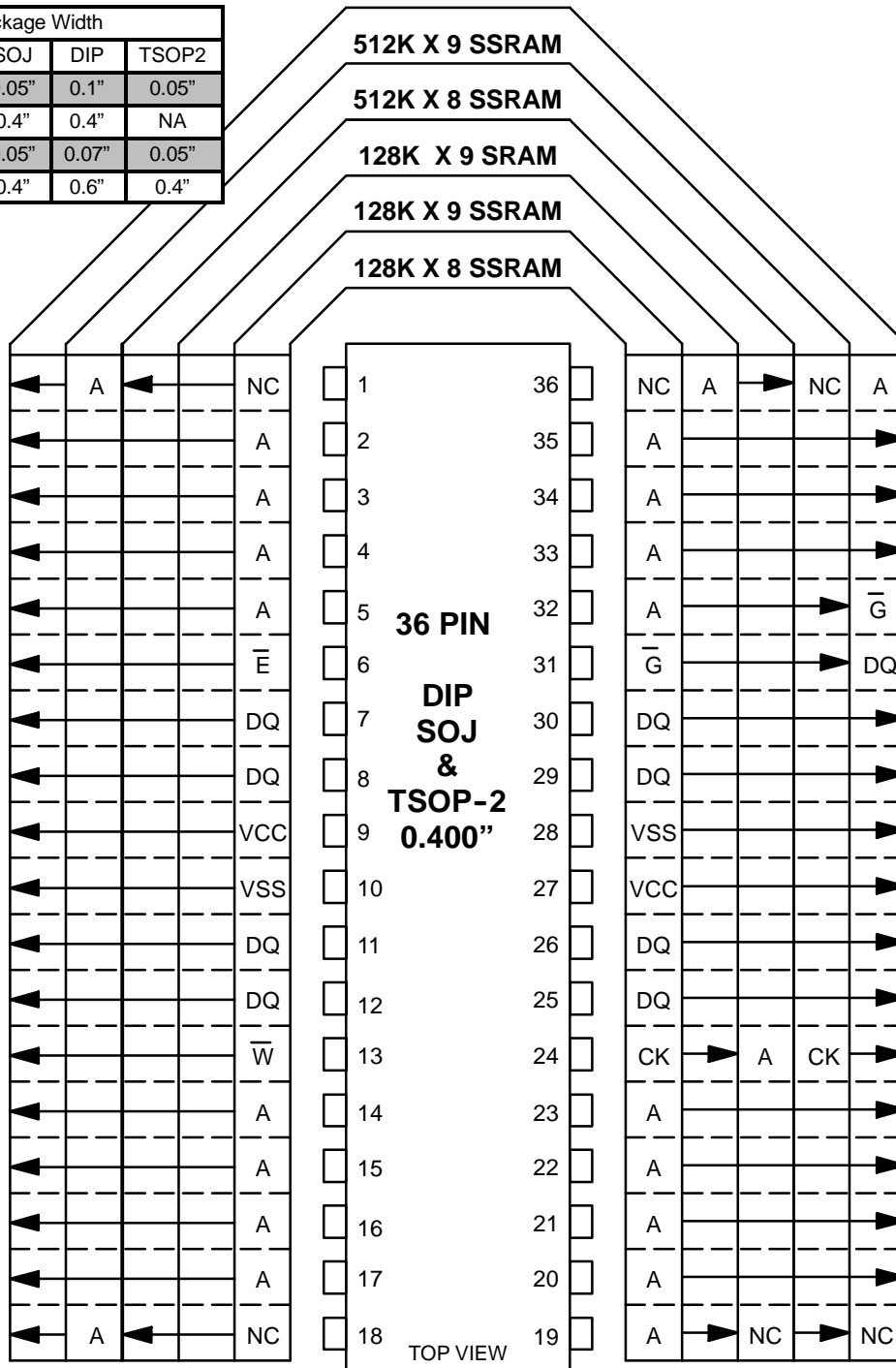


FIGURE 3.7.5-17

128K AND 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN DIP, TSOP2, & SOJ

Burst SRAM Ball Grid Array (BGA) Package Ball Assignments, Top View							
X9	1	2	3	4	5	6	7
A	VDDQ	SA	SA	\overline{SAP}	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA~	\overline{SAC}	NC, SA*	NC, $\overline{SE2}$,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	NC	NC	VSS	NC, ZQ	VSS	NC	NC
E	NC	NC	VSS	\overline{SS} , \overline{SE}	VSS	NC	DQ, NC
F	VDDQ	NC	VSS	\overline{G}	VSS	NC	VDDQ
G	NC	DQ	VSS	\overline{SADV}	VSS	NC	DQ
H	DQ	NC	VSS	NC	VSS	DQ	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQ	VSS	CK, K	VSS	NC	DQ
L	DQ	NC	VSS	\overline{CK} , \overline{K} , NC	VSS	DQ	NC
M	VDDQ	NC	VSS	\overline{SW}	VSS	NC	VDDQ
N	NC	NC	VSS	SA1	VSS	NC	NC
P	NC	NC	VSS	SA0	VSS	NC	NC
R	NC	SA	\overline{LBO}	VDD	\overline{FT}	SA	NC
T	NC	SA	SA	SA	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

Address Assignment and Package Dimension Table		
Density	Address Assignment	Nominal Exterior Package Dimension
1M (128K X 9)	Basic SA	14 mm X 22 mm
2M (256K X 9)	~	14 mm X 22 mm
4M (512K X 9)	~, *	14 mm X 22 mm
8M (1M X 9)	~, *, ◇	TBD
16 M (2M X 9)	~, *, ◇, #	TBD

FIGURE 3.7.5-18
128K TO 2M BY 8/9 BURST SRAM IN BGA

Synchronous SRAM Ball Grid Array (BGA) Package Ball Assignments, Top View							
X9	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC,SE2,SA#	NC, SA~	NC	NC, SA*	NC,SE2,SA◇	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	NC	NC	VSS	NC, ZQ	VSS	NC	NC
E	NC	NC	VSS	$\overline{SS}, \overline{SE}$	VSS	NC	DQ, NC
F	VDDQ	NC	VSS	$\overline{G}, \overline{SG}$	VSS	NC	VDDQ
G	NC	DQ	VSS	NC, \overline{C}	VSS	NC	DQ
H	DQ	NC	VSS	NC, C	VSS	DQ	NC
J	VDDQ	VDD	VREF, NC	VDD	VREF, NC	VDD	VDDQ
K	NC	DQ	VSS	CK, K	VSS	NC	DQ
L	DQ	NC	VSS	$\overline{CK}, \overline{K}, NC$	VSS	DQ	NC
M	VDDQ	NC	VSS	\overline{SW}	VSS	NC	VDDQ
N	NC	NC	VSS	SA	VSS	NC	NC
P	NC	NC	VSS	SA	VSS	NC	NC
R	NC	SA	M1, NC	VDD	M2, NC	SA	NC
T	NC	SA	SA	SA	SA	SA	ZZ, NC
U	VDDQ	TMS, NC	TDI, NC	TCK, NC	TDO, NC	NC, TRST	VDDQ

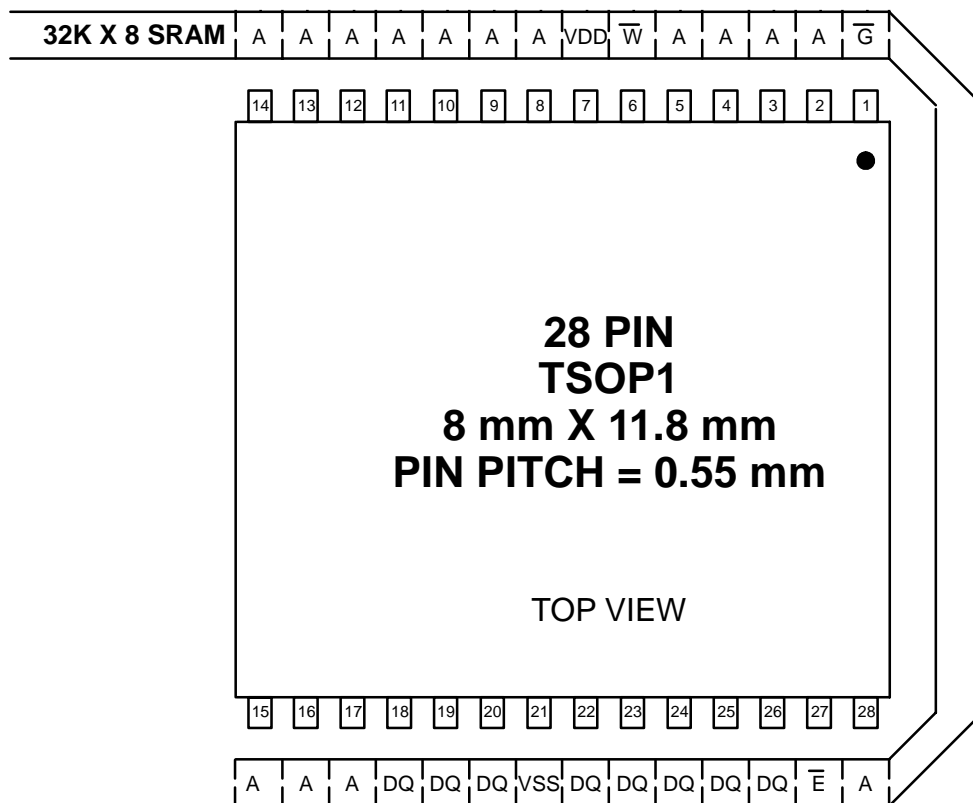
Address Assignment and Package Dimension Table		
Density	Address Assignment	Nominal Exterior Package Dimension
1M (128K X 9)	Basic SA	14 mm X 22 mm
2M (256K X 9)	~	14 mm X 22 mm
4M 512K X 9)	~, *	14 mm X 22 mm
8M (1M X 9)	~, *, ◇	TBD
16 M (2M X 9)	~, *, ◇, #	TBD

Mode Truth Table	M1	M2
Single Clock, Register Flow Through	VSS	VSS
Single Clock, Register-Register	VSS	VDD
Single Clock, Register-Latch	VDD	VSS
Dual Clock	VDD	VDD

FIGURE 3.7.5-19
128K TO 2M BY 8/9 SSRAM IN BGA

SSRAM Boundry Scan Order						
X9 Part						
Exit Order	Signal	Ball #		Exit Order	Signal	Ball #
1	M2, NC	5R		22	NC, SA~	3B
2	SA	6T		23	NC, SE2 SA#	2B
3	SA	4P		24	SA	3A
4	SA	4T		25	SA	3C
5	SA	6R		26	SA	2C
6	SA	5T		27	SA	2A
7	NC, ZZ	7T				
				28	DQ	2G
8	DQ	6L				
				29	DQ	1H
9	DQ	7K				
				30	ZQ, NC	4D
10	\bar{K} , NC	4L		31	\bar{SS}	4E
11	K	4K		32	\bar{C} , NC	4G
12	\bar{G}	4F		33	C, NC	4H
				34	\bar{SW}	4M
13	DQ	6H				
14	DQ	7G		35	DQ	2K
				36	DQ	1L
15	DQ, NC	7E				
16	SA	6A				
17	SA	6C		37	SA	3T
18	SA	5C		38	SA	2R
18	SA	5A		39	SA	4N
20	NC, SE2 SA◇	6B		40	SA	2T
21	NC, SA*	5B		41	M1, NC	3R

FIGURE 3.7.5-20
128K TO 2M BY 8/9 SSRAM IN BGA BOUNDRY SCAN ORDER



**FIGURE 3.7.5-21
 32K BY 8 SRAM IN TSOP-1**

x9 Separate I/O Sigma SRAM Pinout - Top View

	1	2	3	4	5	6	7	8	9	10	11
A	D1	D2	A	E2	A, NC (16M)	ADV, MCL	A, NC (8M)	E3	A	NC	NC
B	D3	D4	NC	NC	A	\overline{W}	A	NC	NC	NC	NC
C	D5	D6	NC	NC	A, NC (128M)	$\overline{E1}, \overline{R}$	A	A	NC	NC	NC
D	D7	D8	VSS, VSSQ	NC, VREF	NC	\overline{G}, MCL	NC	NC, VREF	VSS, VSSQ	NC	NC
E	D9	Q1	VDD, VDDQ	VDD, VDDQ	VDD	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
F	Q3	Q2	VSS, VSSQ	VSS, VSSQ	VSS	MCL, ZQ	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
G	Q5	Q4	VDD, VDDQ	VDD, VDDQ	VDD	MCH, EP2	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
H	Q7	Q6	VSS, VSSQ	VSS, VSSQ	VSS	MCL, EP3	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
J	Q9	Q8	VDD, VDDQ	VDD, VDDQ	VDD	M4	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
K	NC, CQ	NC, CQ	CK	NC, \overline{CK}	VSS	MCL, \overline{CKE}	VSS	\overline{C}, NC	C, NC	NC	NC
L	NC	NC	VDD, VDDQ	VDD, VDDQ	VDD	M2	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
M	NC	NC	VSS, VSSQ	VSS, VSSQ	VSS	M3	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
N	NC	NC	VDD, VDDQ	VDD, VDDQ	VDD	MCH, \overline{SD}	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
P	NC	NC	VSS, VSSQ	VSS, VSSQ	VSS	MCL, ZZ	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
R	NC	NC	VDD, VDDQ	VDD, VDDQ	VDD	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
T	NC	NC	VSS, VSSQ	NC, VREF	NC	MCL, \overline{LBO}	NC	NC, VREF	VSS, VSSQ	NC	NC
U	NC	NC	NC	A	A, NC (64M)	A	A, NC (32M)	A	NC	NC	NC
V	NC	NC	A, NC (2M)	A	A	A1	A	A	A, NC (4M)	NC	NC
W	NC	NC	NC, TMS	NC, TDI	A	A0	A	NC, TDO	NC, TCK	NC	NC
11 x 19 Array BGA - 14 mm x 22 mm Body - 1 mm Ball Pitch - MS-028vBC											

FIGURE 3.7.5-22
1Mb - 128Mb (x9) Sync Separate I/O SRAM in 209 BGA

x9 Separate I/O Sigma SRAM Pinout - Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	D1	D2	VSS, VSSQ	A	E2	A, NC (16M)	ADV, MCL	A, NC (8M)	E3	A	VSS, VSSQ	NC	NC
B	D3	D4	VDD, VDDQ	NC	NC	A	\overline{W}	A	NC	NC	VDD, VDDQ	NC	NC
C	D5	D6	VSS, VSSQ	NC	NC	A, NC (128M)	$\overline{E1}, \overline{R}$	A	A	NC	VSS, VSSQ	NC	NC
D	D7	D8	D9	VDD, VDDQ	NC, VREF	NC	\overline{C} , MCL	NC	NC, VREF	VDD, VDDQ	NC	NC	NC
E	Q3	Q2	Q1	VSS, VSSQ	VSS, VSSQ	VSS	MCL, ZQ	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC	NC
F	Q5	Q4	VDD, VDDQ	VDD, VDDQ	VDD	VDD	MCH, EP2	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
G	Q7	Q6	VSS, VSSQ	VSS, VSSQ	VSS	VSS	MCL, EP3	VSS	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
H	Q9	Q8	VDD, VDDQ	VDD, VDDQ	VDD	VDD	M4	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
J	NC, CQ	NC, \overline{CQ}	CK	NC, \overline{CK}	VSS, VSSQ	VSS	MCL, \overline{CKE}	VSS	VSS, VSSQ	\overline{C} , NC	C, NC	NC	NC
K	NC	NC	VDD, VDDQ	VDD, VDDQ	VDD	VDD	M2	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
L	NC	NC	VSS, VSSQ	VSS, VSSQ	VSS	VSS	M3	VSS	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC
M	NC	NC	VDD, VDDQ	VDD, VDDQ	VDD	VDD	MCH, \overline{SD}	VDD	VDD	VDD, VDDQ	VDD, VDDQ	NC	NC
N	NC	NC	NC	VSS, VSSQ	VSS, VSSQ	VSS	MCL, ZZ	VSS	VSS, VSSQ	VSS, VSSQ	NC	NC	NC
P	NC	NC	NC	VDD, VDDQ	NC, VREF	NC	MCL, \overline{LBO}	NC	NC, VREF	VDD, VDDQ	NC	NC	NC
R	NC	NC	VSS, VSSQ	NC	A	A, NC (64M)	A	A, NC (32M)	A	NC	VSS, VSSQ	NC	NC
T	NC	NC	VDD, VDDQ	A, NC (2M)	A	A	A1	A	A	A, NC (4M)	VDD, VDDQ	NC	NC
U	NC	NC	VSS, VSSQ	NC, TMS	NC, TDI	A	A0	A	NC, TDO	NC, TCK	VSS, VSSQ	NC	NC
13 x 17 Bump BGA - 13 x 15 mm2 Body - 0.8 mm Bump Pitch - MO-210vAK													

FIGURE 3.7.5-23
1Mb - 128Mb (x9) Sync Separate I/O SRAM in 221 BGA