

### **3.7.4 Nibble Wide ECL SRAM**

All of the following standards are for devices which operate with ECL interface levels and power voltages.



#### 3.7.4.1 – .25K AND 1K BY 4, 100K ECL SRAM IN DIP AND SFP

CAPACITY—256, WORDS OF 4 BITS  
ELECTRICAL INTERFACE—100K ECL  
There are two versions of this part: one in SFP and the other in DIP  
PACKAGE—24 PIN DIP, 0.4" WIDE  
PIN ASSIGNMENT—Fig. 3.7.4-1  
PACKAGE—24 PIN SFP, 0.380" BY 0.380"  
PIN ASSIGNMENT—Fig. 3.7.4-2  
This standard was developed by Committee 42.1.

#### 3.7.4.2 – 1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP

CAPACITY—1K, 4K, & 16K, WORDS OF 4 BITS  
ELECTRICAL INTERFACE—10K or 100K ECL  
—USES 100K ECL CENTERED POWER PINS  
PACKAGE—1K in 24 PIN DIP, 0.4" WIDE  
—4K & 16K in 28 PIN DIP, 0.4" WIDE  
PIN ASSIGNMENT—Fig. 3.7.4-1  
This standard was developed by Committee 42.1.

#### 3.7.4.3 – .25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP

CAPACITY—256, 1K, 4K, 16K WORDS OF 4 BITS  
ELECTRICAL INTERFACE—10K ECL  
—USES 10K ECL CORNERED POWER PINS  
—4K part, also 100K ECL  
PACKAGE—.25K & 1K, 24 PIN DIP, 0.4" WIDE  
—4K & 16K, 28 PIN DIP, 0.4" WIDE  
PIN ASSIGNMENT—Fig. 3.7.4-4  
This standard was developed by Committee 42.1.

#### 3.7.4.4 – 16K BY 4, 10K & 100K ECL SSRAM IN DIP

CAPACITY—16K, WORDS OF 4 BITS  
ELECTRICAL INTERFACE—10K or 100K ECL  
—USES 100K ECL CENTERED POWER PINS  
PACKAGE—32 PIN DIP, 0.4" WIDE  
THESE DEVICES CONTAIN BUILT IN WRITE CYCLE TIMING  
PIN ASSIGNMENT—Fig. 3.7.4-5  
This standard was developed by Committee 42.1.

#### 3.7.4.5 – 64K TO 4M BY 4 ECL SRAM IN DIP, SOJ, AND TSOP-2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURE—COMMON DATA INPUT & OUTPUT PINS  
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES  
ELECTRICAL INTERFACE—ECL  
PACKAGE—28, 32, or 36 PIN SOJ, & TSOP-2, 0.3", 0.4" or 0.5" WIDE with PP=0.05"  
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-6

#### 3.7.4.6 – 64K TO 4M BY 4 ECL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES  
ELECTRICAL INTERFACE—ECL  
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP-2, 0.3", 0.4" or 0.5" WIDE with PP=0.05"  
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—MULTIPLE CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-7

■ **3.7.4.7 – 64K TO 4M BY 4 ECL SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2**

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
—OUTPUT ENABLE FOR ALL DENSITIES  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"  
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-8

■ **3.7.4.8 – 64K BY 4 ECL SRAM IN FP**

CAPACITY—64K WORDS OF 4 BITS  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—28 PIN FP, 0.535" WIDE, 0.030" LEAD PITCH  
PIN ASSIGNMENT—Fig. 3.7.4-9

■ **3.7.4.9 – 256K BY 4/512K BY 2 RECONFIGURABLE SRAM IN DIP & SOJ**

CAPACITY—256K WORDS OF 4 BITS OR 512K WORDS OF 2 BITS  
LOGIC FEATURES—RECONFIGURABLE CAPACITY & DATA INTERFACE  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—32 PIN DIP or SOJ, 0.4" wide  
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-10

■ **3.7.4.10 – 64K TO 4M BY 4 SRAM FAMILY IN DIP AND SOJ IN DIP, SOJ, AND TSOP-2**

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
—BIT SELECTION  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—36 or 40 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"  
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-11

■ **3.7.4.11 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2**

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
—DIFFERENTIAL CLOCKS  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—32, 36, or 40 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"  
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-12

■ **3.7.4.12 – 64K TO 4M BY 4 SSRAM FAMILY IN SIP AND SOJ IN DIP, SOJ, AND TSOP-2**

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT  
LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS  
—BIT SELECTION  
ELECTRICAL INTERFACE—10K or 100K ECL  
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP2, 0.3", 0.4", or 0.5" wide  
—36, 40, or 44 PIN DIP, 0.3", 0.4", or 0.6" wide..  
PACKAGE—36, 40, or 44 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"  
—36 or 40 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".  
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS  
PIN ASSIGNMENT—Fig. 3.7.4-13

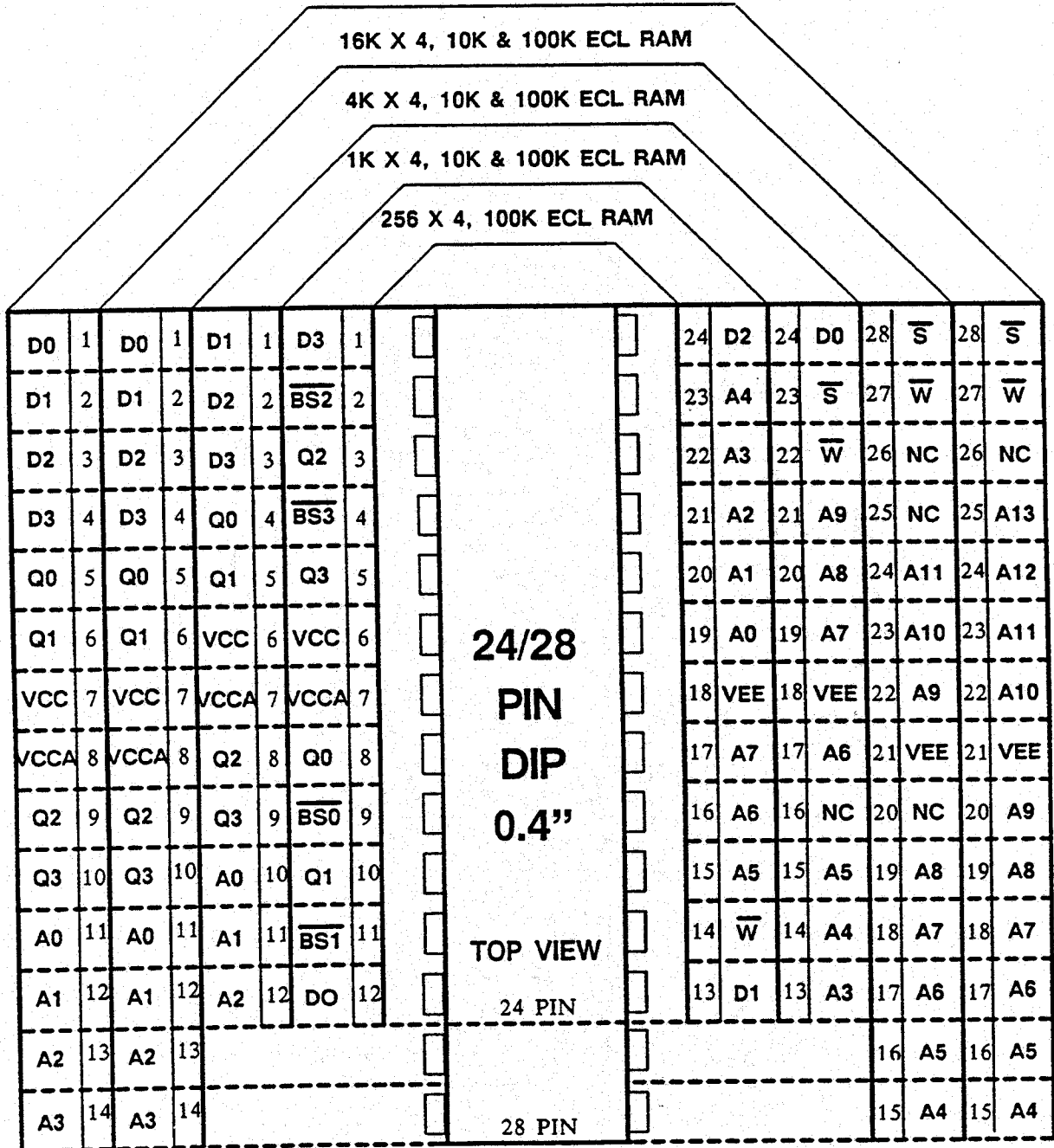
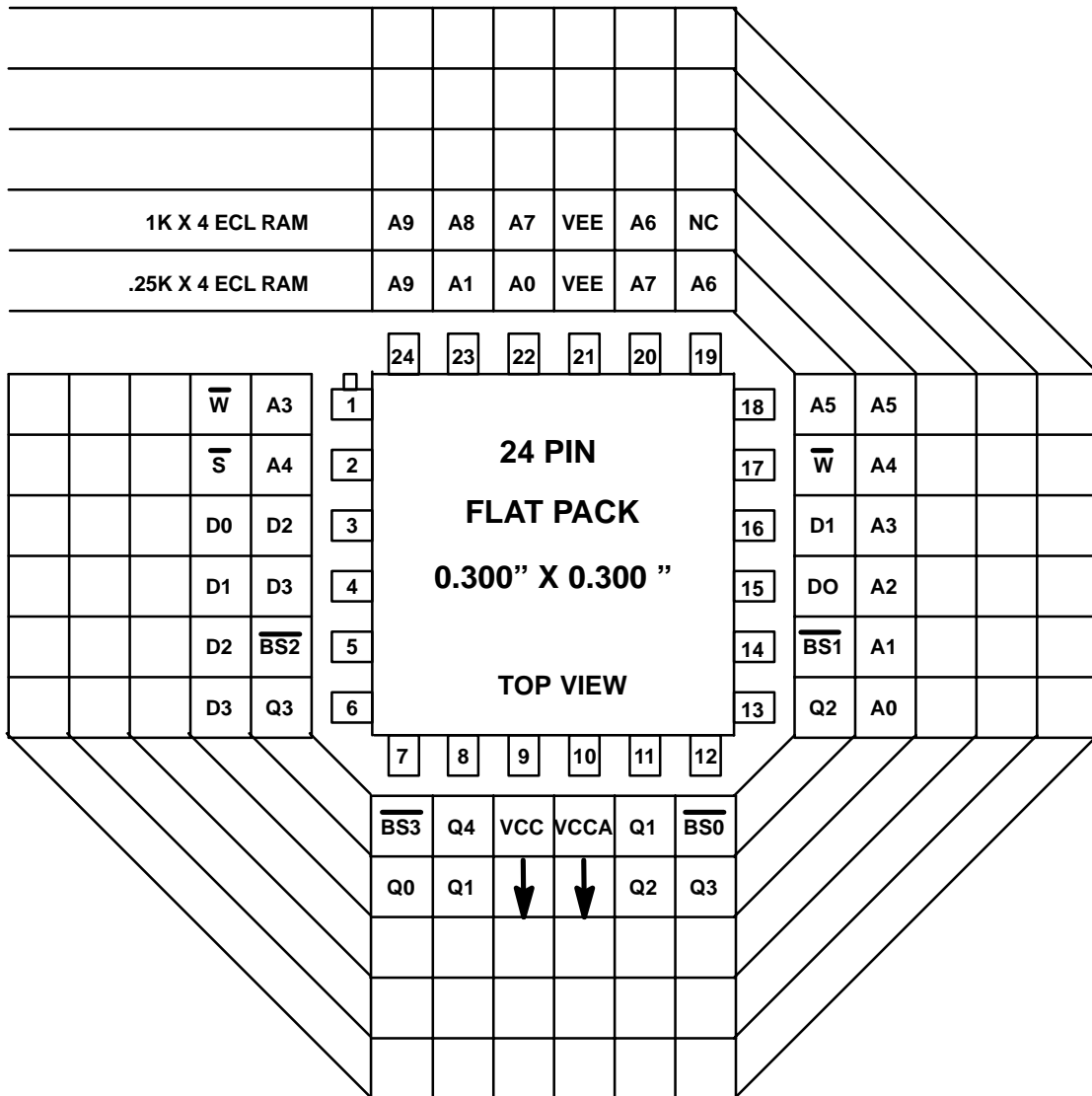
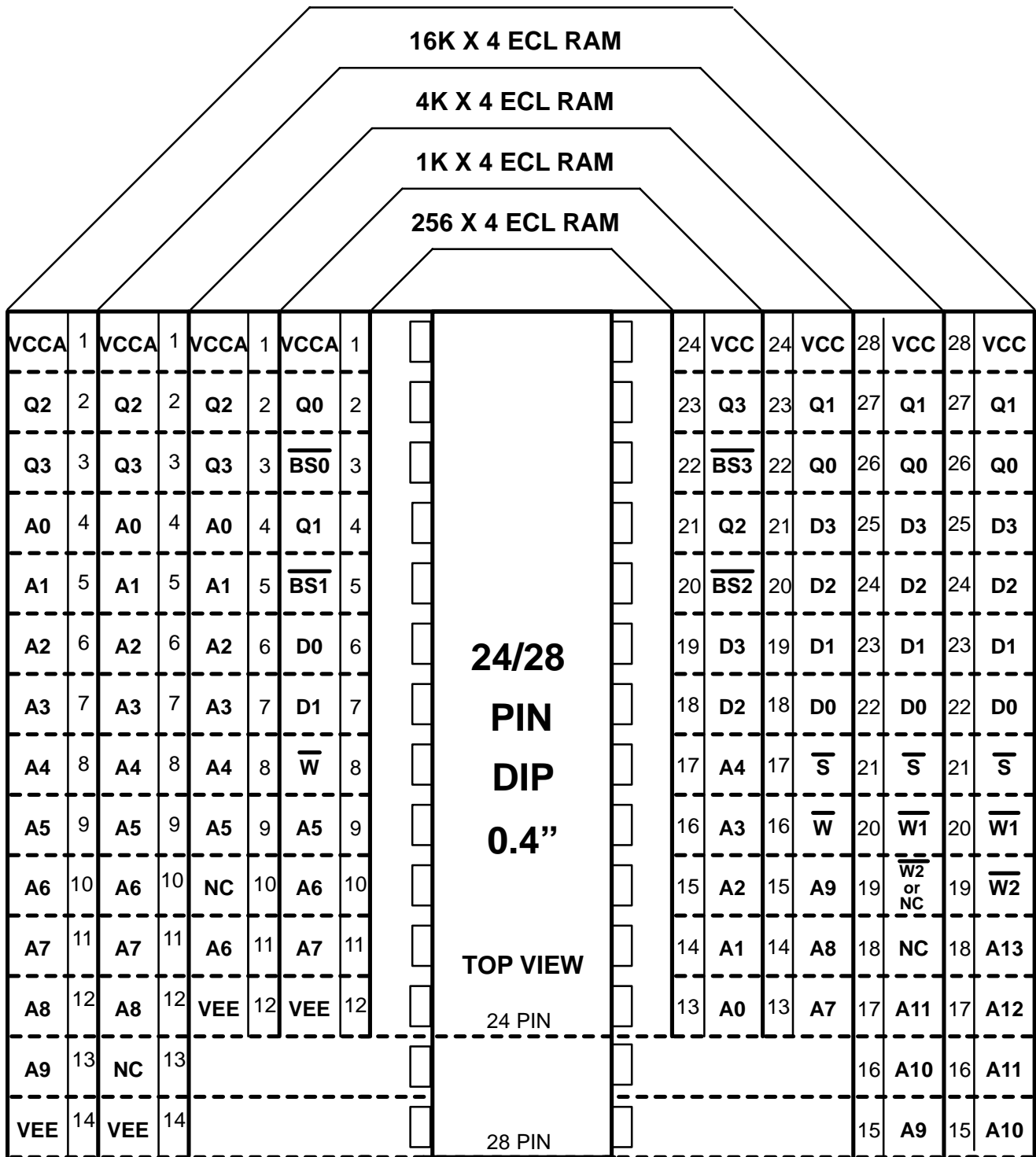


FIGURE 3.7.4-1  
256 BY 4, 100K ECL SRAM IN DIP  
1K TO 16K BY 4, 10K & 100K ECL SRAM IN DIP

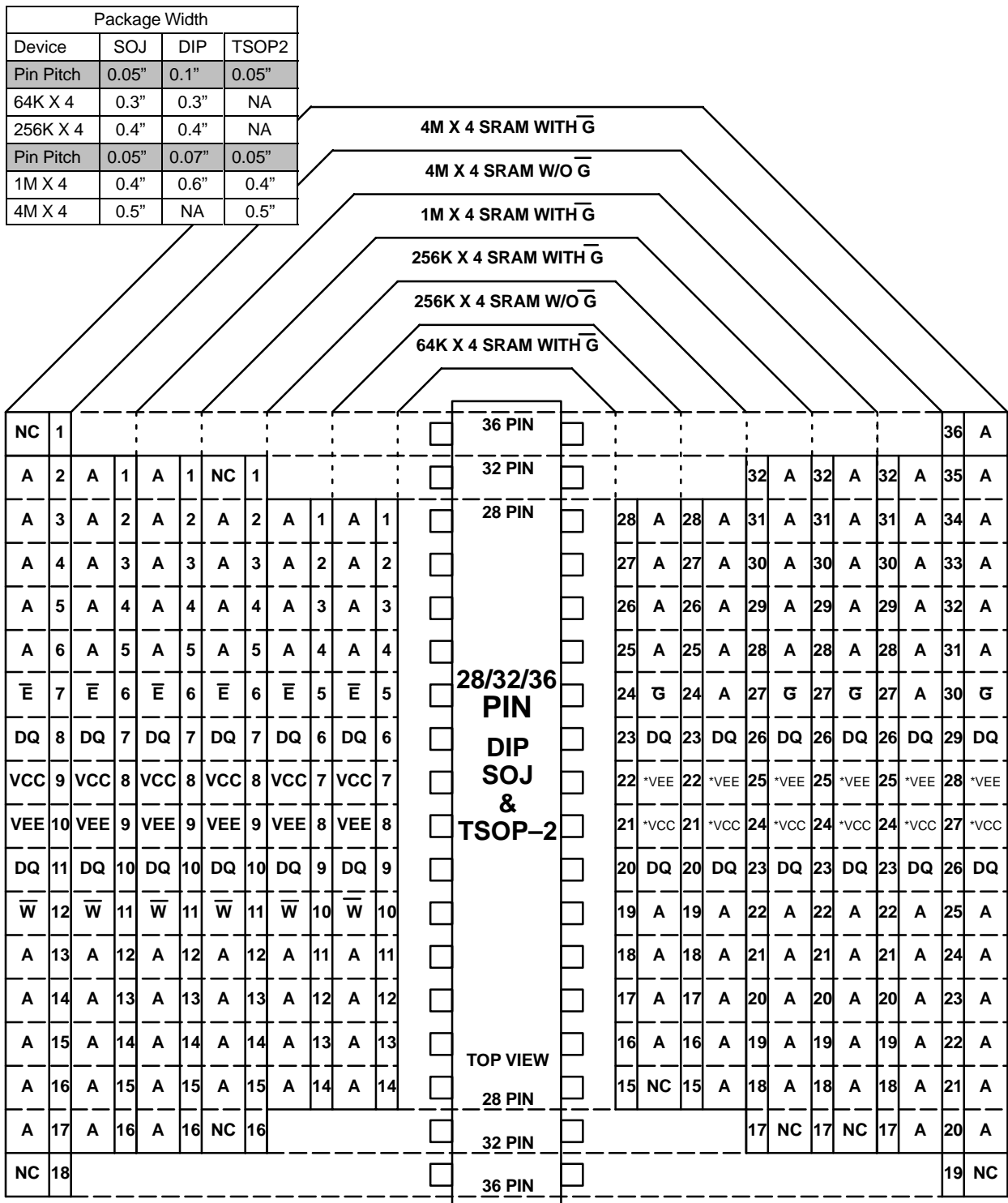


**FIGURE 3.7.4-2**  
**256 & 1K BY 4, 100K ECL SRAM IN SFP**



**FIGURE 3.7.4-4**  
**0.25K TO 16K BY 4, 10K & 100K ECL SRAM FAMILY IN DIP**  
Release 1



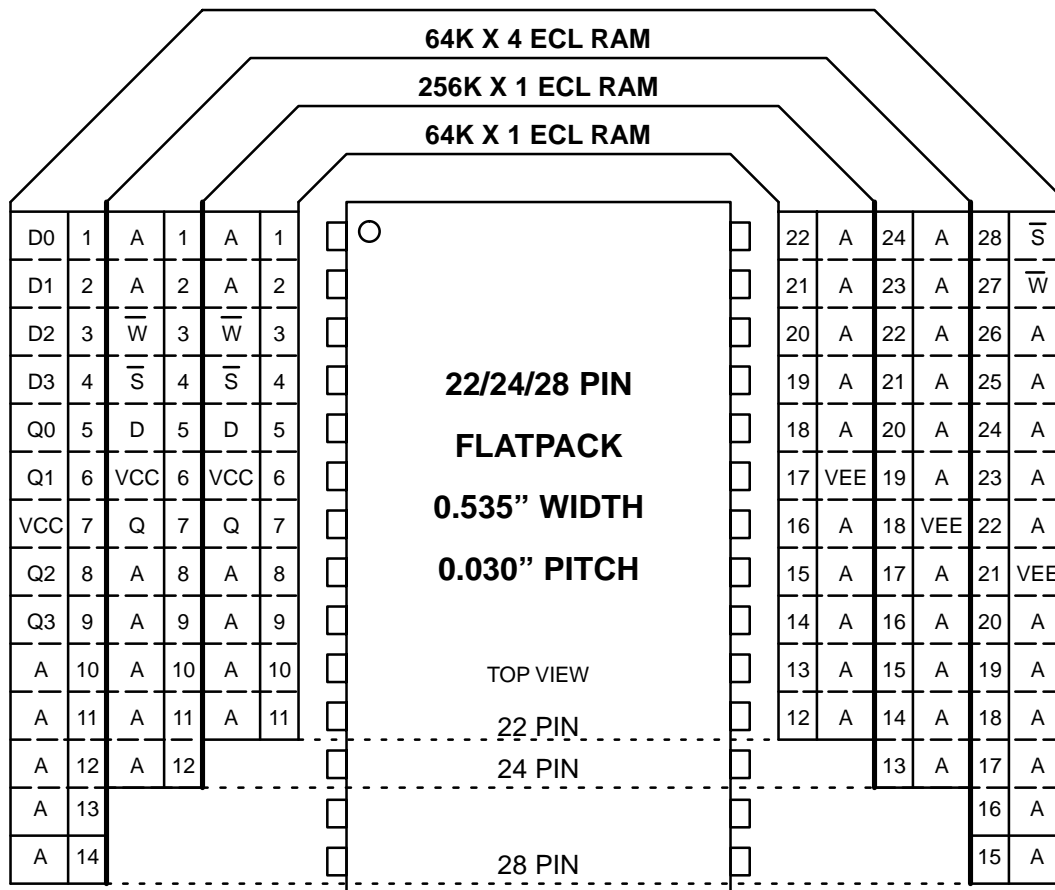


\* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

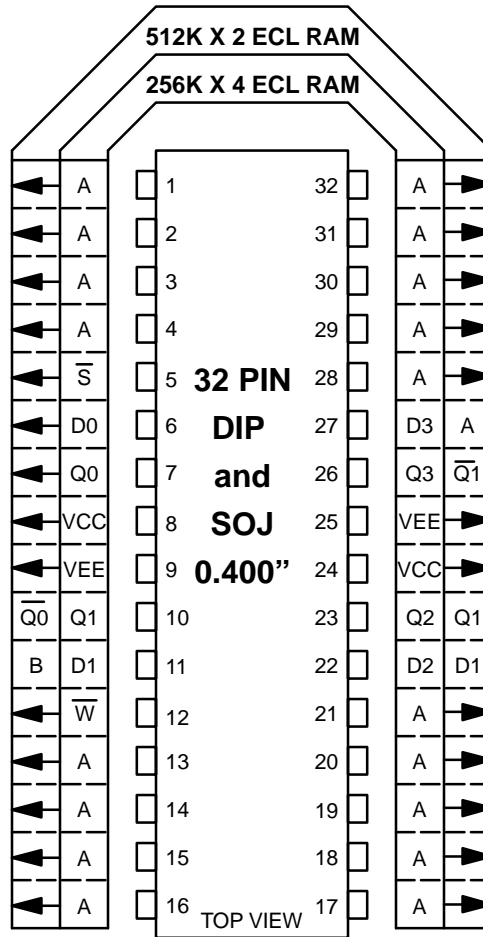
**FIGURE 3.7.4-6**  
**64K TO 4M BY 4 ECL SRAM FAMILY IN DIP, SOJ, AND TSOP-2**







**FIGURE 3.7.4-9**  
**64K BY 4 ECL SRAM IN FP**

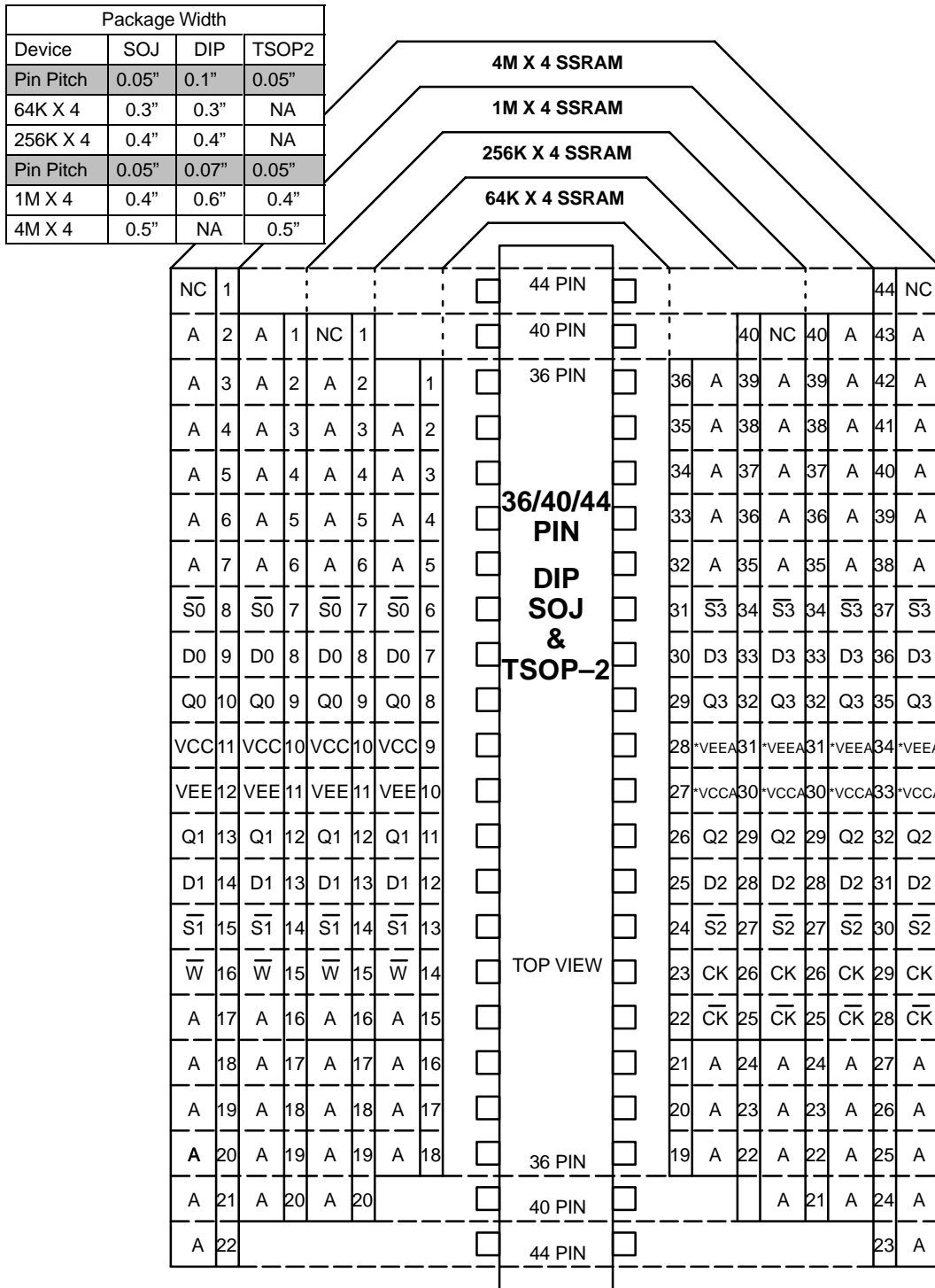


Multi-function Pin Truth Table Function vs. Mode Select Pin (11) Level		
Pin 11 Level/Function	> VEE / D1	VEE / B
RAM Organization	256K X 4	512K X 2
Pin #		
6	D0	D0
7	Q0	Q0
10	Q1	Q0
11	D1	B (VEE)
22	D2	D1
23	Q2	Q1
26	Q3	Q1
27	D3	A18

**FIGURE 3.7.4-10**  
**256K BY 4 or 512K BY 2 CONFIGURABLE ECL SRAM IN DIP AND SOJ**  
Release 2







\* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

FIGURE 3.7.4-13

64K TO 4M BY 4 BIT SELECTABLE ECL SSRAM FAMILY IN DIP, SOJ, AND TSOP-2