

3.7.1 Bit Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.1.1 – .25K & 1K BY 1 TTL SRAM IN DIP

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—16 PIN DIP, 0.3" WIDE
PIN ASSIGNMENT—Fig. 3.7.1-1

This standard was developed by Committee 42.1.

3.7.1.2 – .25K & 1K BY 1 TTL SRAM IN SCC

CAPACITY—.25K & 1K WORDS OF 1 BIT
PACKAGE—20 PIN (PAD) SCC, 0.350" X 0.350"
PIN ASSIGNMENT—Fig. 3.7.1-2

This standard was developed Committee 42.1.

3.7.1.3 – 4K TO 2M BY 1 TTL SRAM FAMILY IN DIP

CAPACITY—4K, 16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—18, 20, 22, 24, or 28 PIN DIP, 0.3", or 0.4" wide or UNDEFINED
PIN ASSIGNMENT—Fig. 3.7.1-3

3.7.1.4 – 16K BY 1 TTL SRAM IN RCC

CAPACITY—16K WORDS OF 1 BIT
PACKAGE—20 PAD (PIN) RCC, 0.290" x 0.425"
PIN ASSIGNMENT—Fig. 3.7.1-4

3.7.1.5 – 64K BY 1 TTL SRAM IN RCC

CAPACITY—64K WORDS OF 1 BIT
PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"
PIN ASSIGNMENT—Fig. 3.7.1-5

3.7.1.6 – 16K TO 2M BY 1 TTL SRAM IN SOJ

CAPACITY—16K, 64K, 256K, 1M, 2M WORDS OF 1 BIT
PACKAGE—24 or 28 PIN SOJ, 0.3" or 0.4" wide or UNDEFINED
Release 5 adds approval for the 256K X 1 part to be supplied in a 0.3" SOJ or TSOP-2
PIN ASSIGNMENT—Fig. 3.7.1-6

3.7.1.7 – 256K TO 16M BY 1 TTL SRAM AND 4M BY 1 SSRAM IN DIP, SOJ, AND TSOP-2

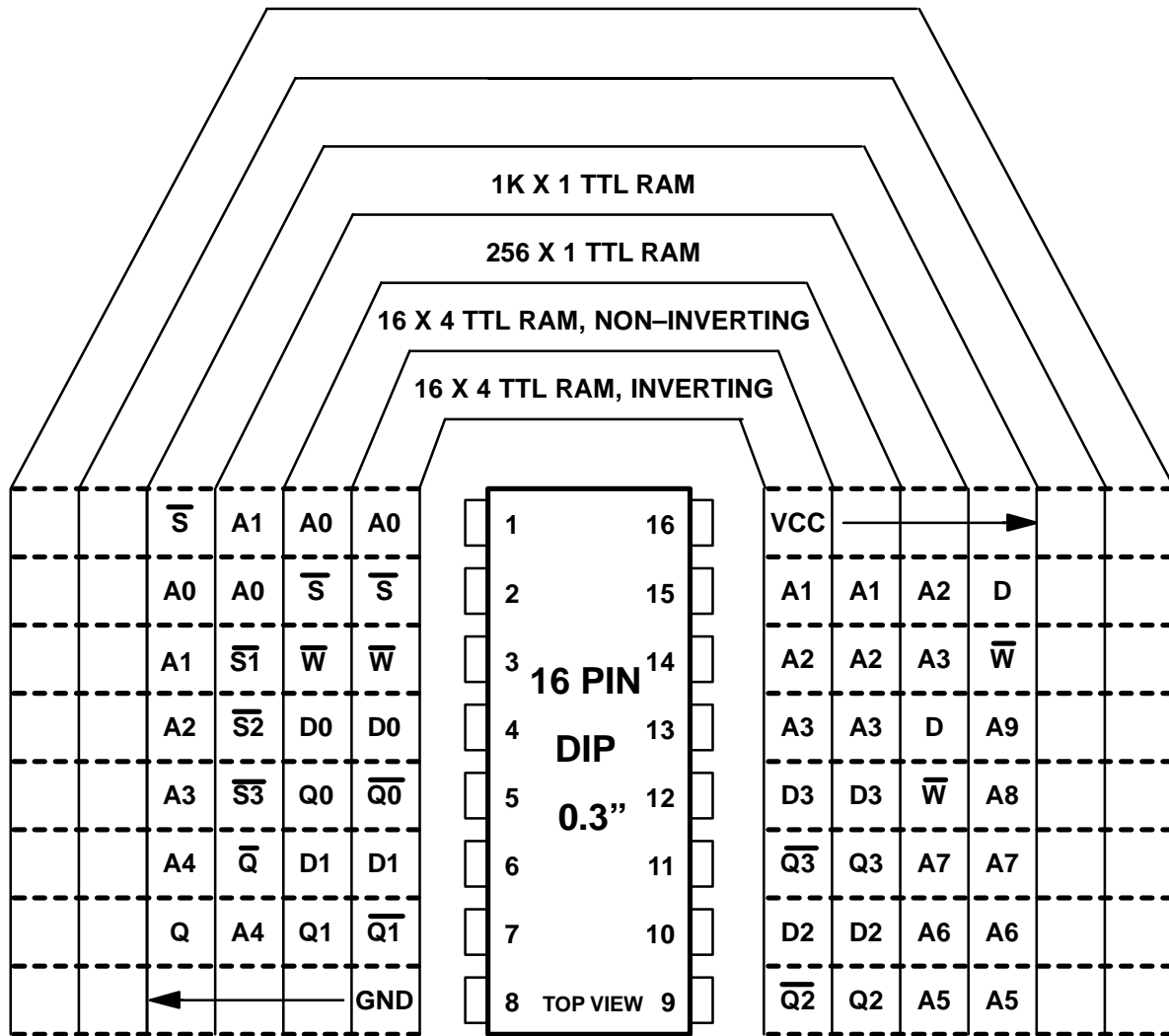
CAPACITY—256K, 1M, 4M, AND 16M WORDS OF 1 BIT
LOGIC FEATURES—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES
—SEPARATE DATA INPUT & OUTPUT PINS
—4M DENSITY PART APPROVED AS SYNCHRONOUS SRAM
PACKAGE—28 or 32 PIN SOJ, & TSOP2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES—MILTIPLE CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.1-7

3.7.1.8 – 256K BY 1 TTL SRAM IN RCC

CAPACITY—256K WORDS OF 1 BIT
PACKAGE—28 PAD (PIN) RCC, 0.350" X 0.550"
PIN ASSIGNMENT—Fig. 3.7.1-8

3.7.1.9 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP, SOJ, AND TSOP-2

CAPACITY—4M, 16M WORDS OF 1 BIT OR 1M, 4M WORDS OF 4 BITS
LOGIC FEATURES—THE DATA INTERFACE CONFIGURATION MAY BE SET TO X1 OR X4 UNDER CONTROL OF THE SIGNAL LEVEL TO A CONFIGURATION INPUT
PACKAGE—4M DENSITY, 32 PIN DIP, 0.6" with PP=0.07"; 32 PIN SOJ and TSOP-2, 0.4"
—16M DENSITY; 36 PIN SOJ AND TSOP-2, 0.5"
PIN ASSIGNMENT—Fig. 3.7.1-9



NC OR F

FIGURE 3.7.1-1
0.25K & 1K BY 1 TTL SRAM IN DIP

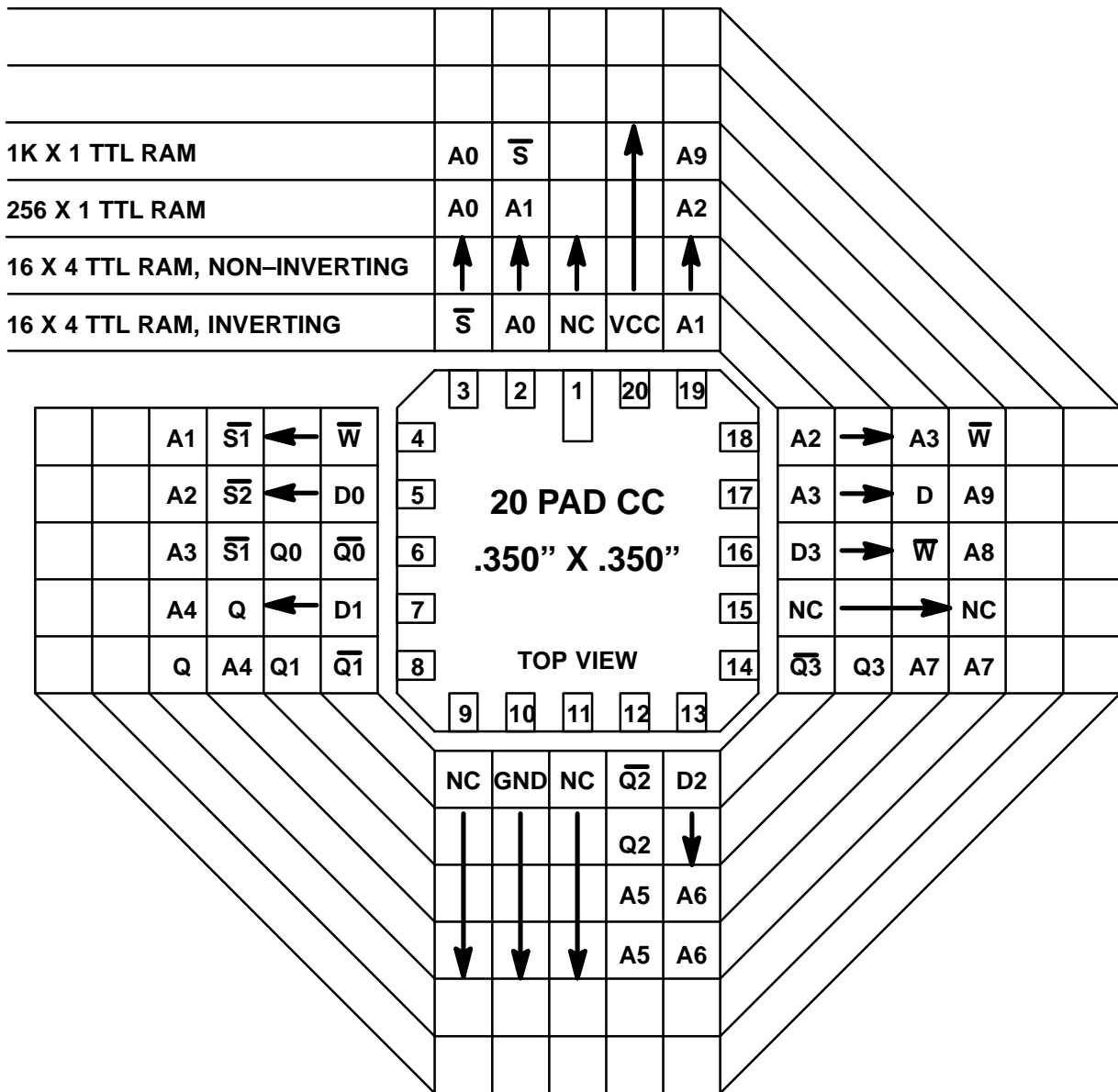


FIGURE 3.7.1-2
0.25K & 1K BY 1 TTL SRAM IN SCC

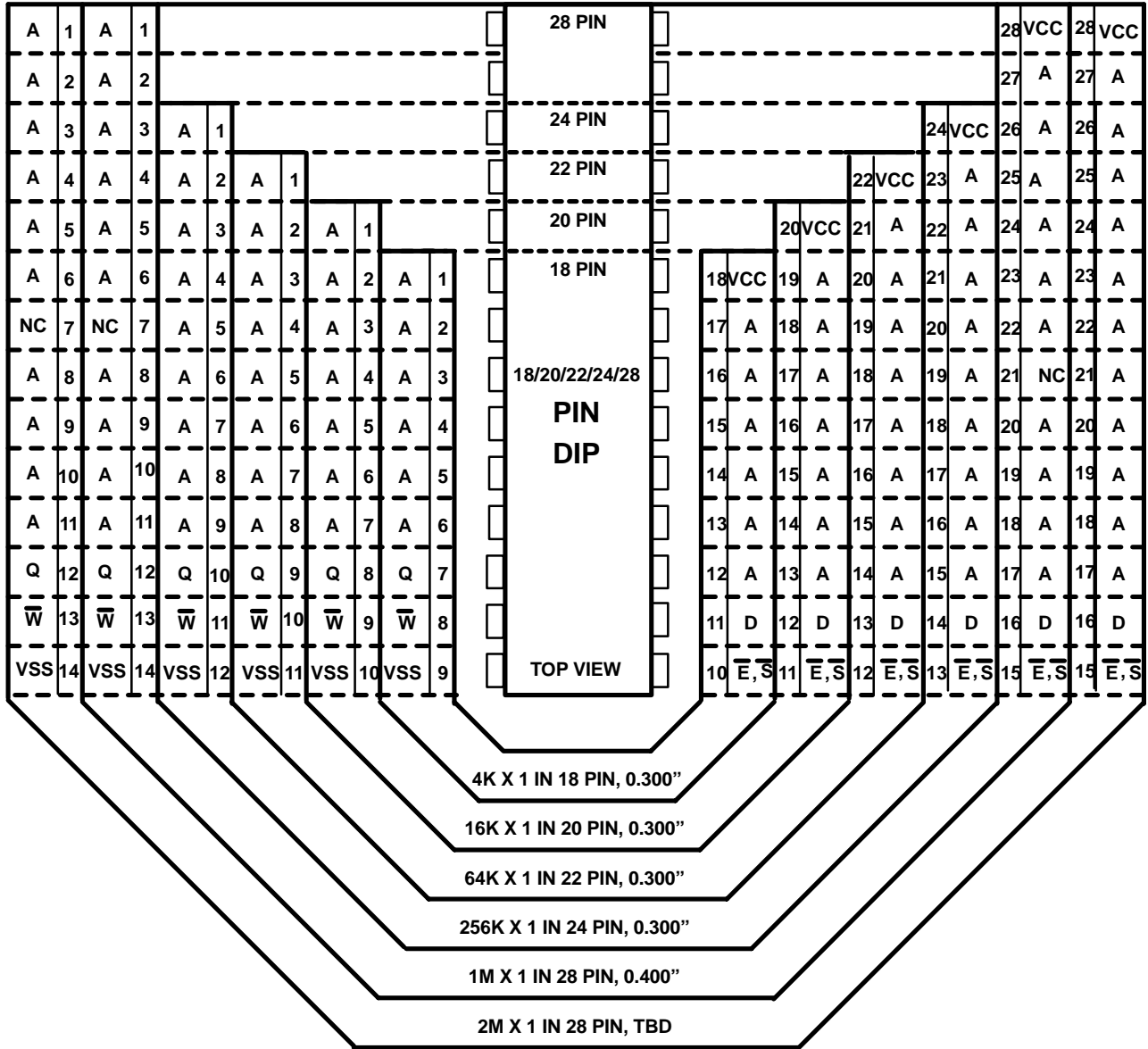


FIGURE 3.7.1-3
4K TO 2M BY 1 TTL SRAM FAMILY IN DIP

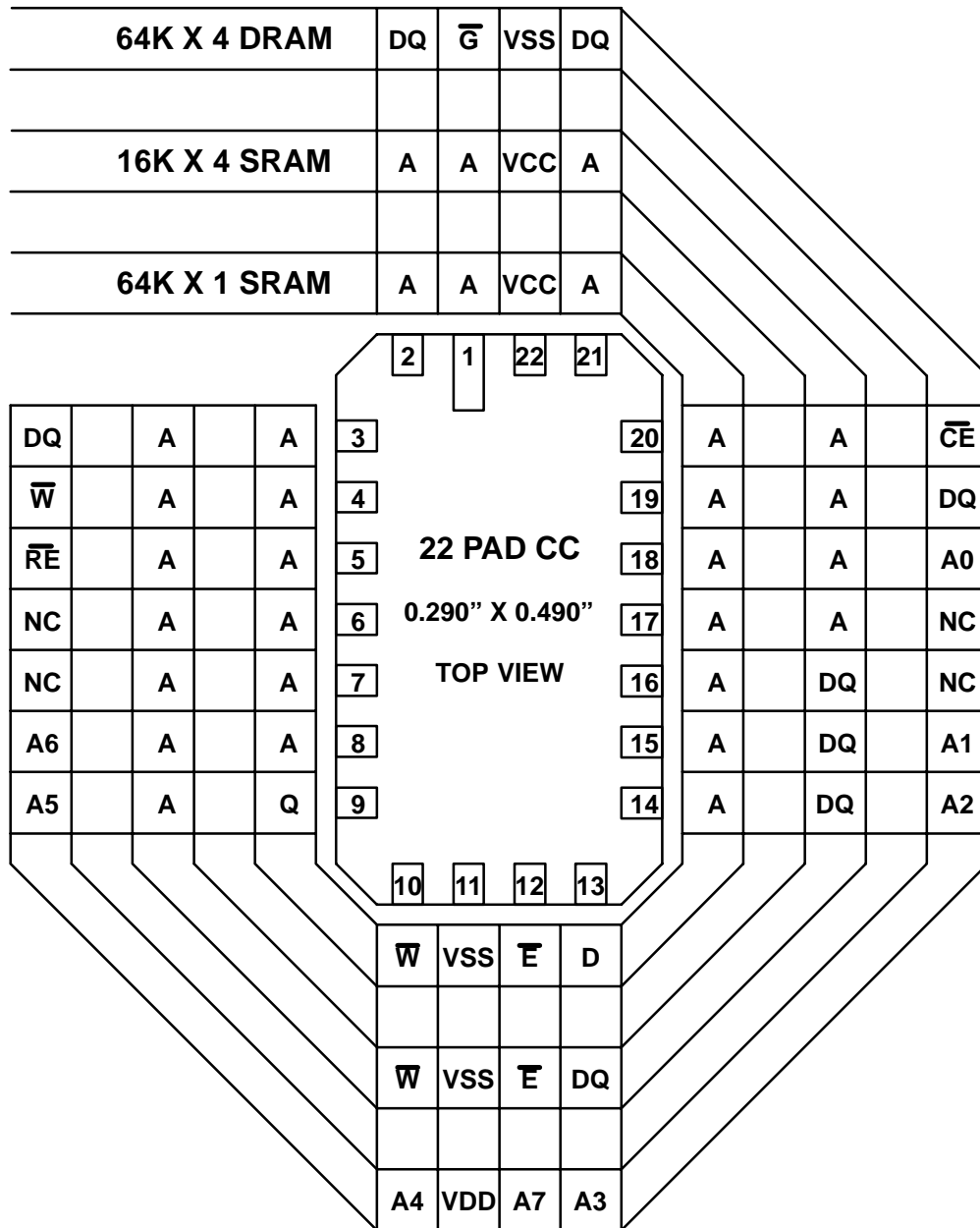
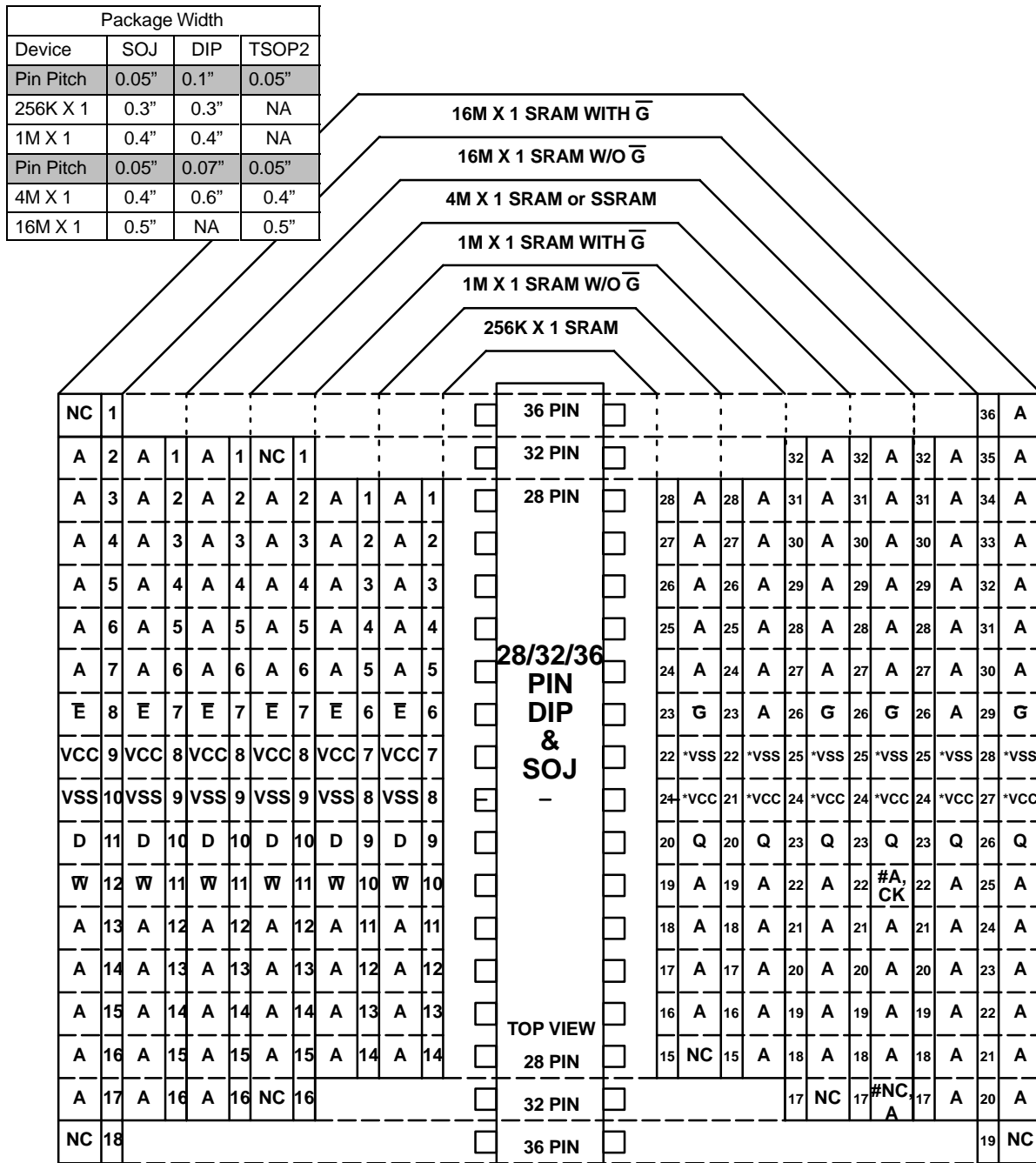


FIGURE 3.7.1-5
64K BY 1 TTL SRAM IN RCC



* These power pins may be VCC OR VCCA (VSS OR VSSA) as a Manufacturer option

NOTE: For the 4M X 1 devices, the pin assignments for pins 17 & 22 are different for the SRAM and SSRAM as follows.
For SRAM, P17 = NC, P22 = A
For SSRAM, P17 = A, P22 = CK

FIGURE 3.7.1-7

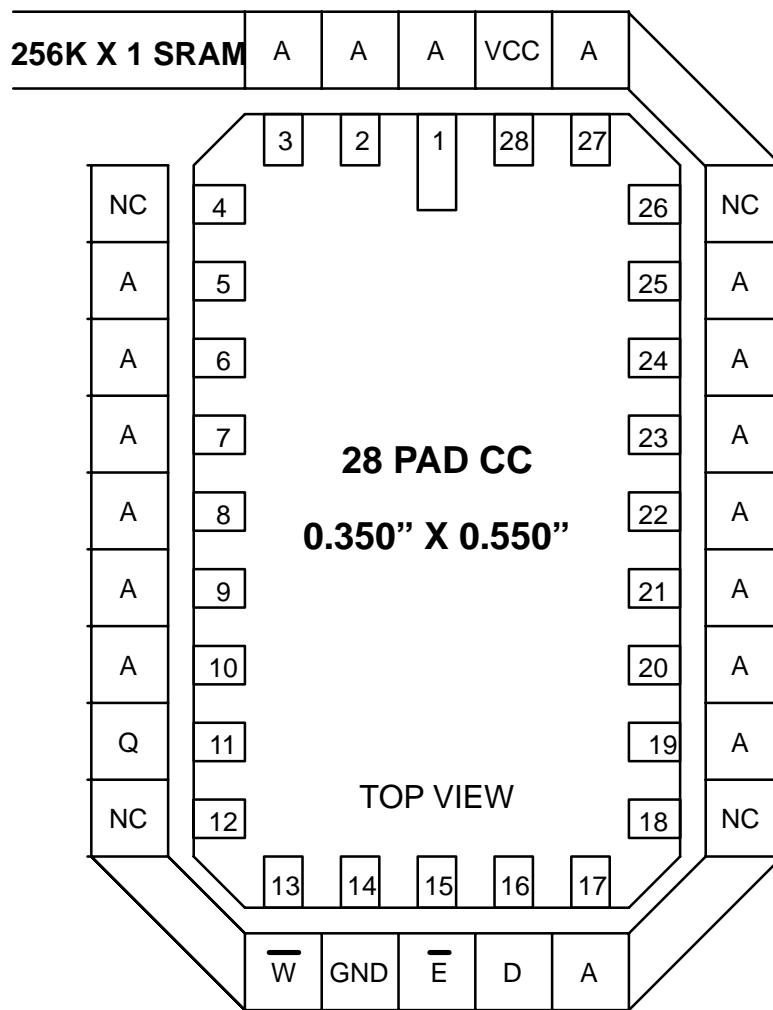


FIGURE 3.7.1-8
256K BY 1 TTL SRAM IN RCC

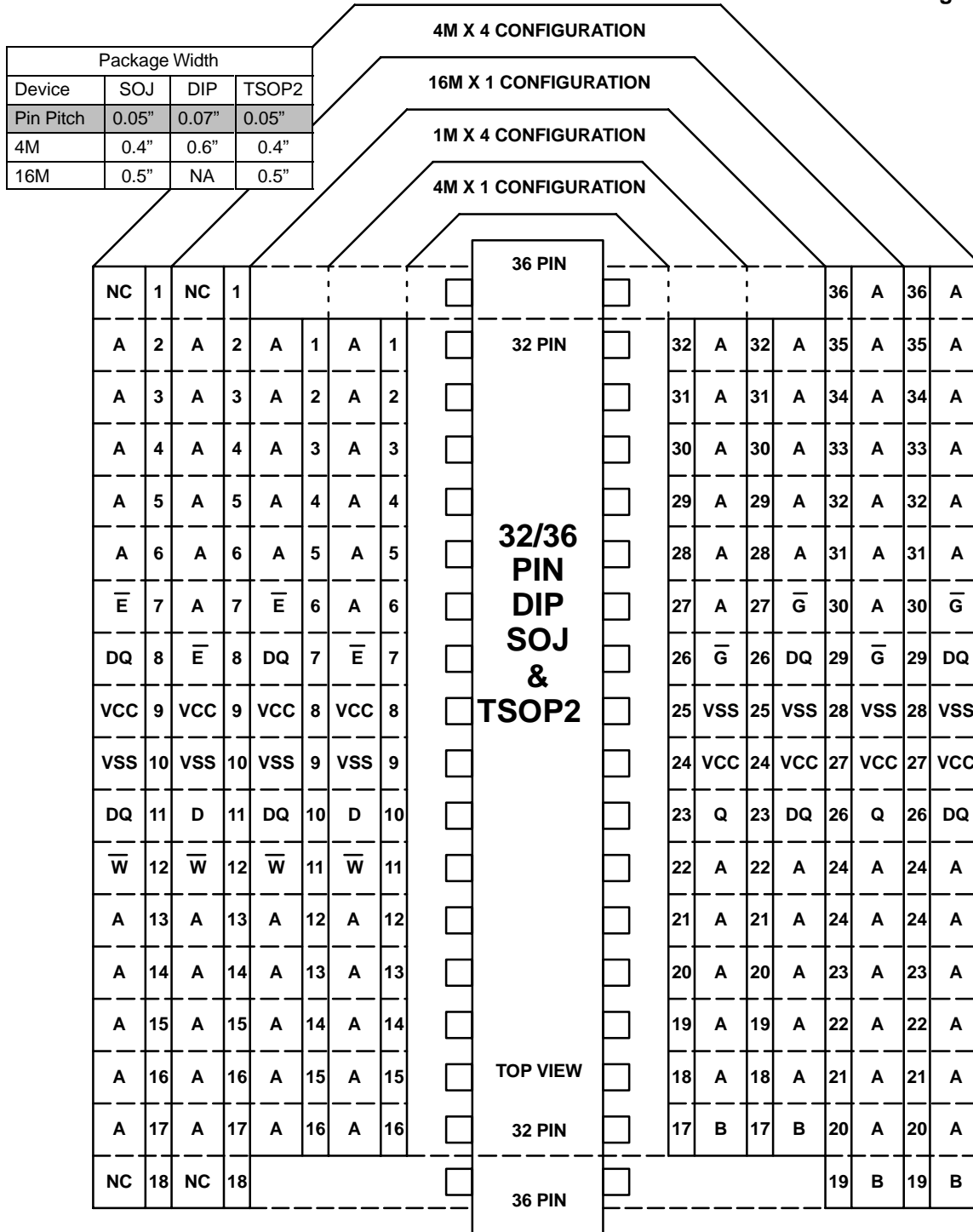


FIGURE 3.7.1-9

4M AND 16M CONFIGURABLE SRAM IN DIP, TSOP2, AND SOJ