

3.5.3 EEPROM EXTENDED FEATURES

There are a number of extended feature standards for EEPROMS that depend on the capacity and number of power supplies used in the design. The various standards and their location are listed as follows:

- 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARDS. PP 3.5.1-15 to 22
- DUAL POWER SUPPLY EEPROM COMMAND SET. Fig. 3.5.3.2, P 3.5.3-13
- EXTENDED FEATURE SET FOR EEPROM (256Kb and larger) . Sec. 3.5.3.1 following
- SINGLE POWER SUPPLY EEPROM COMMAND CODES. SEC. 3.5.3.3
- EEPROM TOGGLE BIT FEATURE (larger than 256 Kb) . Sec. 3.5.3.4

3.5.3.1 - EXTENDED FEATURE SET FOR EEPROM (256Kb and larger)

This standard specifies features beyond the existing pinout standards that need to be standardized for EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.3.2

3.5.3.1.1 - REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 256Kb and larger EEPROMs and must be implemented to be in compliance with this standard:

- Operate with a primary power supply of 5.0 V and lower nominal
- Operate in conformance with the defines standard command set
- Operate in conformance with the standard truth table
- Have read and write timing cycles which are consistent with the standard timing diagrams
- Contain Data & Address Latches for Write cycles
- Operate with self timed write cycles
- Operate with input levels between 0 and 5 Volts.
- DATA\ Polling

3.5.3.1.2 - OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:

- Page Write Mode with standard write cycle timings
- Minimum page size of 16 Byte in page write mode
- Software Data Protect Option
- Hardware Mass Erase (All 1's)
- Software Mass Erase (All 1's)

3.5.3.2 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices. This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.1-11

3.5.3.3 - SINGLE POWER SUPPLY EEPROM COMMAND CODES

These tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

3.5.3.4 - EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies. The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

3.5.3.5 - SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH) IN 86-PIN TSOP-2 AND 90-BALL FBGA

This section provides the Mode Register Architecture (Figure A1-11) and Truth Tables 1 and 2.

3.5.3.6 - EEPROM with two SPD Software Write Protect Methods

This section describes two methods to software write protect the EEPROM.

EEPROM EXTENDED FEATURE STANDARD (256Kb and greater)

The mandatory features, which are the minimum set necessary to achieve functional compability for 256Kb and larger EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optional features may be implemented at the manufacturers discretlon. However, if an optional feature defined In this standard is implemented, it must operate as specltied in this standard to be in compliance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible wltth the required and optlonal features in this standard.

BYTEWIDE EEPROM REQUIRED STANDARD FEATURES (256Kb and larger)

1. VDD SUPPLY IS 5 V OR LESS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1-1)
3. STANDARD COMMAND SET (Fig. A1-2)
4. STANDARD READ CYCLE TIMING (FIG. A1-3)
5. STANDARD BYTE WRITE CYCLE FEATURES
 - TIMING (FIG. A1-4)
 - DATA AND ADDRESS LATCHES
 - SELF-TIMED WRITE CYCLES
 - ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.
6. DATA POLLING (FIG. A1-5)
 - MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING

OPTIONAL FEATURES

1. PAGE WRITE MODE (FIG. A1-6)
 - STANDARD PAGE WRITE CYCLE TIMING
 - 16 BYTE MINIMUM PAGE SIZE (A0 - A3)
2. SOFTWARE DATA PROTECT OPTION (FIGS. A1-7 & A1-8)
3. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1-9)
4. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1-10)

EEPROM TRUTH TABLE					
\bar{E}	\bar{G}	\bar{W}	MODE	DQ	POWER
L	L	H	READ	Q	ACTIVE
L	H	L	WRITE	D	ACTIVE
H	X	X	STANDBY AND WRITE INHIBIT	HIGH Z	STANDBY
L	L	L	WRITE INHIBIT	HIGH Z	ACTIVE
L	H	H	WRITE INHIBIT	HIGH Z	ACTIVE

~NOTE: \bar{G} functions as both an output control and a write inhibit control in this EEPROM Standard.

FIGURE A1-1

SINGLE-SUPPLY EEPROM COMMAND SET

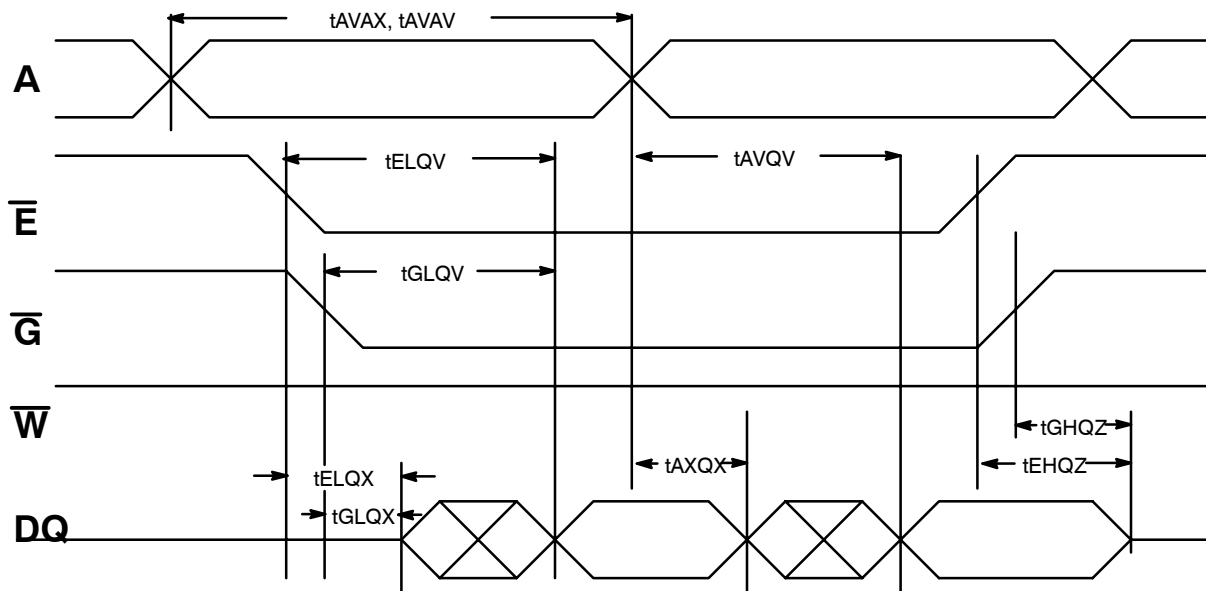
Bus Command Table

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Note: A0 is always LSB regardless of data width.

FIGURE A1-2

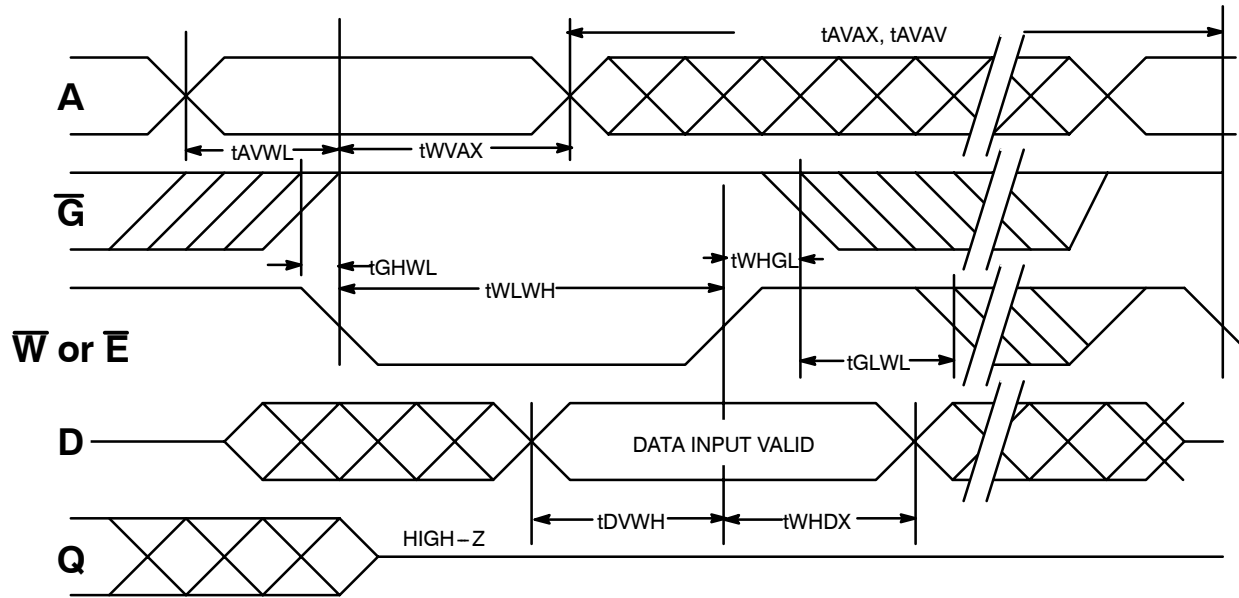
SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL	DESCRIPTION
t_{AVAX} , t_{AVAV}	ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)
t_{ELQV}	\bar{E} LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)
t_{AVQV}	ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) t_{GLQV}
t_{ELQX}	\bar{E} LOW TO ACTIVE OUTPUT
t_{GLQX}	\bar{G} LOW TO ACTIVE OUTPUT
t_{EHQZ}	\bar{E} HIGH TO HIGH-Z OUTPUT
t_{GHQZ}	\bar{G} HIGH TO HIGH-Z OUTPUT
t_{AXQX}	ADDRESS INVALID TO DATA OUT INVALID

FIGURE A1-3

SINGLE SUPPLY EEPROM READ CYCLE TIMING



SYMBOL (NOTE 1)	DESCRIPTION
t_{WLWL}, t_{ELEL}	\bar{W} OR \bar{E} LOW TO \bar{W} OR \bar{E} LOW CYCLE TIME (WRITE CYCLE TIME)
t_{AVWL}, t_{AVEL}	ADDRESS VALID TO \bar{W} OR \bar{E} LOW TIME (ADDRESS SETUP TIME)
t_{WLAX}, t_{ELAX}	\bar{W} OR \bar{E} LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)
t_{GHWL}, t_{GHLEL}	\bar{G} HIGH TO \bar{W} OR \bar{E} LOW TIME
t_{WHGL}, t_{EHGL}	\bar{G} HIGH HOLD TIME FROM \bar{W} OR \bar{E} HIGH
t_{WLWH}, t_{ELEH}	\bar{W} OR \bar{E} LOW TO \bar{W} OR \bar{E} HIGH (WRITE PULSE DURATION)
t_{GLWL}, t_{GLEL}	\bar{G} LOW TO \bar{W} OR \bar{E} LOW (\bar{G} LOW WRITE INHIBIT SETUP TIME)
t_{DVWH}, t_{DVEH}	DATA INPUT VALID TO \bar{W} OR \bar{E} HIGH (DATA SET-UP TIME)
t_{WHDX}, t_{EHDX}	\bar{W} OR \bar{E} HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1-4

SINGLE SUPPLY EEPROM DATA BAR POLLING AND AUTOMATIC WRITE OPERATION STATUS

IN PROGRESS	AUTO PROGRAMMING	DQ7	TOGGLE	0	0	0	RFU
	PROGRAMMING IN AUTO-ERASE	0	TOGGLE	0	0	1	
	ERASING IN AUTO-ERASE	0	TOGGLE	0	1	1	
EXCEEDED TIME LIMITS	AUTO PROGRAMMING	DQ7	TOGGLE	1	0	0	RFU
	PROGRAMMING IN AUTO-ERASE	0	TOGGLE	1	0	1	
	ERASING IN AUTO-ERASE	0	TOGGLE	1	1	1	

FIGURE A1-5

Definition of Automatic Algorithm

Automated Write

Data Command = 10h/ Byte Address and Data (1st/2nd bus cycle)

Write the automated program set-up command (10h) and program command (Byte address and program data). The device automatically times the program pulse width, provides the program verify to guarantee adequate data retention, and counts the number of pulses required for complete programming.

A data polling status bit (output pin DQ7) and a toggle bit status (output pin DQ6) provide feedback to the system as to the status of the programming operation. Either DQ7 or DQ6 can be used.

Data Polling- DQ7

While the automated algorithms are in operation, an attempt to read the device (address = don't care) will produce the compliment of the intended valid program or erase data on DQ7. Upon completion of the automated algorithm, an attempt to read the device will produce the valid data expected from DQ7.

The data polling feature is valid after the rising edge of the second W pulse of the two write pulse sequence.

Toggle Bit- DQ6

While the automated algorithms are in progress, successive attempts to read data (address = don't care) from the device will result in DQ6 toggling between the logic levels "1" and "0". Once the automated operation is complete, DQ6 will stop toggling and valid data will be read.

The toggle bit is valid after the rising edge of the first W pulse of the two write pulse sequence, unlike data polling which is valid after the rising edge of the second W pulse. This

feature allows the user to determine if the device is partially through the two write pulse sequence.

Exceeded Timing Limits - DQ5

DQ5 will indicate if the program or erase pulse counts have exceeded the specified limits. Under this condition, DQ5 will provide a logic "1" output.

Hardware Sequence Flash - DQ4

If the device has exceeded the specified erase or program time and DQ5 is at logic level "1", then DQ4 will indicate which step in the algorithm the device exceeded limits. A logic level "0" in DQ4 indicates that the programming limits were exceeded. A logic level "1" indicates erase limits were exceeded.

Sector Erase Timer- DQ3

After the completion of the initial sector erase command sequence, the sector erase time-out of 100 μ s will begin. If another sector erase command is written within the 100 μ s time-out window, the timer is reset.

If Data Polling or the Toggle bit (DQ6) indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is at logic level "1" the internally controlled erase cycle has begun. Any further attempts to write subsequent commands to the device will be ignored until the erase operation is completed which is indicated by Data Polling or the Toggle bit. If DQ3 is at logic level "0", the device will accept additional sector erase commands.

DQ0-DQ2 are reserved for future use.

SINGLE SUPPLY EEPROM OPTIONAL SOFTWARE DATA PROTECTION

- SOFTWARE DATA PROTECTION IS A DIFFERENT METHOD OF PREVENTING INADVERTANT WRITE OPERATIONS IN A NONVOLATILE MEMORY COMPARED TO THE "HARDWAREU METHODS, SUCH AS: E, G, AND W LOGIC COMBINATIONS, VCC LEVEL DETECTORS, AND POWER UP TIMERS.
- A SPECIFIC DATA AND ADDRESS SOFTWARE SEQUENCE MUST BE ISSUED TO ENABLE A SINGLE PAGE OR BYTE WRITE.
- DATA INPUT FORMAT: D7/D6/D5/D4/D3/D2/D1/D0
- ADDRESS FORMAT: A14/A13/A12/A11/A10/A9/A8/A7/A6/A5/A4/A3/A2/A1/A0

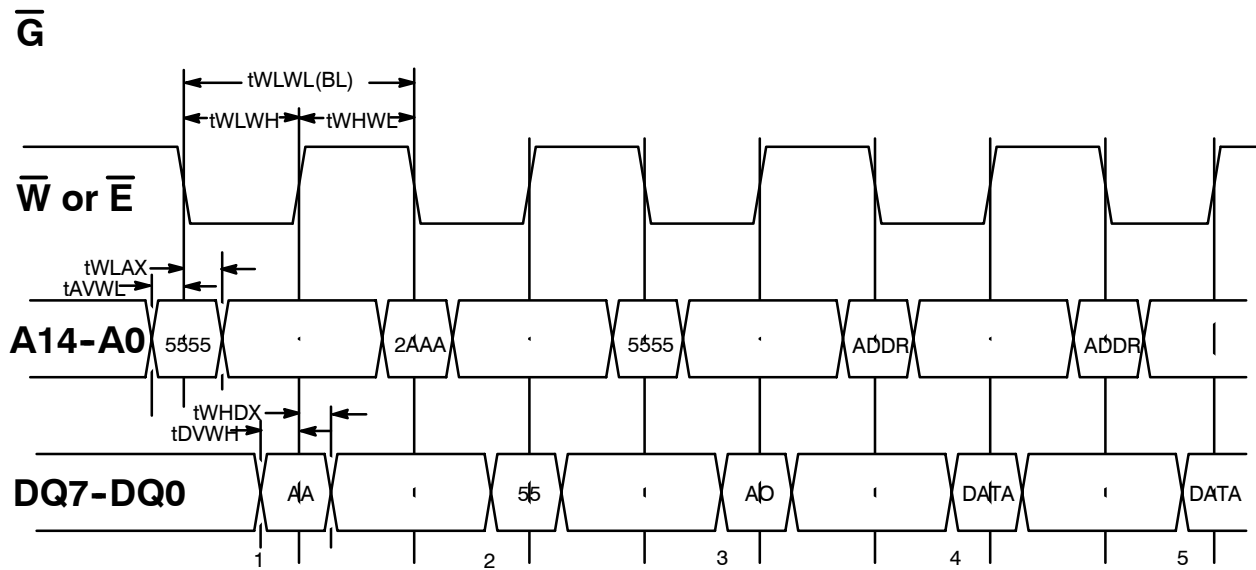
STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS WRITE"	5555H	AAH
2	"ACCESS WRITE"	2AAAH	55H
3	"ACCESS WRITE"	5555H	A0H
4	"PAGE WRITE"	Address	Data

- ALL WRITES MUST CONFORM TO THE PAGE MODE TIMING REQUIREMENTS FOR THE PART.
- SINCE THE PAGE ADDRESS IS CHANGED (A VIOLATION OF THE NORMAL PAGE MODE WRITE CYCLE), THE FIRST THREE "ACCESS" WRITES (STEPS 1-3) ARE USED ONLY FOR SOFTWARE ACCESS, NO DATA IS ACTUALLY WRITTEN TO THE EEPROM.
- THE FIRST TIME THIS SEQUENCE IS APPLIED TO THE PART A NON-VOLATILE BIT IS SET, WHICH RECONFIGURES THE PART FROM HARDWARE PROTECTED ONLY TO HARDWARE AND SOFTWARE SEQUENCE PROTECTED. ONCE THIS BIT IS SET, THE SOFTWARE SEQUENCE MUST BE USED TO WRITE TO THE PART.
- THE SOFTWARE PROTECTION CAN BE DISABLED AND THE PART RECONFIGURED TO HARDWARE-ONLY PROTECTION, BY APPLYING THE SIX STEP SOFTWARE SEQUENCE BELOW:

STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	20H

FIGURE A1-7

SINGLE SUPPLY EEPROM SOFTWARE DATA PROTECTION TIMING



NOTE 5: Software Data Protection Timings are referenced to \overline{W} or \overline{E} Inputs, whichever is last going LOW, and the \overline{W} or \overline{E} Inputs, whichever is first going HIGH.

SYMBOL (NOTE 5)	DESCRIPTION
$t_{WLWL}(BL)$, $t_{ELEL}(BL)$	\overline{W} OR \overline{E} LOW TO \overline{W} OR \overline{E} LOW BYTE LOW CYCLE TIME
t_{WLWH} , t_{ELEH}	\overline{W} OR \overline{E} LOW TO \overline{W} OR \overline{E} HIGH (WRITE PULSE DURATION)
t_{WHWL} , t_{EHEL}	\overline{W} OR \overline{E} HIGH TO \overline{W} OR \overline{E} LOW TIME (WRITE HIGH RECOVERY)
t_{AVWL} t_{AVEL}	ADDRESS VALID TO \overline{W} OR \overline{E} LOW TIME (ADDRESS SET-UP TIME)
t_{WLAX} , t_{ELAX}	\overline{W} OR \overline{E} LOW TO ADDRESS INVALID TIME (ADDRESS HOLD TIME)
t_{DVWH} , t_{DVEH}	DATA INPUT VALID TO \overline{W} OR \overline{E} HIGH (DATA SET-UP TIME)
t_{WHDX} , t_{EHDX}	\overline{W} OR \overline{E} HIGH TO DATA INPUT INVALID (DATA HOLD TIME)

FIGURE A1-8

SINGLE SUPPLY EEPROM OPTIONAL HARDWARE MASS ERASE (ALL 1'S) FEATURE

- IF A HARDWARE MASS ERASE MODE IS IMPLEMENTED ON THE 256K EEPROM, THE FOLLOWING CONVENTIONS MUST BE FOLLOWED:
- \bar{E} = LOW LOGIC LEVEL
- \bar{W} = LOW LOGIC LEVEL
- \bar{G} = SUPER VOLTAGE (WAVEFORM, LEVEL AND TIMING TO BE DETERMINED BY THE MANUFACTURER).
- DQ0 - DQ7 = ALL HIGH LOGIC LEVEL (FFH)
- A0 - A14 = DON'T CARE (EITHER HIGH OR LOW LOGIC LEVELS)

FIGURE A1-9

SINGLE SUPPLY BIT EEPROM OPTIONAL SOFTWARE MASS ERASE (ALL 1'S) FEATURE

IF A SOFTWARE MASS ERASE FEATURE IS IMPLEMENTED IN THE SINGLE SUPPLY EEPROM, IT MUST OPERATE BY APPLYING THE FOLLOWING SIX DATA/ADDRESS SEQUENCE TO THE PART.

STEP	MODE	A14-A0	DQ7-DQ0
1	"ACCESS" WRITE	5555H	AAH
2	"ACCESS" WRITE	2AAAH	55H
3	"ACCESS" WRITE	5555H	80H
4	"ACCESS" WRITE	5555H	AAH
5	"ACCESS" WRITE	2AAAH	55H
6	"ACCESS" WRITE	5555H	10H

- ALL ACCESS WRITES MUST FOLLOW THE STANDARD PAGE MODE WRITE CYCLE TIMING SPECIFIED FOR THE PART,
- NO DATA IS ACTUALLY WRITTEN TO THE EEPROM DURING THE "ACCESS" WRITES. ONCE THE 6 STEP SEQUENCE IS COMPLETED, THE PART AUTOMATICALLY COMPLETES A MASS ERASE CYCLE INTERNALLY.

FIGURE A1-10

3.5.3.2 - DUAL POWER SUPPLY EEPROM COMAND SET

The following command set is applicable to dual power supply EEPROMs of any capacity.

COMAND CODES		
1st CYCLE	2nd CYCLE	OPERATION DESCRIPTION
00		RESERVED
10		Automated Write
20	20	Automated Block Erase
20	D0	Automated Block Erase
30	30	Automated Chip Erase
40		Algorithmic Write
50		Reserved
60	60	Algorithmic Block Erase
70		Reserved
80		Reserved
90		Read ID
A0		Algorithmic Erase Verify
B0		Reserved
C0		Algorithmic Write Verify
D0		Reserved
E0		Reserved
F0		

NOTE: All operands are in HEX.

This Standard provides an optional command set for use with the dual supply voltage EEPROM devices. This command set comprehends algorithmic commands and adds a set of automatic codes. A device may respond to either or both operating modes.

The Standard is applicable to devices with all data interface widths..

3.5.3.3 - SINGLE POWER SUPPLY EEPROM COMMAND CODES

The following tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

Three cycle Command Codes

Command	1st Cycle		2nd Cycle		3rd Cycle	
	Address	Data	Address	Data	Address	Data
SDP Write Disable	5555	AA	2AAA	55	5555	A0
Product Identification Entry	5555	AA	2AAA	55	5555	90
Reset/Product Identification Exit	5555	AA	2AAA	55	5555	F0
Note: All operands are in HEX.						

Six Cycle Command Codes

Command	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
SDP Write Disable	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	20
Chip Clear (Erase)	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Note: All operands are in HEX												

All timings are per the EEPROM Software Data Protect Timing shown in Fig. A1-7

The address space required is encompassed by A0-A14; other address lines, e.g., A15, A16, can be at any level between VSS minimum and VCC maximum. The data space required is encompassed by DQ0-DQ7; other I/O lines, DQ8, DQ9, can be at any level between VSS minimum and VCC maximum.

3.5.3.4 - EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies.

- The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.
- Whenever the part is read during a nonvolatile write cycle, the data on DQ6 will toggle, i.e., alternate between high and low, on alternate read cycles. Any address can be used when reading to get the Toggle Bit output. Typically, the first toggle out is high (logic "1").
- When the nonvolatile write cycle automatically times out, normal valid data is read at the outputs for any provided address.
- A software routine uses this feature to determine when the nonvolatile write cycle is complete.
- The normal read cycle timing specified for the part must be used for Toggle Bit read cycles.
- An additional parameter, t_{WHGL} (t_{EHGL}), must also be specified for the toggle bit cycle. t_{WHGL} (t_{EHWL}) is the minimum time the system must wait from the last rising edge of \overline{W} (\overline{WE}) or \overline{E} until the Toggle Bit read cycle is initiated by the falling edge of \overline{G} (\overline{OE}).
- The actual completion of the nonvolatile write cycle is asynchronous with the system; therefore, a Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system will possibly get an erroneous result, i.e., valid data may appear to conflict with DQ6. In order to prevent spurious rejections, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the write cycle, otherwise the reject is valid.

3.5.3.5 - SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH) IN 86-PIN TSOP-2 AND 90-BALL FBGA

3.5.3.5.1 - MODE REGISTER ARCHITECTURE

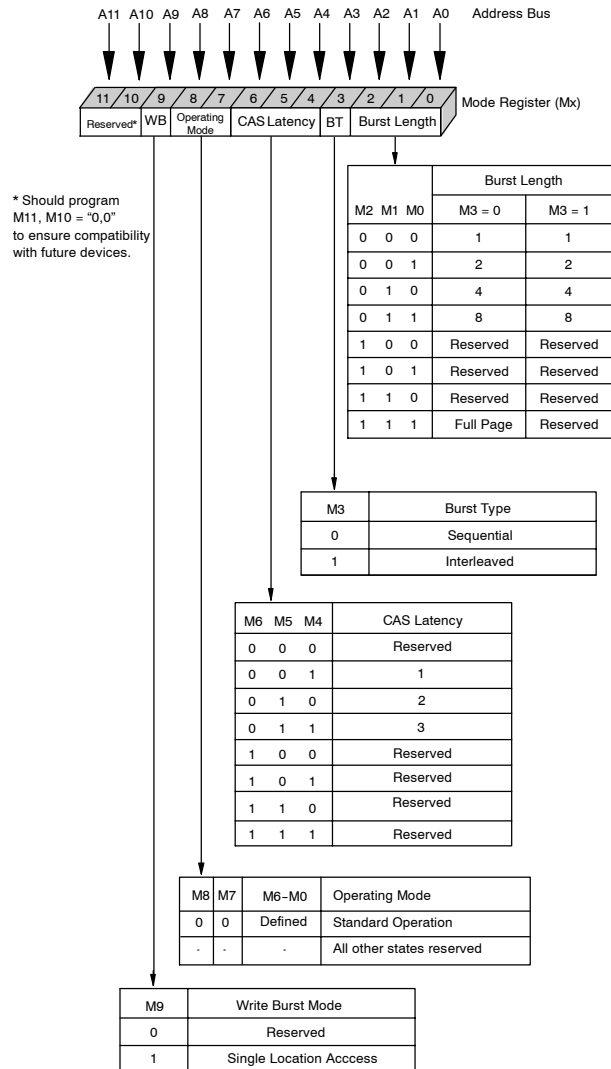


Figure A1-11
Mode Register Definition

3.5.3.5.2 - FUNCTIONAL TRUTH TABLES OF SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH)

TRUTH TABLE 1 : SDRAM-Compatible Interface Commands and DQM Operation

NAME (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	2
READ (Select bank, column and start READ burst)	L	H	L	H	X	Bank/Col	X	3
WRITE (Select bank, column and start WRITE)	L	H	L	L	X	Bank/Col	Valid	3, 4
BURST TERMINATE	L	H	H	L	X	X	Active	
ACTIVE TERMINATE	L	L	H	L	X	X	X	5
LOAD COMMAND REGISTER	L	L	L	H	X	ComCode	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	OpCode	X	8
Write Enable/Output Enable	-	-	-	-	L	-	Active	9
Write Inhibit/Output HighZ	-	-	-	-	H	-	HighZ	9

NOTE:

1. CKE is HIGH for all commands shown.
2. A0-A11 provide row address, and BA0 and BA1 determine which bank is made active.
3. A0-A7 provide column address, and BA0 and BA1 determine which bank is being read from or written to.
4. A PROGRAM SETUP command sequence (see Truth Table 2) must be completed prior to executing a WRITE.
5. ACTIVE TERMINATE is functionally equivalent to the SDRAM PRECHARGE command, however PRECHARGE (deactivate row in bank or banks) is not required for this memory. A10 LOW: BA0 and BA1 determine the bank being active terminated. A10 HIGH: All banks active terminated and BA0 and BA1 are "don't care".
6. A0-A7 define the ComCode, and A8-A11 are "Don't Care" for this operation. See Truth Table 2.
7. LOAD COMMAND REGISTER (LCR) replaces the SDRAM auto refresh or self refresh mode, which is not required for this memory. LCR is the first cycle for Flash Memory Command Sequences. See Truth Table 2.
8. A0-A11 define the OpCode written to the mode register. The mode register can be dynamically loaded each cycle, provided tMRD is satisfied. A default mode register value may be stored in the nvmode register. The contents of the nvmode register are automatically loaded into the mode register during device initialization.
9. Activates or deactivates the DQs during WRITES (zero-clock delay) and READS (two-clock delay).

Truth Table 2: Flash Memory Command Sequences

READ DEVICE CONFIGURATION																	
---------------------------	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

OPERATION	FIRST CYCLE					SECOND CYCLE					THIRD CYCLE						NOTES
	CMD	ADDR13	BANK ADDR	DQ	RP#	CMD15	ADDR	BANK ADDR	DQ	RP#	CMD	ADDR	BANK ADDR	DQ 14	RP#		
READ DEVICE CONFIGURATION	LCR	90H	Bank	X	H	ACTIVE	Row	Bank	X	H	READ	CA	Bank	X	H		5, 6
READ STATUS REGISTER	LCR	70H	X	X	H	ACTIVE	X	X	X	H	READ	X	X	X	H		
CLEAR STATUS REGISTER	LCR	50H	X	X	H	ACTIVE											
ERASE SETUP/CONFIRM	LCR	20H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	D0H	H/VHH		7, 8, 9
PROGRAM SETUP/PROGRAM	LCR	40H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	Col	Bank	DINH	H/VHH		7, 8, 9
PROTECT BLOCK/CONFIRM	LCR	60H	Bank	X	H	ACTIVE	Row	Bank	X	H	WRITE	X	Bank	01H	H/VHH		7, 8, 9, 10
PROTECT DEVICE/CONFIRM	LCR	60H	Bank	X	H	ACTIVE	x	Bank	X	H	WRITE	X	Bank	F1H	VHH		7, 8
UNPROTECT BLOCKS/CONFIRM	LCR	60H	Bank	X	H	ACTIVE	x	Bank	X	H	WRITE	X	Bank	D0H	H/VHH		7, 8, 9, 11
ERASE NVMODE REGISTER	LCR	30H	Bank	X	H	ACTIVE	x	Bank	X	H	WRITE	X		C0H	H		7, 8
PROGRAM NVMODE REGISTER	LCR	A0H	Bank	X	H	ACTIVE	x	Bank	X	H	WRITE	X	Bank	X	H		7, 8

3.5.3.6 - EEPROM with two SPD Software Write Protect Methods

This subsection describes two methods to software write protect the lower 128 bytes (bytes 0-127) of the EEPROM that is used to store the SPD information on the DDR2 DIMM modules. These contents may be protected by either the permanent software write protect (PSWP) method, or the reversible software write protect (RSWP) method

In the first method, the permanent software write protect (PSWP) method, a byte write to address "0-1-1-0-A2-A1-A0-0", where A(2:0) are the EEPROM address inputs, and with don't cares in the address byte and data byte, causes the lower 128 bytes to become permanently write protected. The bytes remain protected even after the EEPROM is powered down. Address A0 is driven to a voltage between 0 and VCC. Once the PSWP is set, a write to "0-1-1-0-A2-A1-A0-0" is no longer acknowledged by the EEPROM. This method has previously been used on many DDR DIMMs.

In the second method, the reversible software write protect method (RSWP), a byte write to address "0-1-1-0-0-0-1-0", where the EEPROM addresses A(2:0) are 0-0-VHV, and with don't cares in the address byte and data byte, causes the lower 128 bytes to become write protected. The bytes remain protected even after the EEPROM is powered down. Address pin A0 is driven to a voltage "VHV" which is a higher than normal voltage. Once the RSWP is set, a write to "0-1-1-0-0-0-1-0" with SA0=VHV is no longer acknowledged by the EEPROM.

The reversible software write protect (RSWP) may be cleared by a byte write to address "0-1-1-0-0-1-1-0", where the EEPROM addresses A(2:0) are 0-1-VHV, and with don't cares in the address byte and data byte. Clearing the RSWP allows the lower 128 bytes of the EEPROM to be writable. The bytes remain writable even if the EEPROM is powered down. Address pin A0 is driven to a voltage "VHV" which is a higher than normal voltage. If the permanent software write protect (PSWP) is set, a write to "0-1-1-0-0-1-1-0" with SA0=VHV is not acknowledged by the EEPROM.

	PIN	Preamble									RW
Command	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0
SET PSWP	SA2	SA1	SA0	0	1	1	0	SA2	SA1	SA0	0
SET RSWP	0	0	VHV	0	1	1	0	0	0	1	0
CLEAR RSWP	0	1	VHV	0	1	1	0	0	1	1	0

	Min	Max	Units	
VHV	7	10	V	Note: VHV-VCC > 4.8 V